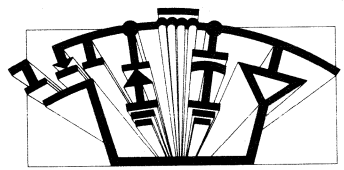
Unitrode Switching Regulated Power Supply Design Seminar Manual



Unitrode Corporation makes no representation that the use or interconnection of the circuits described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use or sell equipment constructed in accordance therewith.

NOTE: The information presented in this bulletin is believed to be accurate and reliable. However, no responsibility is assumed by Unitrode Corporation for its use.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

Resonant Mode Converter Topologies

by Bob Mammano

TOPIC 1

Resonant Mode Converter Topologies

Bob Mammano

Introduction to Resonant Power Conversion

Over the years we have seen power conditioning move from simple but extravagant linear regulators, through early low frequency pulse-width modulated systems, to high frequency square wave converters which pack the same power handling capabilities of earlier designs into a fraction of their size and weight.

Today, a new approach is upon us -- the resonant mode converter -- and while offering new benefits in performance, size, and cost, this new technology brings with it an added dimension of complexity. The purpose of this paper is to offer a means of categorizing and defining the various topologies and operating modes of resonant mode converters with the hope of enhancing the capability for design, analysis, and evaluation of these new power systems.

LINEAR REGULATORS -SIMPLE -POOR EFFICIENCY	1960's and earlier
SWITCHING REGULATORS -COMPLEX -HIGHER EFFICIENCY -DEMAND IC CONTROLS -HIGH NOISE -SLOW RESPONSE	1970's
CURRENT MODE CONTROL -IMPROVED REGULATION -BETTER PROTECTION -HIGHER BANDWIDTH	1980's

Fig. 1 - Power System Development History

5 to 20 kHz	-AUDIBLE NOISE -SLOW BIPOLAR SWITCHES -LARGE L's AND C's
20 to 100 kHz	-ABOVE AUDIBLE RANGE -FAST BIPOLAR TRANSISTOR -MAGNETICS BECOME IMPORTANT -SMALL SIZES
100 to 500 kHz	-POWER MOSFET SWITCHES -LOSSES IN L's AND C's -DIODE RECOVERY TIME -RFI AND EMI -PACKAGING PROBLEMS

Fig. 2 - Power Supply Switching Frequencies

First let us define a resonant converter as a power conditioning system which utilizes a resonant L-C circuit as a part of the power conversion process. All resonant converters operate in essentially the same way: a square pulse of voltage or current is generated by the power switches and this is applied to a resonant circuit. Energy circulates in the resonant circuit and some or all of it is then tapped off to supply the output. While basically simple, this principle can be applied in a wide variety of ways, creating a bewildering array of possible circuits and operating modes.

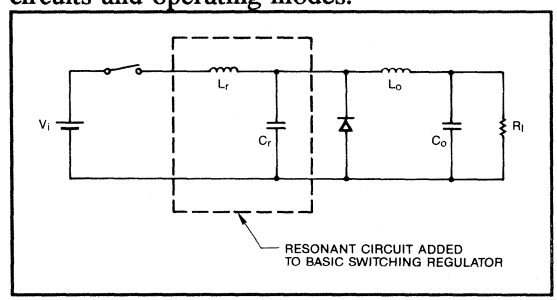


Fig. 3 - Basic Resonant Converter

Resonant Converter Advantages

Before getting into these, however, let's pause to review why we are even interested in resonant mode power conversion.

With the earliest switched-mode power converters, it became obvious that higher frequencies allow smaller L's and C's and this, in turn, should lead to smaller, lighter, and (hopefully) less costly systems. The down side to moving to higher frequencies, however, are the problems of greater susceptibility to parasitic capacitance and leakage inductance, greater stress in the switching devices, and increased EMI and RFI. A resonant mode system offers the potential of achieving the benefits while sidestepping many of the disadvantages of higher frequencies. With a resonant circuit in the power path, the switches can be configured to operate at either zero current or voltage points in the waveform, greatly reducing their stress levels; the resonant sine wave minimizes higher frequency harmon-

ADVANTAGES:
1. ZERO CURRENT SWITCHING
2. LOW COMPONENT STRESS
3. LOW EMI
4. USEFUL PARASITIC ELEMENTS
5. IMPROVED DIODE RECOVERY

DISADVANTAGES:
1. GREATER COMPLEXITY
2. HIGHER PEAK CURRENTS
3. NEW TECHNOLOGY LEARNING CURVE

Fig. 4 - Resonant Converter Advantages

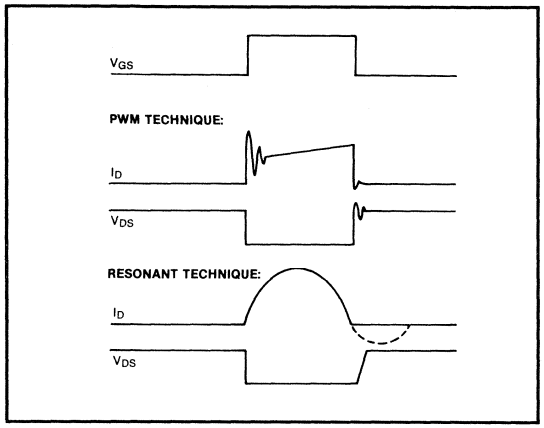


Fig. 5 - PWM vs. Resonant Switching

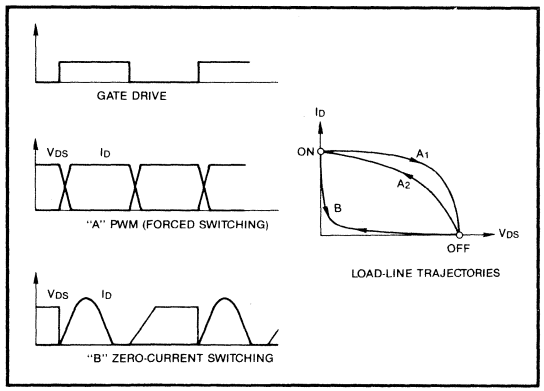


Fig. 6 - Switching Stress and Switching Loss

ics reducing noise levels; and since the circuit now requires inductance and capacitance, parasitic elements may enhance rather than detract from circuit performance. With these benefits, power systems operating in the range of 500 kHz to 2.0 MHz are now practical and - in fact - are already being produced by a few leading edge manufacturers.

Classifying Resonant Converters

Before attempting to classify resonant converter topologies, it might be helpful to introduce the concept of Resonant Switches. A resonant switch consists of a switching device (a transistor with a steering diode, for example) in combination with a two-element resonant circuit. This resonant switch may be configured in several different ways, some of which are shown in Figure 7, but they always perform the same function as the conventional switch in a square wave converter. It is a useful concept as most resonant mode circuit topologies can be visualized as a conventional PWM circuit with the power switch replaced with a resonant switch. We will discuss the operation of the various switch configurations in greater detail as we get into the circuit topologies but first, let's take an overview of some of the circuit options.

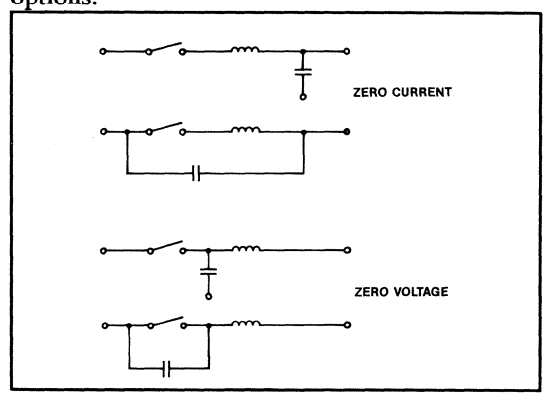


Fig. 7 - Resonant Switches

To bring some order and ease in understanding the broad range of circuit choices which are possible as we move to resonant mode operation, it helps to establish a system to classify resonant topologies by defining the following operating characteristics:

1. Is the load in series or in parallel with the resonant circuit elements?
2. Is the control system a fixed or variable frequency type?
3. Does current (or voltage) in the resonant circuit flow continuously or is it equal to zero for some portion of the switching cycle?

1. SERIES OR PARALLEL LOADED?
2. FIXED OR VARIABLE FREQUENCY?
3. CONTINUOUS / DISCONTINUOUS RESONANCE?
4. ZERO CURRENT OR VOLTAGE SWITCHING?
5. HALF OR FULL CYCLE CONDUCTION?

Fig. 8 - Classifying Resonant Converters

For discontinuous operation, it is also important to know:

4. Is the switching designed for zero current or zero voltage activation, and
5. Does the energy in the resonant circuit flow in only one direction or is there a full cycle before it returns to stop at zero?

The general properties of any resonant converter are completely dependent on these options, so they are a good basis to use as a starting point in understanding the principles involved.

Series or Parallel Loading

Since resonant converters operate by putting energy into a resonant circuit and then transferring some or all of it into the load, we need to know that there are two ways this may be accomplished as shown in Figure 9. If the load is in series with the resonant circuit elements, as in Fig. 9A, we call it a series loaded converter and the operating characteristics tend toward a current source with a high impedance output.

Parallel loading is the opposite, with a low impedance voltage source output as shown in Fig. 9B. Both modes have application to power systems with high voltage outputs usually using series loaded current source drive and low voltage supplies using parallel loading.

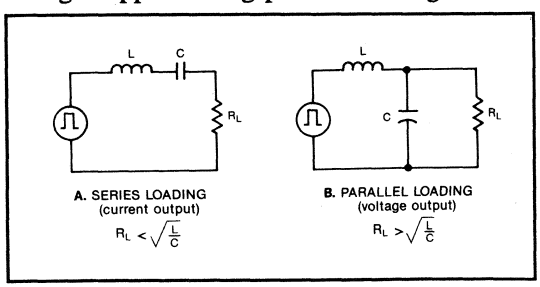


Fig. 9 - Resonant Mode Loading

Fixed or Variable Frequency

Resonant converters may be configured for either constant or variable frequency operation, but these choices infer significant differences in their operation. Fixed frequency control systems use conventional pulse width modulation to change the output in response to a control input, as shown in Figure 10. This forces a fixed-frequency system to have at least one non-zero switching transition and possibly two, thereby voiding one of the more significant reasons for choosing to use a resonant mode topology. This would usually preclude its use unless system considerations required a synchronized frequency operation.

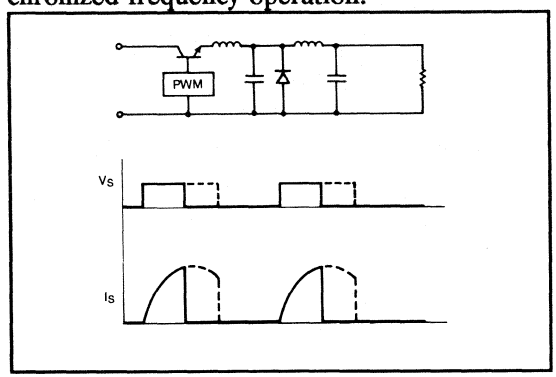


Fig. 10 - Fixed Frequency Resonance

Variable frequency operation, however, needs to be subdivided by the third classification: whether the resonant circuit current is continuous or discontinuous. A circuit operating in the continuous resonant mode uses the slope of the resonant circuit impedance curve to

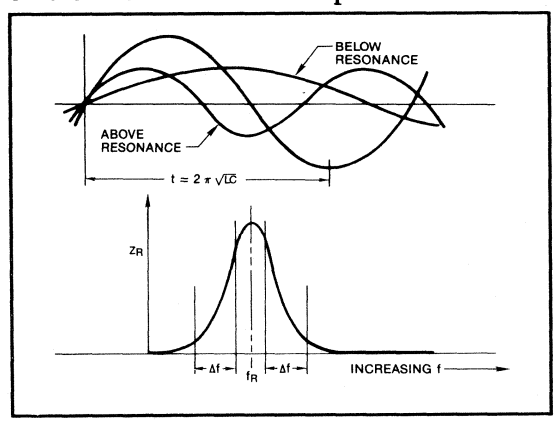


Fig. 11 - Variable Frequency Continuous Resonance

control the output. As shown in Figure 11, the circuit can operate either above or below resonance but the principle is the same: that the control circuit changes the frequency to move either toward or away from resonance, and thereby controls the amount of energy which is transferred into the resonant circuit - and therefore to the load.

While many practical systems have used continuous conduction, variable frequency operation, there are several disadvantages:

1. The non-zero switching adds stress to the transistors.
2. As the frequency approaches resonance, peak currents or voltages can get very high, adding stress to the resonant components.
3. The control transfer function is very non-linear following the resonant impedance curve.

The major advantage of the continuous mode of operation is that the frequency varies over a much smaller range than with the discontinuous mode.

Discontinuous Resonance

The discontinuous operating mode works by supplying constant packets of energy to the load with the rate, i.e. frequency, determined by load power demand.

Perhaps the most popular and important class of resonant converters with variable frequency and discontinuous current is often called *Quasi-Resonance*. Most of the remaining portion of this discussion will be oriented toward this Quasi-Resonant converter category

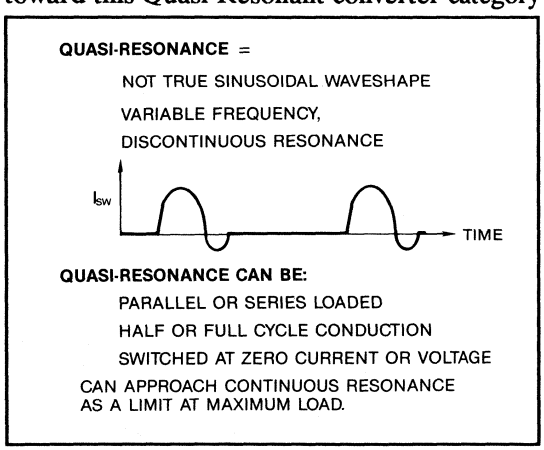


Fig. 12 - Quasi-Resonance Definition

but even within this class there are still many variations in circuit operation.

As indicated in Figure 12, quasi-resonant circuit waveforms are not sinusoidal, but have two essentially linear portions interspersed with two sinusoidal portions.

A quasi-resonant converter control loop is usually configured as shown in Figure 13 with a pulse generator driving the resonant circuit at a repetition rate defined by the control circuit. The pulse generator may be set for constant pulse width - defined by the resonant circuit - or set to sense zero crossing of either current or voltage. With maximum loading and low line voltage, a quasi-resonant converter can approach continuous resonance as a limit when the individual pulses run together.

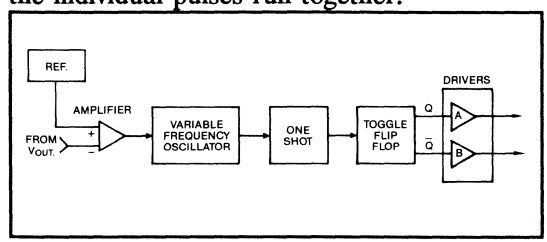


Fig. 13 - Quasi-Resonant Control

Within the variable frequency, discontinuous mode of operation there are two remaining decisions a designer must make which will have significant effect on the characteristics of his power supply:

Zero-Current or Zero-Voltage Switching

Since reducing the stress on the switching components is a major incentive for resonant operation, we need to understand ways in which that might be accomplished. The most common approach, and the one to which most of this paper will address, is to switch at zero current so that the dynamic load line stays very close to the V-I axes. With a sine wave current shape, it should be clear that the peak current will be close to twice the value of an equivalent square wave system, and although this adds to the I^2R losses, most semiconductor devices are much more comfortable with this than the high peak power levels reached with square wave switching.

Of course, low switching stress may also be achieved by switching at zero voltage and one

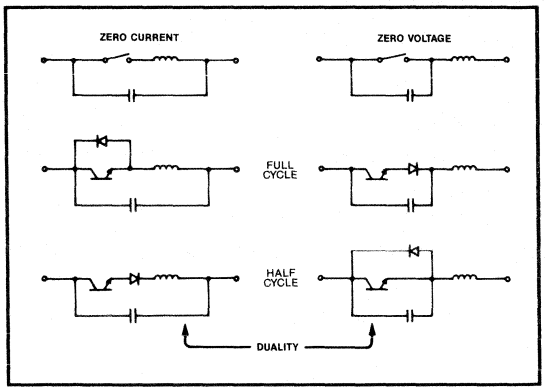


Fig. 14 - Switch Activation

should realize that this approach is merely a dual of zero current as shown in Figure 14. The choice of which approach is best is usually determined by whether the parasitic inductance of the load or the capacitance of the switch is the bigger problem. Zero voltage switching is primarily appropriate with very high frequency operation where rapid charging and discharging of the semiconductor switch capacitance could represent substantial power loss. Note from the duality of characteristics shown in Figure 15

CHARACTERISTIC	ZERO-CURRENT SWITCH	ZERO-VOLTAGE SWITCH
CONTROL	CONSTANT ON-TIME	CONSTANT OFF-TIME
SWITCH VOLTAGE WAVEFORM	≈ SQUARE	≈ SINUSOIDAL
SWITCH CURRENT WAVEFORM	≈ SINUSOIDAL	≈ SQUARE
LOAD RANGE	Rmin → ∞	0 → Rmax
SWITCH LIMITATIONS	PEAK **ON** CURRENT	PEAK **OFF** VOLTAGE

ZERO-VOLTAGE USAGE:

1. VERY HIGH FREQUENCIES WHERE SWITCH PARASITIC CAPACITANCE WOULD CAUSE EXCESSIVE POWER LOSS AT SWITCHING

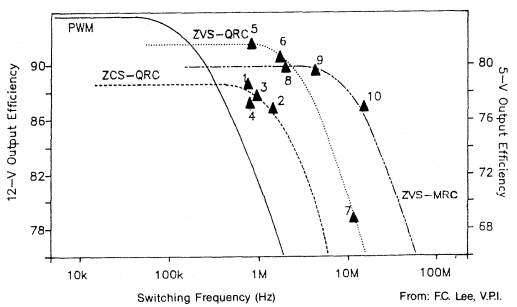


Fig. 15 - Switching Techniques Compared

that zero voltage switching, with its sine voltage waveform, would force high peak voltages on the switch and, although it loses control at light loads, is unaffected by a short circuit.

Half or Full Cycle Conduction

In a quasi-resonant circuit, energy transmission begins and ends at zero followed by a wait defined by the needs of the load. Full or half cycle conduction relates to whether each pulse will allow current to flow only from source to load, or ring in the resonant circuit allowing surplus energy to return to the source. The waveforms shown in Figure 16 describe the operation which is controlled by the placement of diodes either in series or antiparallel with the switch. Effective power supplies can be implemented with either approach but, as one would expect, there are significant differences in their characteristics.

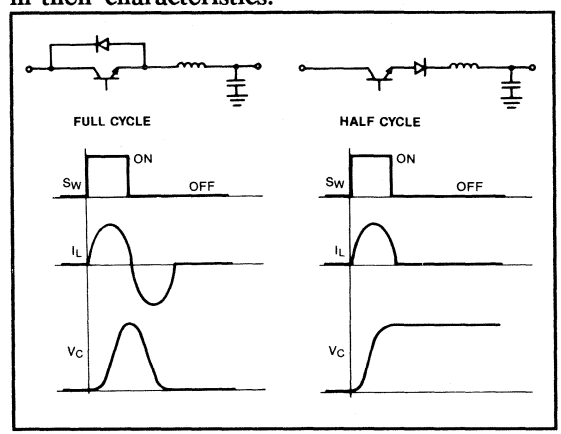


Fig. 16 - Half and Full Cycle Waveforms with Unloaded Resonant Switch

While half cycle operation may be easier to implement, the pulse repetition rate is a direct function of the loading and, when coupled with input voltage variations, can result in huge swings in switching frequency. A full cycle configuration usually requires a diode in series with the switch as well as the antiparallel diode in order to prevent any reverse conduction through the slow switch body diode. Additionally, with current flowing in both directions, conduction losses tend to be greater. The advantage is that by returning surplus energy to the source, switching frequency is independent of load.

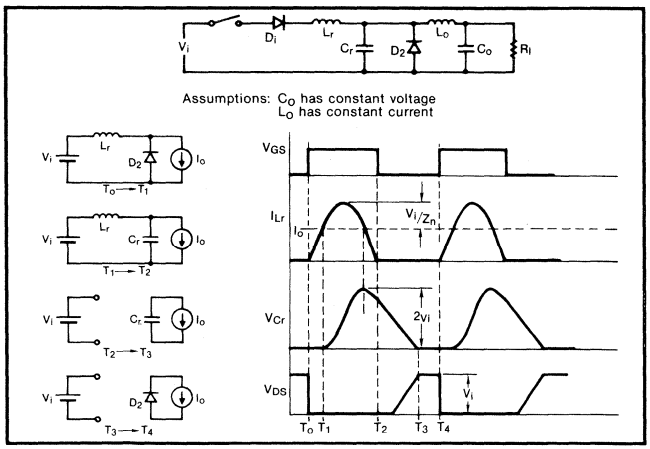


Fig. 17 - Quasi-Resonant Switching Operation

Resonant Converter Basic Operation

After having defined the various classifications of resonant mode topologies, we will now describe the detailed operation of one such circuit. This material, derived from work done by Dr. Fred Lee and the Power Electronics Group at V.P.I. is illustrated here in Figure 17. The circuit is a single-ended, buck-derived, parallel-loaded, half-cycle, zero-current switching, quasi-resonant converter. We will later extrapolate this operation to other circuit topologies.

A resonant converter, like all switching regulators, requires an output filter to smooth the power delivered to the load. This output filter must have a break frequency less than one fifth the *lowest* switching frequency. Therefore we assume the current through Lo and the voltage across Co are both essentially constant at the switching frequency. The waveforms on the right of Figure 17 define the current and voltages during the four time increments, T_0 to T_4, which make up the total switching period. The portions of the circuit which are active during each time increment are shown on the left.

At time T_0, the output current is all flowing through D_2 and with the activation of the switch, inductor current, I_{Lr}, starts to ramp up linearly with constant V_i across L_r.

At time T_1, the output current transfers to L_r and the inductor current continues to rise in a sine wave to a peak defined by V_i and the resonant tank impedance. At the same time, C_r starts to charge with a cosine function to a value of $2V_i$. When the inductor current falls below I_o, C_r begins to contribute to I_o and its voltage starts to fall.

At time T_2, the current through L_r reaches zero and I_o can come only from C_r. With a constant I_o, the voltage on C_r falls linearly and when it reaches V_i, diode D_1 lets the voltage transfer to the open switch. Note that the switch can open at any time between this point and T_2.

At time T_3, the resonant tank is dry and I_o flows completely from D_2 until the next switch activation.

The same process can be used to analyze other circuit topologies remembering that a square wave circuit can be converted to a resonant circuit by merely adding a resonant switch. Figure 18 shows four such configurations.

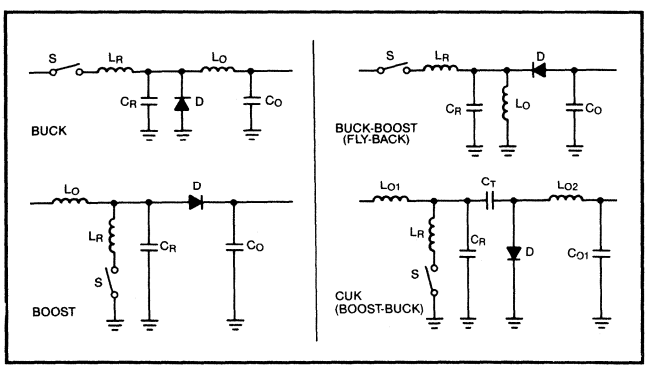


Fig. 18 - Parallel-Loaded Resonant Converter Versions of Square-Wave Power Conversion Topologies

Transformer Coupling

The introduction of a transformer into the power path does not change anything from a topology standpoint but it adds some interesting and useful features. Figure 19 shows some possible extensions of the simple buck regulator discussed above. In Fig. 19A, the resonant circuit is in the primary and the transformer provides merely an impedance match to a parallel load. This approach has the advantage that the transformer passes only load current and therefore current sensing is easily done in the primary side. Fig. 19B moves the resonating capacitor to the secondary with two benefits: the leakage inductance of the transformer is no longer

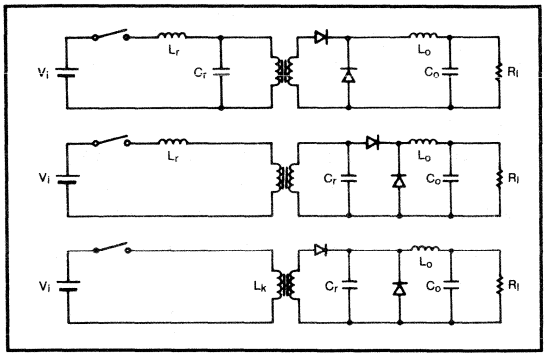


Fig. 19 - Transformer Coupling

a parasitic but adds directly to the resonating inductance, and with sine wave current flow, secondary diode switching is soft with less tendency for transient ringing.

The Vinciarelli Circuit of Fig. 19C moves the capacitor further to the other side of the rectifying diode and while transformer reset must now be accomplished by some other means, the lack of reverse current frees the primary side of the need for high-voltage, high-speed blocking diodes. In addition, the transformer now sees only the square voltage waveform from the primary switch and thus has to support less volt -seconds. The practical implementation of this circuit also builds enough leakage inductance into the transformer such that it becomes the total resonating inductance, eliminating a separate component.

Alternate Resonant Operating Modes

Without going into the same depth that was used above in the description of the single-ended, buck-derived circuit, we will now examine and compare the whole range of operating modes for both series and parallel resonant converters. For this comparison, we will use a classic half-bridge topology as shown in Figures 20 and 21. These circuits have been normalized with all waveforms drawn to the same scale and the following definitions apply:

V_s: The switched input voltage into the resonant circuit
I_r: The resonant current in the inductor
V_r: The voltage on the resonating capacitor
V_d: The voltage at the transformer secondary
I_d: The current through each leg of the output diodes

In all cases, Vo is assumed constant and the primary diodes defining full-cycle or half-cycle operation are not shown.

The Series Resonant Converter

Figure 20A; Variable-frequency, Half-cycle, Discontinuous Mode: In this mode, current is allowed to flow in only one direction through each switch as can be seen from the Ir waveform. This power stage has a constant power output characteristic where the output power is given by $1/2\ C_r\ V_s^2\ F_s$. An increase in either the input voltage or the switching frequency will proportionately increase the power delivered to the load, irrespective of the load impedance. In the ideal case, the output voltage can rise almost infinitely and some method must be used to limit it under no load conditions. The slope of the output curve changes with the load impedance which affects the small signal gain of the power stage and makes it more difficult to include inside a feedback loop. The switching frequency is also dependent on both the input voltage and the load current and so may have a very wide switching frequency range. This circuit and its derivatives are among the most simple and least costly to produce converter circuits available but the resultant dynamic performance has been traded for this low cost.

Figure 20B; Variable-frequency, Full-cycle, Discontinuous Mode: As the I_r waveform shows, in this mode the switches carry current in both directions which gives the circuit a constant current output characteristic. The low frequency model is simply a voltage controlled current source feeding the output capacitor. The switching frequency variation in this converter mode is directly related to the output current. If a wide output current range is needed, the switching frequency range will also be wide. This will restrict the control loop bandwidth when used for a constant voltage output. This circuit is most commonly used for high voltage outputs because peak voltage on the secondary is simply equal to the output voltage. An interesting aspect of this converter is the way the resonant current waveform changes slope abruptly on each half cycle as the current crosses through zero. The output

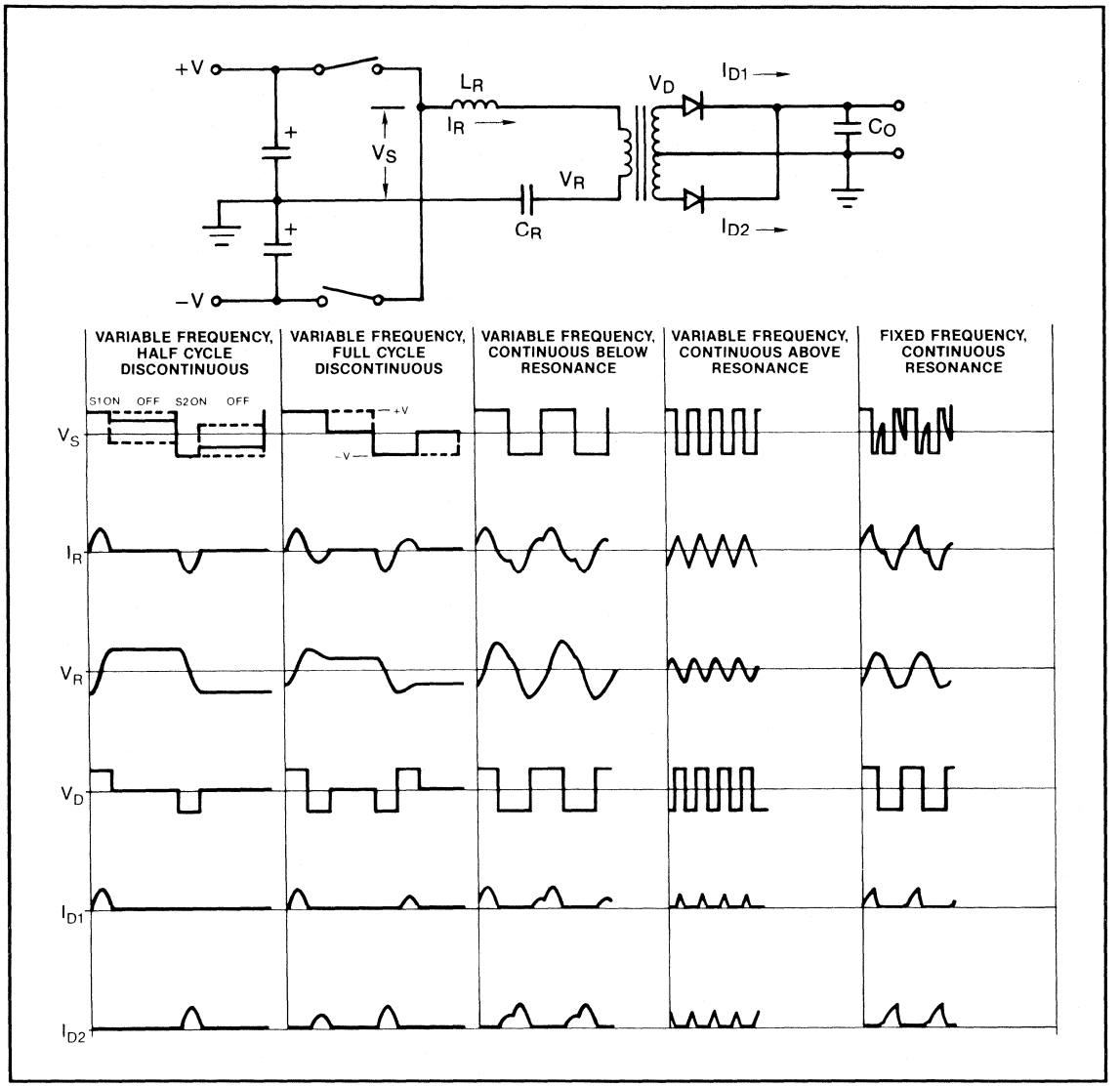


Fig. 20 - Series-Loaded, Half-Bridge Converter

voltage is reflected into the resonant circuit through the diode bridge and when the current reverses, the reflected output voltage changes sign. This lowers the effective voltage across the resonant circuit and hence the resonant current is lower. Note that although the current through the switches and diodes is sinusoidal, the voltage waveforms are square. This behavior is characteristic of all series resonant converters.

Figure 20C; Variable-frequency, Continuous, Below Resonance: Notice that in this mode the resonant voltage and current are both partial sine waves. Because the current in the inductor is continuous, each switch transition must force commutate the antiparallel diode of the opposite switch. Also, as noted before, the diode voltage is still square although the current is sinusoidal. Phase shift is occurring between the switch voltage and the resonant current. The transfer function of the power stage is nonlin-

ear since its gain is dependent on the impedance slope of the resonant circuit. This makes this circuit somewhat difficult to stabilize but reasonably wide control bandwidths can be maintained as long as the output load is able to keep the circuit in continuous resonance. If the load goes open the switching frequency will go to zero. The small signal analysis of this mode is given in Ref. [3] for both above and below resonance.

Figure 20D; Variable-frequency, Continuous, Above Resonance: As was noted in the preceding paragraph, below resonance each switch must force the opposite antiparallel diode off and carry the current which was flowing through it. Above resonance the switch turns on naturally at zero current because its antiparallel diode conducts first, but the switch must turn off with current through it. The antiparallel diode of the opposite switch will conduct immediately and is then naturally commutated by the resonant circuit in its turn. Above resonance, the resonant current resembles a sawtooth wave more than a sinusoid even though it is made up of sinusoidal sections. The capacitor voltage is the integral of the current and it more closely resembles a sine wave. The frequency range of this mode of operation is generally low and it operates on the slope of the resonant circuit impedance curve the same way it does below resonance. A required limit on minimum switching frequency allows the control loop bandwidth to be wide although the transfer function of the circuit in this mode is still very nonlinear. Also note that with a large load current variation, the switching frequency range will be wide and if the load goes to an open circuit the switching frequency will go to infinity.

Figure 20E; Fixed-frequency, Continuous, At Resonance: The waveforms in this mode are similar to the ones of variable frequency continuous resonance mode above resonance. The switch voltage is different because the resonant circuit begins to ring after the current goes to zero. This shows up as the funny looking blip in V_s which is the start of ringing. Obviously, the switching frequency does not vary with load or input voltage but the pulse width may vary over the whole range. The operation of the circuit is similar to an amplitude modulation system. The square wave coming from the switches has a fundamental frequency and many harmonics. A change to the pulse width produces a similar change in the amplitude of the fundamental frequency component. The action of the resonant circuit eliminates the harmonics and passes a sinusoidal current at the fundamental frequency to the output where it is rectified and filtered.

The Parallel Resonant Converter

Figure 21A; Variable-frequency, Half-cycle, Discontinuous: This mode again blocks reverse current flow through the switches which is readily seen in the I_r waveform. Like the series resonant converter in this mode, the parallel resonant converter also has a constant power output characteristic which is given by the same equation: $P_o = 1/2\ C_r\ V_s^2\ F_s$. An increase in the switching frequency will produce a similar change in the power delivered to the load irrespective of the load impedance. In the ideal case the output current can become quite high under a short circuit and some means must be used to provide a maximum current limit. The constant power output characteristic makes the small signal gain of the stage dependent on both the output load and the input voltage, so it is more difficult to stabilize a feedback loop around a converter operating in this mode. The switching frequency dependency on both the input voltage and the load current results in a very wide switching frequency range if there is a large variation in the load current. A circuit with a 1 MHz resonant tank might be operating near 50 kHz at high line and light load. As was the case with series resonance, this circuit and its derivatives trade performance for simplicity and low cost.

Figure 21B; Variable-frequency, Full-cycle, Discontinuous: Full-cycle conduction provides for current flow in both directions through the switches. The resonant current in the inductor has a DC component on each half of the switching cycle which is equal to the output inductor current. This is also responsible for the small time delay on the leading edge of the resonant voltage waveform, V_r. This voltage is clamped at zero as long as the output diodes

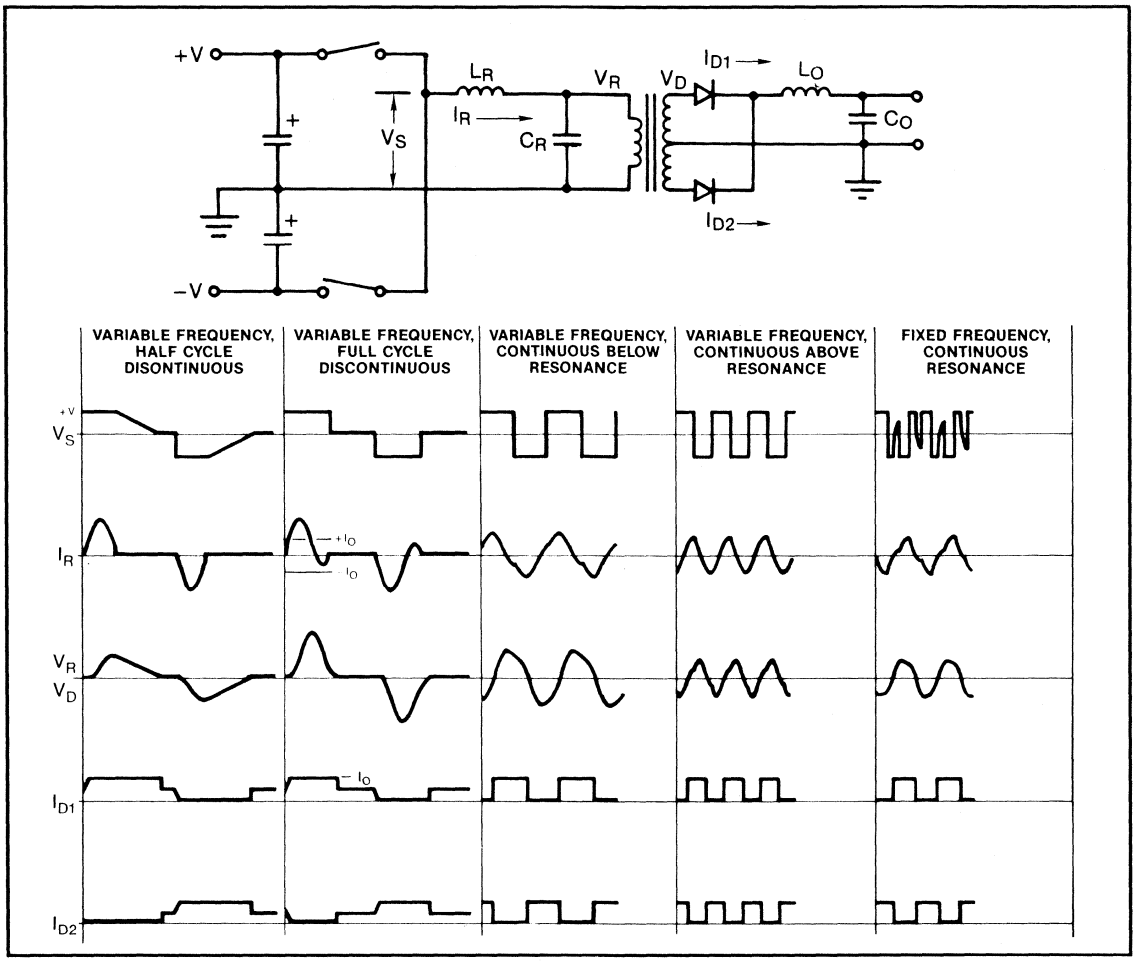


Fig. 21 - Parallel-Loaded Half-Bridge Converter

are all conducting. This is the case at the beginning of a cycle and it continues until the resonant inductor current, I_r, is equal to the output inductor current. The resonating inductor current does not have to reverse as shown here but if not, the switches must be force commutated off and the switch dissipation and EMI output go up considerably. If I_r is as shown in the figure, the switches will commutate naturally. Both switch transitions occur at zero current and it is thus true zero current switching. This mode of operation has an extremely linear transfer function and a low output impedance which makes it an excellent voltage source. Its dynamic characteristics are very similar to those of a standard PWM buck converter. It is easy to close a voltage loop around this circuit and achieve excellent dynamic performance and wide loop bandwidth. The switching frequency is not dependent on the load current so the switching frequency range is reasonably small. This circuit is well suited to a wide variety of applications.

Figure 21C; Variable-frequency, Continuous, Below Resonance: In this mode, when each switch turns on it must force commutate the current flowing in the opposite antiparallel diode and thus has some switching loss although the switches are commutated off naturally. The output diodes see a square wave of current but a sinusoidal voltage, as expected from a single tuned converter. The transfer

function for this mode of operation is nonlinear because it is operating on the slope of the resonant circuit impedance curve and its small signal properties are similar to those of the series resonant converter. The overall switching frequency change is reasonably small as long as the circuit is operating in continuous resonance so the bandwidths may be reasonable and the circuit will have good dynamic performance. If the load current goes to zero, the current in the output inductor will become discontinuous and this will force the switching frequency toward zero.

Figure 21D; Variable-frequency, Continuous, Above Resonance: Above resonance the switches are force commutated off but turn on naturally at zero current because their antiparallel diodes conduct first. Note that this circuit has a phase change from that observed when operating below resonance. In this mode also, the switching frequency variation will be small unless the load becomes an open circuit, in which case the switching frequency will go to infinity. The known minimum switching frequency allows a wide control loop bandwidth to be achieved, however, the nonlinear transfer function makes it more difficult to stabilize a feedback loop.

Figure 21E; Fixed-frequency, Continuous, At Resonance: These waveforms are very similar to the continuous resonance mode above resonance. One of the switch transitions again requires that the switch be force commutated. The sawtooth section in V_s is caused by the start of ringing when the switch current goes to zero. The switching frequency of the circuit is obviously fixed but the pulse width may cover the entire range. The operating principle of this circuit is similar to amplitude modulation. The voltage waveform from the switches contains a fundamental and many harmonics. The resonant circuit eliminates the harmonics and allows only the fundamental to reach the output circuit. As the pulse width of the switches

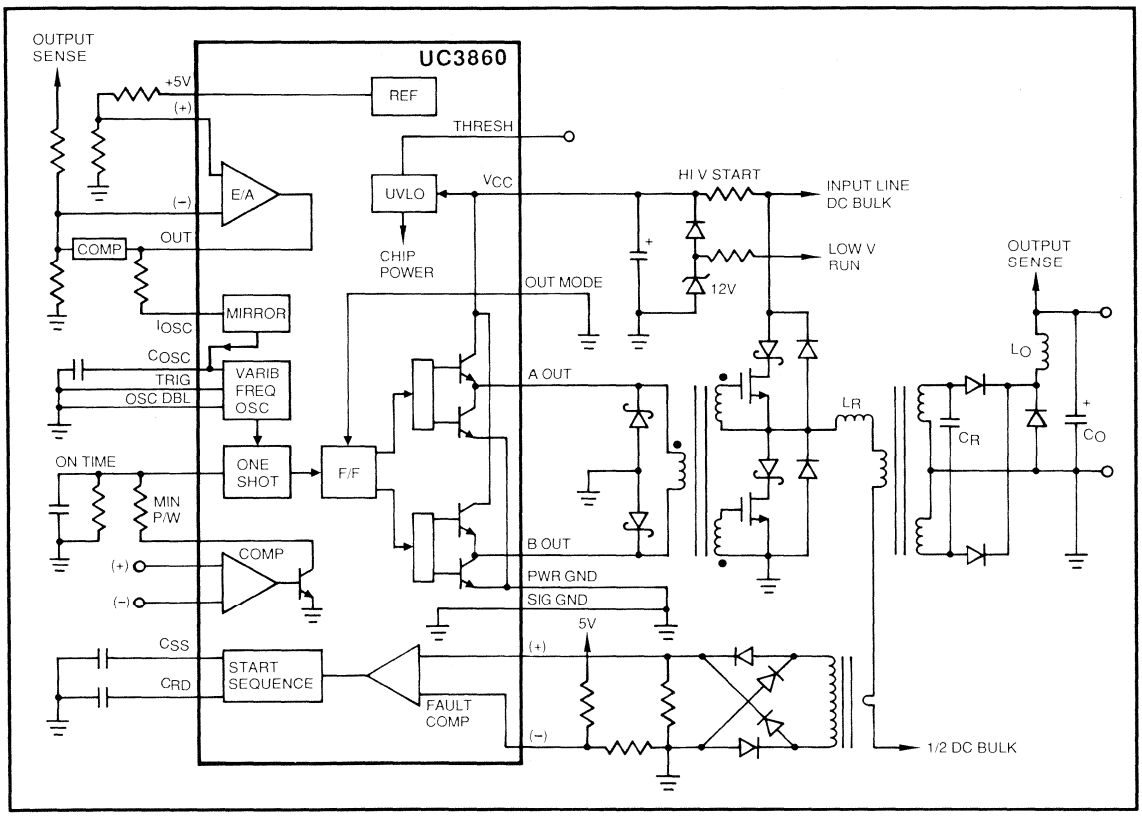


Fig. 22 - Half-Bridge Off-Line Quasi-Resonant Converter

changes, the amplitude of the fundamental component of the voltage will change correspondingly. This varies the amplitude of the fundamental voltage across the resonating capacitor and thus the output. The rectified sine waves are then averaged by the output filter.

A Practical Resonant Converter Example

To show a more complete power supply architecture, the schematic of Figure 22 combines a half-bridge resonant power stage with a new IC control chip designed by Unitrode for use in resonant mode power converters of many different topologies. This application features the parallel-loaded, half-bridge topology in a variable frequency mode. It includes full current limiting, minimum frequency limiting, and over voltage control for zero loaded conditions, as well as many other protection and programming functions needed for practical power supply operation. With the introduction of control circuits like the UC3860, the use of resonant mode power conversion techniques can be expected to rapidly advance and become the technique of choice in the next few years.

References

[1] R.P. Severns and G. E. Bloom, "Modern DC-to-DC Switchmode Power Converter Circuits," *Van Nostrand Reinhold Co., New York,* 1985.

[2] P. C. Todd and R. W. Lutz, "Practical Resonant Power Converters - Theory and Application," *Powertechnics Magazine;* April, May and June, 1986.

[3] V. Vorperian and S. Cuk, "Small Signal Analysis of Resonant Converters," *Proceedings of the IEEE Power Electronics Specialists Conference,* 1983.

[4] Liu, Oruganti, and Lee, "Resonant Switches - Topologies and Characteristics", *Proceedings of the IEEE Power Electronics Specialists Conference,* 1985.

[5] W. F. Santelmann, Jr., "Designing Ultra-Efficient High Voltage Supplies Using a High Frequency Resonant Flyback Technique," *Proceedings of Powercon 9,* Paper G-2, 1982.

[6] F. Lhermite and D. Catala, "Control of a Single Ended Off-Line Quasi-Resonant Power Supply," *Proceedings of PCI,* 1987.

1 MHz 150 W Resonant Converter Design Review

by Bill Andreycak

TOPIC 2

1 MHz 150W Resonant Converter Design Review

Bill Andreycak

Abstract:

This paper is intended to explore in significant detail the intricacies of the quasi-resonant half bridge topology. Voltage and current waveforms and transferred charge and energy will be analyzed as functions of time and input/output conditions. Specific and generalized design equations are given, which are also applicable to other topologies by those skilled in modern power supply design.

Introduction:

The pioneers of resonant mode power conversion have generated a tremendous amount of interest in this new and emerging technology and approach to power conversion. Expectations of lossless switching and multi-megahertz operation are rapidly approaching realization. Given this recent stimulus, a new control IC, the UC3860, has been introduced for controlling many of the various resonant and quasi-resonant design approaches.

Despite the differences among the numerous resonant and quasi-resonant switching topologies, all have one common denominator -- the need for a high speed, complete and versatile resonant mode control IC. The ideal candidate would incorporate modular functions or building blocks that could be easily configured by the user to control various circuit topologies and implementations.

This paper will show one application of this resonant control IC in a typical power supply design example. Described in the text is a 150 watt off-line converter switching at a maximum frequency of 1 megaHertz. This results in an effective 500 kiloHertz utilization of the main transformer. Delivering 15 volts at 10 amperes of load current, it operates from a 110/220 AC input, or from a 220 to 370 V dc bus at high efficiency.

Design Specifications:

An off-line 150 watt, single output design has been selected as a typical application for the purposes of this paper. Several items common to most designs will not be highlighted, for example, primary to secondary isolation and input filter calculations. However, this discussion will concentrate on relevant calculations and new material regarding the quasi-resonant converter.

Input Voltage:
(110 VAC) : 85 -- 132 VAC
(220 VAC) : 170 -- 265 VAC
(DC Input) : 220 -- 375 VDC

AC Line Frequency: 50 Hz min

Output Voltage: 15 VDC

Output Current: 2.5 -- 10 Amps

Line Regulation: 15 mV

Load Regulation: 15 mV

Output Ripple: 100 mV p-p, dc-20 MHz
Efficiency: 85 % at full load

Quasi-resonant Circuit Operation

The quasi-resonant Buck regulator circuit shown in Fig. 1 is applicable to high frequency power conversion systems and will be described in detail. Initial conditions are given with the switch Q open, and no current flowing from the input source V. The resonant current I_r is zero, and no voltage is across either of the resonant components L_r or C_r. There is an output current I_{out} and voltage V_{out} delivered entirely by the output filter components L_o, C_o and D_o. For the purposes of this model, assume that each component is ideal.

Switch Q is closed at time t_0 applying voltage V_{IN} across the circuit input. The input current I_{in} begins at zero and rises linearly at the rate of V_{IN}/L_r until it reaches output current I_{out}.

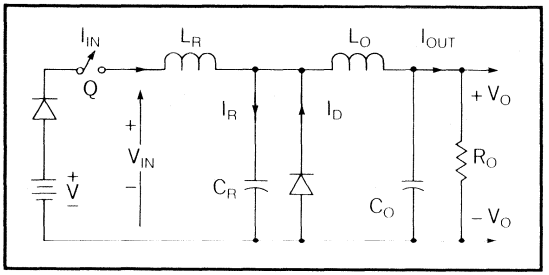


Fig. 1 - Quasi-Resonant Buck Regulator

Simultaneously, the output diode current I_d which began at I_{out} linearly decreases to zero. At this point, the input power source is supplying the full output current I_{out}. This occurs at time t_1 which will vary linearly with I_{out} and V_{IN}. During the interval between t_0 and t_1, no resonant current I_r flows in capacitor C_r.

Beginning at t_1 the resonant circuit current component I_r sinusoidally flows through C_r. This adds to the output current, making the input current the summation of both. Peak input current occurs at $t_1 + \pi/(2\omega)$. It later intersects the I_{out} level at t_2, corresponding to $t_1 + \pi/\omega$.

The sinusoidal input current continues until t_3 where it reaches zero. Here, the switch is opened and turn-off is initiated at *zero current* which facilitates lossless switching. Since t_1 varies with I_{out} and V_{IN}, the zero current switch point t_3 varies also with these changing parameters.

A zero current detection circuit can be used to facilitate turn-off at precisely zero current. Another technique utilizes a fixed *on* time at the primary switches. This time constant is set above the maximum required *on* time of the resonant network over all line and load combinations. While this technique is easier to implement, it may compromise overall design at the maximum conversion frequency. The inability to switch consecutively at maximum rate hurts transformer turns ratio optimization. Higher currents will result due to the lower turns ratio, degrading overall efficiency at all frequencies.

During the interval between t_3 and t_4, C_r discharges, providing a constant current I_{out} to the load. The capacitor voltage decreases linearly, reaching zero at t_4.

The output filter section releases its stored energy between t_4 and t_5. The conversion period ends at t_5, which corresponds to the beginning of the next cycle, t_0. A detailed analysis of the voltages and currents during each interval is provided in the Appendix.

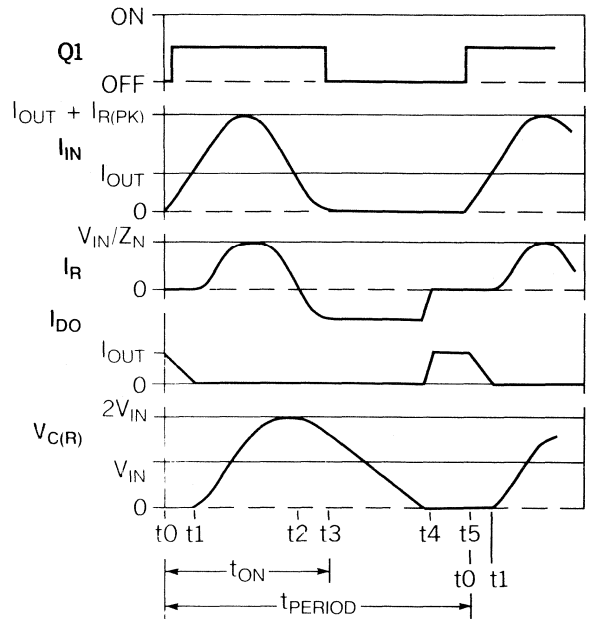


Fig. 2 - Quasi-Resonant Waveforms

Quasi-Resonant Half Bridge -- Topology Fundamentals and Overview

The general circuit diagram for a quasi-resonant half bridge converter using secondary side resonance is shown in Fig. 3. The resonant half bridge portion and its associated waveforms are shown in Figs. 4 and 5.

Transistors Q_1 and Q_2 are alternately driven from the control circuitry at a repetition rate, or frequency determined by the error voltage.

Q_1 turns on, connecting the transformer primary across capacitor C_1 with voltage $V_{IN}/2$. This rectangular voltage waveform is divided by the turns ratio N (N_{pri}/N_{sec}) and coupled to the secondary side(s) of the transformer. Diode D_1 is forward biased, and secondary current I_{sec} flows through L_{r1} and D_1. This can be expressed as two individual components, the "constant" output current I_{out} and the sinusoidal current I_r through C_r. During this interval, D2 is reversed biased and is essentially out of the picture.

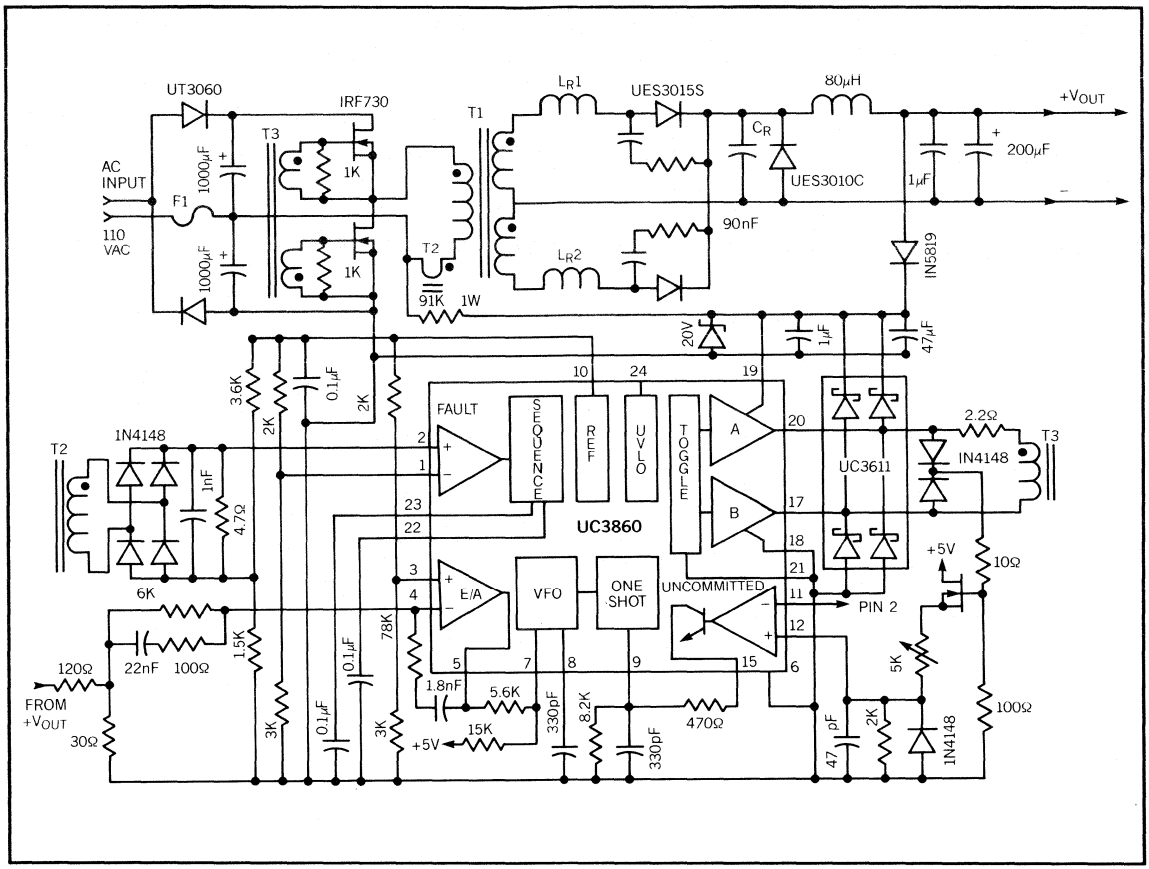


Fig. 3 - 150 Watt Off-Line Quasi-Resonant Half Bridge

The secondary current starts at zero at time t_0 and ramps up linearly, reaching I_{out} at t_1. I_{sec} then becomes sinusoidal, peaks at $I_{sec(peak)}$, and intersects the output current again at t_2. At t_3, zero current is reached sinusoidally and Q_1 is turned off.

Peak voltage across C_r occurs at t_2 and diminishes during the remainder of the interval ending at t_5. When the voltage across C_r reaches zero, all of its stored charge has been transferred to the output load, thus completing the conversion cycle. This process is repeated for transistor Q_2, resulting in similar operation.

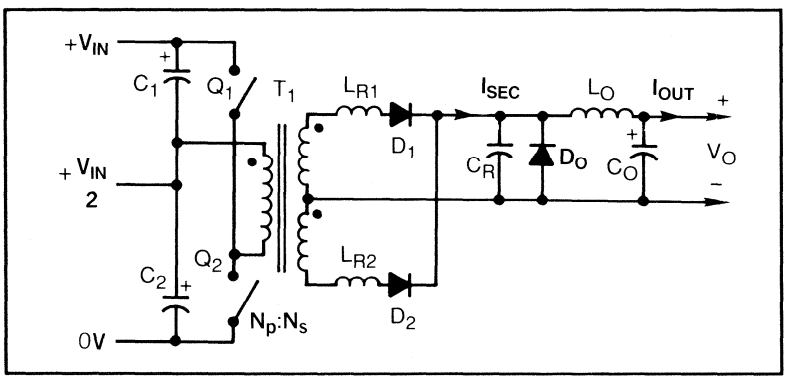


Fig. 4 - Quasi-Resonant Half Bridge

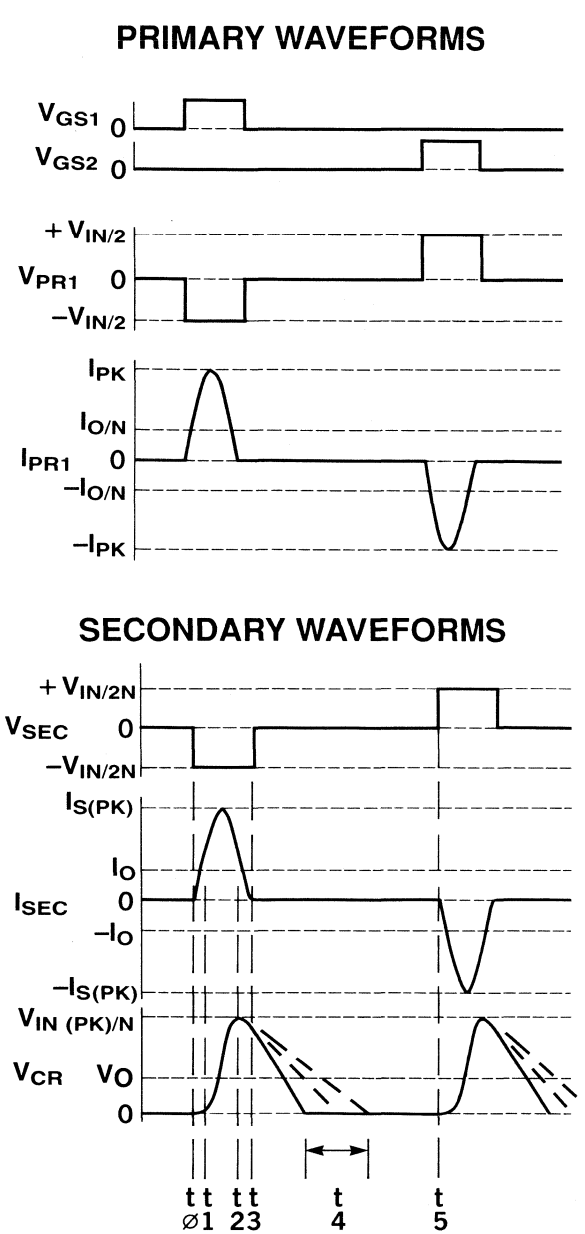


Fig. 5 - Primary and Secondary Waveforms

Half Bridge Advantages and Alternatives

The thrust towards resonant mode power supply designs has been fueled by the demands for higher power densities and high overall efficiency. Although several basic topologies deserve consideration in this off-line application, the Half Bridge configuration offers many key advantages.

Unlike the single-ended forward converters, the half bridge provides bidirectional utilization of the transformer. This eliminates the need to incorporate dissipative or complex flux reset mechanisms for the main transformer. Also, the primary switched voltage is one-half that of its single ended or full-bridge counterpart, halving the transistor voltage rating requirements.

In addition, the reduced voltage significantly reduces turn-on losses. Bear in mind that zero current switching minimizes *only* the turn-off losses. During turn-on, however, the current rises linearly before resonance commences, and the half bridge has the lowest turn-on losses of all configurations.

Transformer size is smaller for the half bridge because the forward converter "wastes" half the period with no power transfer while the core is being reset. Also, all windings have half the number of turns compared to a forward converter approach. This could significantly lower the leakage inductance in certain designs where low voltage, high current designs stand to benefit the most.

Half Wave Resonance: The half-wave resonant mode of operation facilitates a unidirectional current flow from the primary to the secondary. The major advantages of this can be seen near the primary switches. When a reverse current flows through the Mosfet, its parasitic drain-body diode conducts, exhibiting slow reverse recovery characteristics. To prevent this, the reverse current is generally directed to an external fast recovery diode that shunts the Mosfet. A Schottky diode must be added in series with the Mosfet to guarantee that the external diode will conduct. This "elaborate" network is not lossless, and can significantly impact the power supply overall efficiency.

Secondary side half wave resonance eliminates the need for these components. Reverse current flow is restricted on the secondary side of the transformer by the series rectifiers. Serving a dual purpose, these diodes isolate the resonant tank from the primary in addition to rectifying the secondary waveform.

Full wave designs return excess tank energy back to the primary, and require bidirectional

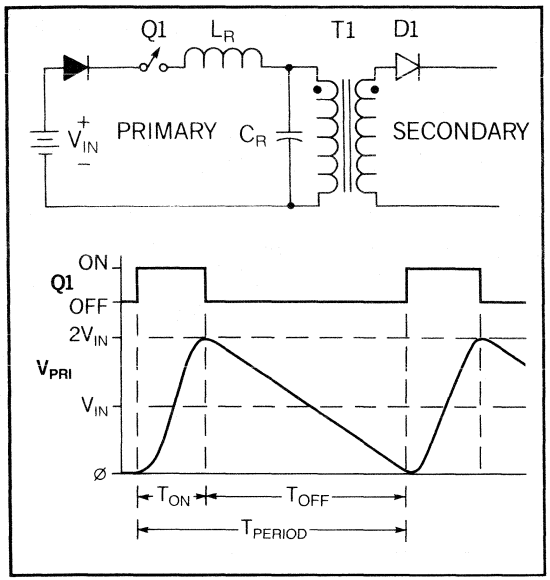


Fig. 6 - Primary Side Half Wave Resonance

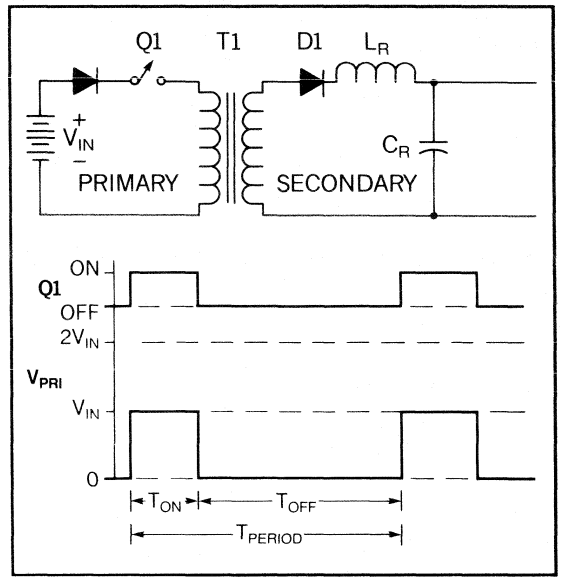


Fig. 7 - Secondary Side Half Wave Resonance

switches on the primary. One merit, however, is that the switching frequency range is fairly narrow over various line and load combinations. On the other hand, the half wave resonant approach must span a fairly wide range of switching frequencies to maintain regulation for the same input and output variations, since all resonant tank energy must be delivered to the output.

Secondary Side Resonance: Secondary side resonance helps minimize transformer size. With the resonant capacitor located on the transformer secondary side, the volt-second product depends only on the input voltage and transistor *on* time. During the remainder of the period, or *off* time, the transformer is not supporting the resonant capacitor discharge. Lower core losses are attained with this configuration, and are easier to analyze. The waveform is rectangular and is a function of input voltage, *on* time and switching frequency.

Resonant Control Circuit

Refer to the simplified block diagram and waveforms of Fig. 8.

Error amplifier: The error amplifier is used to generate an output voltage proportional to the error between the amplifier inputs. A precision reference voltage is at the noninverting input, while the power supply output voltage is applied to the inverting input. The difference between the two is amplified and will respond to millivolt changes in power supply output voltage, providing tight regulation. The error amplifier output is high when the supply output voltage falls below its setpoint, and a low amplifier output indicates the output voltage is higher than ideal. This variable error amplifier output voltage indicates the need for correction to maintain regulation.

Variable frequency oscillator: This device converts a variable input voltage to a variable frequency output pulse train. Increasing input voltage yields an increase in the frequency of the output pulses. Regulation of the output voltage is thus obtained over various line and load combinations by varying the switching (conversion) frequency. The VFO is driven by the error amplifier output voltage and is used to trigger the one-shot pulse generator.

One shot pulse generator: This module generates an accurate pulse width, or duration corresponding to the *on* time required for the resonant tank circuit switches. In fixed *on* time quasi-resonant applications this time constant is set slightly longer than one-half of the full resonant period. Another approach utilizes zero current switching (ZCS) which turns off the switches at zero current. In this application, the one shot is programmed for the maximum circuit on-time and modulated to facilitate ZCS.

Toggle flip flop and gating circuitry: Alternating outputs for "bridge" applications require a toggle flip-flop to divide the VFO frequency by two. This provides out-of-phase drive signals to each of the resonant switches with the proper on-time. In single ended applications like the Buck, Forward and Fly-back topologies, a toggle function is not used.

High power Mosfet drivers: High peak gate currents are required to deliver sharp Mosfet turn-on and turn-off transitions. The driver accepts low power (TTL) logic inputs and delivers high power (1 to 3 amp peak) Mosfet gate drive compatible outputs.

Zero current switching circuitry: Primary current is monitored and used to turn off the one shot–hence the outputs–when zero current is crossed. This minimizes the switching losses in the primary switches.

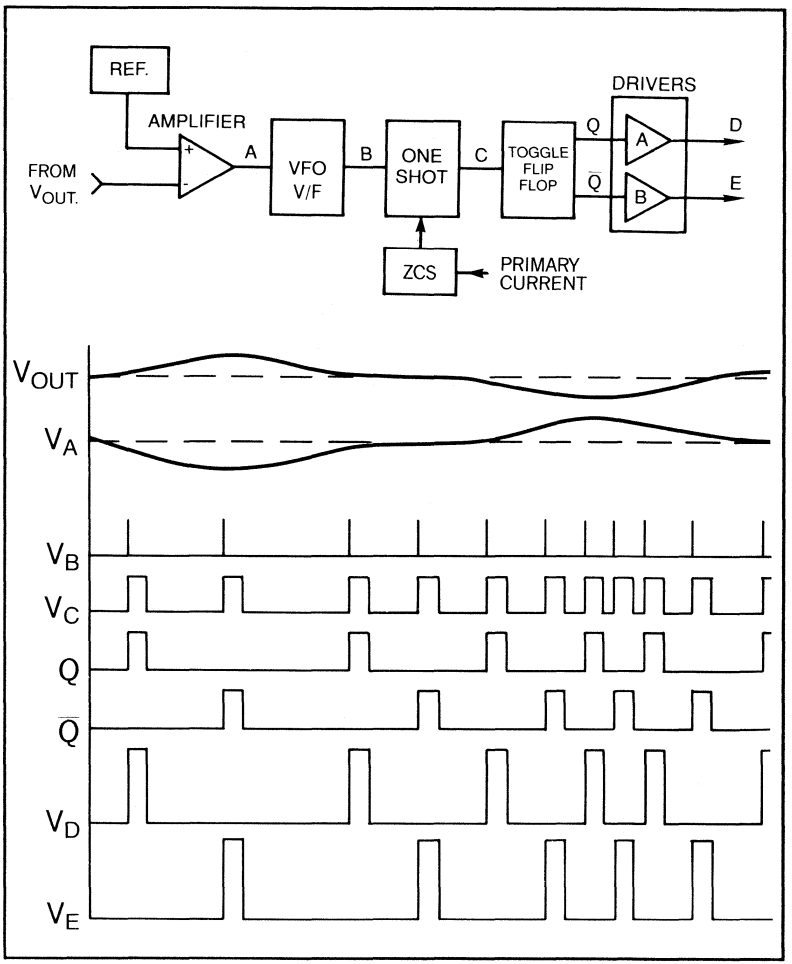


Fig. 8 - Control Circuit Fundamentals

Quasi-Resonant Circuit Limitations

One obvious circuit constraint is that the peak resonant current component I_r *must* be greater than I_{out}. Otherwise, zero current will not be reached as shown in the figure below. This relationship specifies the limits of V_{IN} and I_{out} of the resonant tank as a function of the L_T–C_T resonant tank characteristic impedance, Z_T.

Increasing the resonant current component far above I_{out} max is one solution, but an inefficient one. The primary switch losses vary with primary current squared, and techniques to minimize this current are required.

The ideal ratio of the output current I_{out} to the minimum resonant peak current $I_{r(pk)}$ min is unity. This insures resonance at all loads while preventing excessively high peak resonant tank currents and losses. The resonant component initial tolerances and temperature variations need to be analyzed and accommodated by adjusting the ratio of $I_{out\ max}$ to $I_{r(pk)}$. A twenty-five percent safety margin is used in this

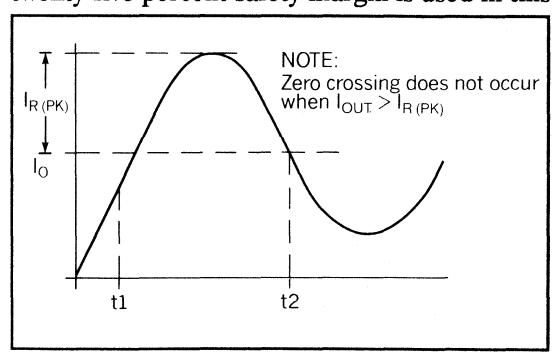


Fig. 9 - Input Current - No Zero Crossing

design corresponding to a ratio of 0.75:1.

The resonant L–C elements are now defined *uniquely* by the power supply output voltage and load current for a specific resonant tank frequency and current ratio $I_{out\ max}$ to $I_{r(pk)}$.

$$I_{r(min)} = \frac{V_{IN\ min}}{Z_r}, \text{ or } Z_r \leq \frac{V_{IN\ min}}{I_{out\ max}}$$

Substituting $Z_r = \omega_r L_r$ and $V_{IN} = V_{sec}$ for secondary resonance, the resonant inductor L_r and C_r are defined by :

1. $L_r = \frac{0.75 V_{sec\ min}}{\omega I_{out\ max}} \Rightarrow \frac{0.12 V_{sec\ min}}{f_{res} I_{out\ max}}$

2. $C_r = 1/(\omega^2 L_r) \Rightarrow .025/(f_{res}^2 L_r)$

3. Verify that $Z_r < V_{out}/I_{out\ max}$. If not, the ratio of the resonant to output current may need to be altered.

Transformer Turns Ratio

The transformer turns ratio is derived by equating the circuit input and output volt-second products. A topology coefficient K_t is introduced which specifies the ratio of the maximum switching frequency to that of the resonant tank frequency. It is somewhat analagous to maximum duty cycle in a square wave converter. Allowing K_t to approach unity in a resonant converter maximizes the turns ratio, thus lowering the primary current.

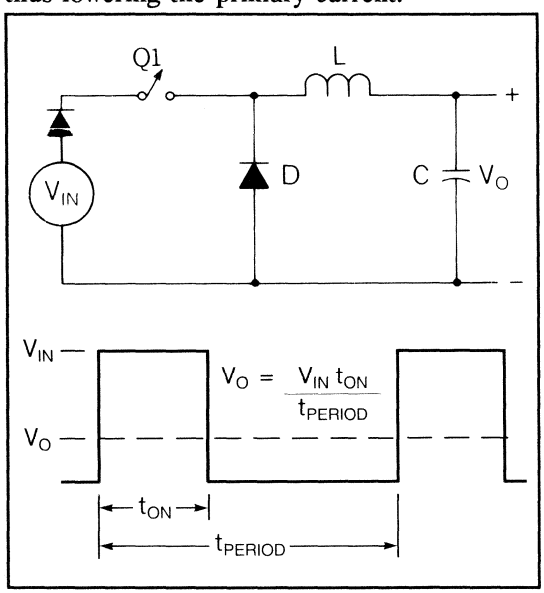


Fig. 10 & 11 - Square Wave Buck Regulator

As switching frequencies approach 1 MHz, diode recovery times and Mosfet rise and fall times prevent the topology coefficient from reaching unity. In addition, the resonant capacitor requires time to discharge into the output load. A K_t value of 0.8 is suggested by several of the references listed in the Appendix. The turns ratio can now be calculated from the volt second relationship described previously.

The transformer turns ratio N =

$$V_o = \frac{V_{IN}\ K_t}{2\ N}, \qquad N = \frac{K_t\ V_{IN\ min}}{2\ V_o}$$

Accounting for the voltage drops,both the primary and secondary:

$$N = \frac{K_t}{2} \cdot \frac{V_{IN\ min} - V_{loss\ pri}}{V_{o\ min} + V_{diode} + V_{loss\ sec}}$$

The actual transformer secondary voltage has now been defined by V_{input} and the turns ratio N. The conversion period or frequency can be extracted from the energy transfer equations in the Appendix by substituting V_{sec} for V_{IN} in the given equations.

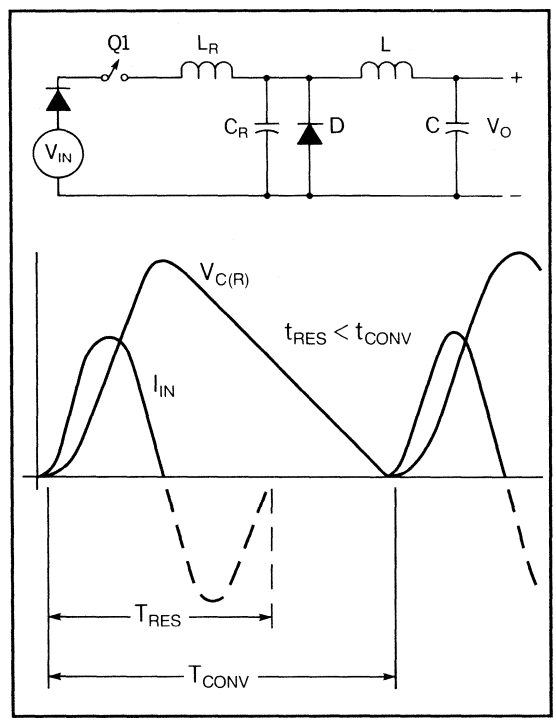


Fig. 12 & 13 - Resonant Mode Buck Regulator

Conversion Frequency

As the output load current I_{out} and input voltage V_{IN} vary, the control circuit adjusts the conversion frequency to maintain a constant output voltage, V_{out}. The maximum conversion frequency will occur at low line and full load, where by design, the frequency equals the resonant tank frequency divided by K_t, the topology coefficient.

$$K_t = \frac{f_{conv\ max}}{f_{res}}; \qquad f_{conv\ max} = K_t f_{res}$$

Minimum frequency will occur at high line $V_{IN\ max}$ and light load $I_{out\ min}$ which can be estimated by the following relationship:

$$1/f_{conv\ min} = T_{conv\ max} = \frac{V_{IN\ min}\ Q}{2NV_oI_{o\ min}}$$

where

$$Q = \left[\frac{2NL_rI_{o\ min}^2}{V_{IN\ min}} + \frac{V_{IN\ min}\ C_r}{N} + \frac{\pi I_{o\ min}}{2f_{res}}\right]$$

Quasi-Resonant Circuit Relationships

SUMMARY OF APPENDIX 1

Timing relationships:

t_o = time when the cycle is initiated
$t_1 = L_r \cdot I_{out}/V_{sec}$
$dt_{21} = \pi/\omega_{res}$
$t_2 = t_1 + dt_{21}$
$dt_{32} = 1/\omega_{res} \cdot \sin^{-1}(I_{out}\ Z_r/V_{sec})$
$t_3 = t_2 + dt_{32}$
$dt_{43} = v_{Cr(t3)}\ C_r/I_{out}$
$t_4 = t_3 + dt_{43}$
$t_5 = [V_{sec}Q_t/(V_{out}I_{out})]$ (approx)

The charge transferred per cycle, Q_t, is approximated by :

$$Q_t = L_rI_{out}^2/V_{sec} + 2V_{sec}Cr + \pi I_{out}/\omega$$

Design Procedure and Calculations

The design specifications listed on page 1 will be used for this 150 watt application. A maximum switching frequency of 1 MHz has been selected as a good compromise between the attempts to obtain high power density (small size) and high overall efficiency.

1. Select the maximum switching frequency:

$$f_{conv\ max} = 1.0\ \text{MHz}$$

This also determines the resonant tank circuit frequency using the topology conversion coefficient, K_t.

$$K_t = f_{conv\ max}/f_{res}. \quad \text{Use } K_t = 0.8$$

2. Calculate the resonant tank frequency, f_{res}

$$f_{res} = f_{conv\ max}/K_t = 1\ \text{MHz}/0.8 = 1.25\ \text{MHz}$$

3. Determine the transformer turns ratio, N

$$N = N_{pri}/N_{sec} = K_tV_{IN\ min}/(2V_{out} + V_{diode}) = 5.19 \quad \text{(use 5:1)}$$

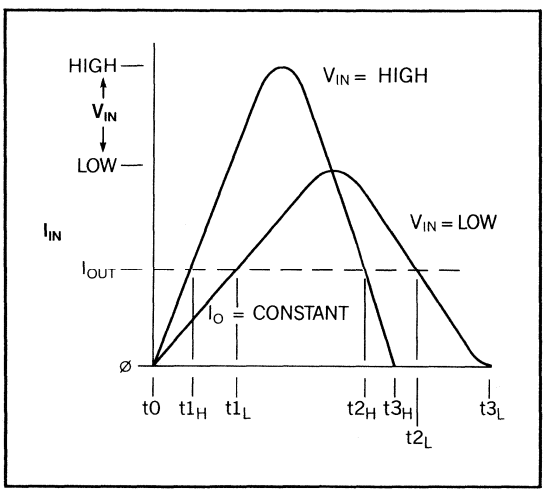


Fig. 14 - Effects of Line Change on I_{in}

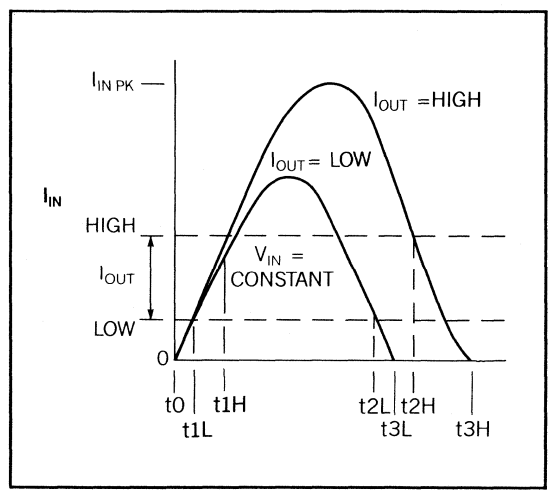


Fig. 15 - Effects of Load Change on I_{in}

4. Calculate $V_{in\ min}$, the minimum input voltage referred to the secondary:

$$V_{in\ min} = V_{s\ min}/2N = 220V/(2 \cdot 5) = 22\ V$$

The resonant inductor and capacitor values are calculated using the minimum input voltage to the secondary.

5. Calculate the resonant inductor value, L_r

$$L_r = 0.12V_{in\ min}/f_{res}I_{out\ max} = 176\ nH$$

6. Calculate the resonant capacitor value, C_r

$$C_r = .025/f_{res}^2 I_{out\ max} = 90.9\ nF$$

7. Calculate and check resonant impedance Z_n

$$Z_n = (L_r/C_r)^{1/2} = 1.39\ \Omega \text{ (yes, <1.5 ohms)}$$

The basic sections of the circuit are now complete. Detailed analysis of the primary and secondary voltages and currents follow.

Peak current calculations: The peak secondary current is approximated by:

$$I_{sec\ pk} = I_o + V_{in}/Z_n = I_o + V_s/(2 \cdot N \cdot Z_n)$$
$$= .072\ V_s$$

The peak current is a function of both input voltage and output current, and is graphically shown in Fig. 16.

The need for high peak current devices in a resonant mode power supply is evident from the values shown below, especially compared with a square wave converter of similar output power.

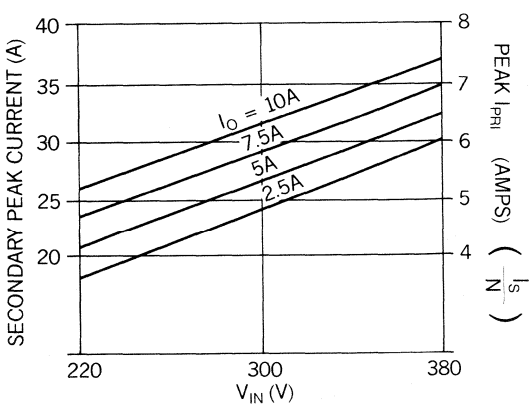


Fig. 16 - Peak Secondary Current vs. V_{in} and I_o

The peak secondary voltage is:

$$V_{s\ pk} = V_{s\ max}/2N = 370/2 \cdot 5 = 37V$$

Rectifiers in the secondary circuit need to block at least twice the peak voltage, and are typically selected with a much higher rating. Schottky diodes can be ruled out in this 15V output application due to their 45 to 90 volt breakdown voltages, so an ultra to hyperfast diode is required. A 150 volt,30 amp (DC) device provides ample safety margin. A low capacitance power package is also desired to minimize parasitics and power losses.

rms current calculations: The primary and secondary RMS currents can be approximated to a high degree of accuracy by a pulsed sinusoidal waveform. The relationships derived in the previous section for peak currents, *on* times and conversion frequencies will be used to calculate the RMS currents incorporating the following equation.

$$I_{rms} = I_{peak}\left[\frac{T_{on}}{2\ T_{per}}\right]^2$$

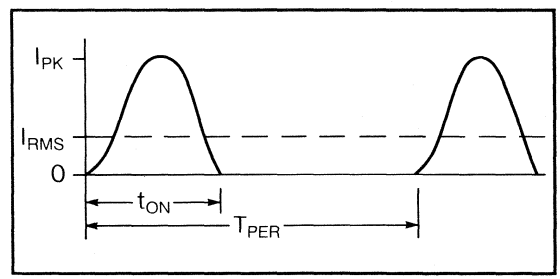


Fig. 17 - rms Current Calculation

The primary current calculations will use the conversion period of $1/f_{conv}$ due to the bidirectional switching of the primary. Secondary currents conduct only once per two conversion periods due to the bridge arrangement of the secondary windings. Both low and high input voltage conditions will be examined at full output load to determine worst case conditions.

The transformer primary wire size will be calculated using the rms current components, in addition to thermal considerations of the transistor switches and rectifiers.

Each of the Mosfet switches, secondary rectifiers and transformer secondary windings conduct current only once per two conversion

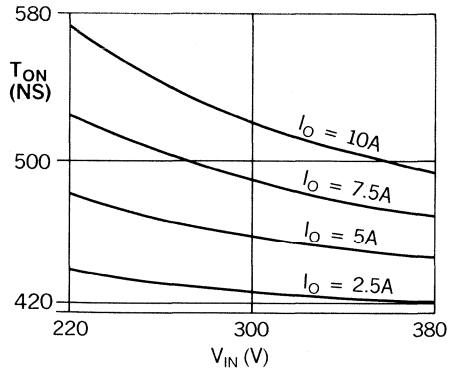


Fig. 18 - On Time vs. V_{in} and I_{out}

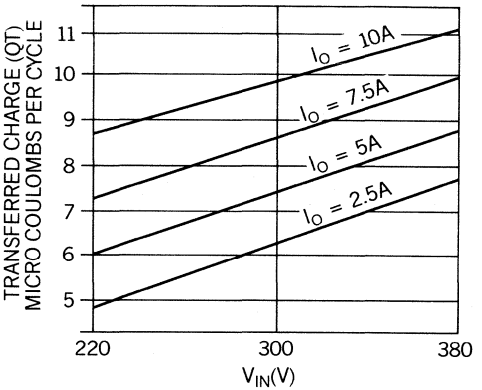


Fig. 19 - Q_t, Transferred Charge vs. V_{in} and I_{out}

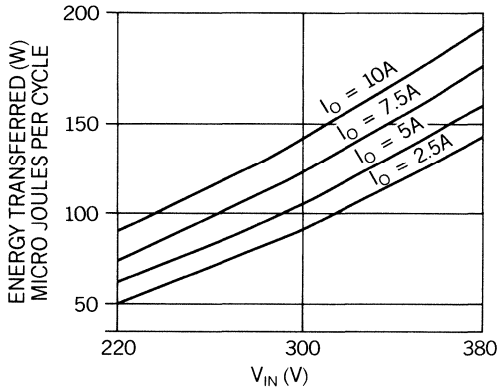


Fig. 20 - Energy Transfer per Cycle vs. V_{in} and I_{out}

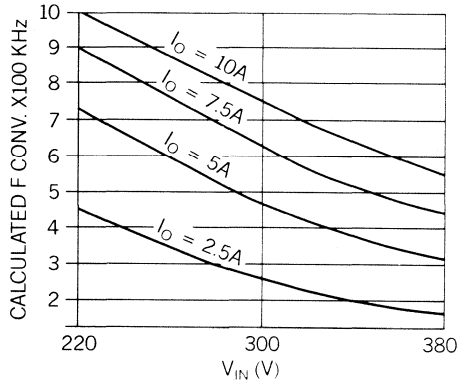


Fig. 21 - Calc. Conversion Freq vs. V_{in} and I_{out}

cycles. This results in a lower rms current through each device.

Low Line	High Line
$I_{sec\ pk}$ = 26 A	$I_{sec\ pk}$ = 37 A
$I_{pri\ pk}$ = 5.2 A	$I_{pri\ pk}$ = 7.4 A
t_{on} = 575 ns	t_{on} = 495 ns
T_{per} = 1.0 µs	T_{per} = 1.82 µs

rms Transformer Primary Current:

$I_{pri\ rms}$ = 2.78 A $I_{pri\ rms}$ = 2.72 A

rms Current - Mosfet Switches and Secondary Rectifiers:

$I_{rect\ rms}$ = 9.86 A $I_{rect\ rms}$ = 9.65 A

$I_{MOS\ rms}$ = 1.97 A $I_{MOS\ rms}$ = 1.93 A

Timing Considerations: The operation of this quasi-resonant circuit has been described as requiring a variable frequency, *fixed on time* control pulse train. Actually, the *on* time must be varied to facilitate zero current switching with changes in input voltage and output current. Using the timing relationships presented earlier, the *on* time is calculated and plotted for the ranges of V_{in} and I_{out} in Fig. 18.

Transferred charge: The charge transferred from the primary to the secondary per cycle is a function of both V_{in} and I_{out}. Using the equations presented in the Appendix, the results are graphically represented in Fig. 19.

For the selected values of voltage and current shown, the average change required in voltage or output current per microCoulomb transferred have been calculated:

Avg dV/µC = 5.935, and Avg dI/µC = 2.086

The energy transferred per cycle is obtained by multiplying the results from the charge calculations by $V_{in}/2$ to convert from charge to energy, with the results shown in Fig. 20.

The conversion period is obtained by dividing the energy transferred per cycle by the out-

put power, accounting for an overall efficiency near 85%. Conversion frequency, its inverse, is graphically depicted for various input voltages and output currents in Fig. 21.

Power Mosfet Switch Considerations

The power Mosfet selection process must take into account the three types of losses incurred by the high voltage switch. First, and probably the most predominant loss contributor is the FET *on* resistance, or $R_{ds(on)}$. Conduction losses are minimized by using a FET with the lowest $R_{ds(on)}$ obtainable.

$$P_{loss\ dc} = I_{pri\ rms}^2\ R_{ds(on)} \quad \text{(Watts)}$$

Generally the low resistance is attained by paralleling numerous FET cells of higher on resistance. The result is a single high current, low resistance device with a large die size, or geometry. This technique is great for lower frequency applications where the transition (turn-on and turn-off) times are a small percentage of the entire duty cycle. At high frequencies and especially with high voltages, this paralleling scheme introduces many difficulties in minimizing the switching transition losses.

Each cell has a finite output capacitance which quickly "adds up" when many are placed in parallel. The FET output capacitance is charged and discharged to the FULL input bulk voltage each cycle, contributing losses. At high frequencies, changing to a larger size FET could increase the total FET losses, despite having a lower *on* resistance. The incremental gains of lower conduction losses are lost to the higher switching losses of the larger capacitance FET. For this reason, it is a worthwhile exercise to examine several different size FETs over the line and load ranges of this design.

$$P_{loss\ ac} = 0.5 C_{oss} V_{in}^2 f_{conv}/2 \quad \text{(Watts)}$$

The gate drive power losses are generally negligible with respect to the total losses, but can be calculated from:

$$P_{loss\ gate} = 0.5 V_{aux} Q_t f_{conv}/2 \quad \text{(Watts)}$$

where Q(t) is the FET total gate charge, accounting for the gate to source charge plus the Miller effect charge.

The greatest primary current occurs at full load, which will be used for the worst case evaluation of power losses. Both high and low input voltage were used to calculate the ac losses, then averaged. The following list is a summary of the total power loss for each Mosfet switch in this application. A 100°C junction temperature at the FET die was assumed, where the actual *on* resistance is double that of the published specification. Various size FETs have been analyzed to compare the ac and dc losses to select one which exhibits the lowest total losses.

Circuit specifics (at the FET switches):

$I_{pri\ rms}$ = 1.97A at V_{in} = 220V, f_{conv} = 1 MHz

$I_{pri\ rms}$ = 1.93A at 375V, 550 KHz

Device @100°C	R_{ds} Ω	C_{oss} pF	Q_g nC	P_{dc} W	P_{ac} W	P_g W	P_{total} $W_{(ea)}$
IRF720	3.6	64	20	13.7	1.05	0.08	14.87
IRF730	2.0	100	35	7.62	1.57	0.11	9.30
IRF740	1.1	210	63	4.19	3.30	0.19	7.68
IRF820	6.0	54	19	22.8	0.85	0.07	23.78
IRF830	3.0	91	32	11.4	1.43	0.10	12.96
IRF840	1.7	180	63	6.47	2.83	0.19	9.49
IRFP440	1.7	180	63	6.47	2.83	0.19	9.49
IRFP450	0.8	350	130	3.04	5.51	0.39	8.95
IRFP460	0.54	480	190	2.05	7.56	0.57	10.19

The lowest overall losses are obtained with the 740 type devices which will be utilized in this application. This procedure will yield different results for each application, and is a recommended step towards minimizing power losses.

Rectifier Selection

Evident from Figures 16 and 17 is the need for high performance rectifiers to achieve an overall high efficiency power supply. Peak secondary currents approach 40 amps, with an rms component near 14 amps. Due to the high peak reverse voltages of nearly 100 volts, Schottky diodes cannot be used as the secondary rectifiers. Even the "freewheeling" diode must withstand 80 volt peaks at high line.

Reverse recovery times must be minimal to prevent reverse current from flowing in the primary switches in addition to enhancing efficiency. While the circuit currents are quasi-sinusoidal, the rectifier voltage is not. Parasitic inductances and capacitances of the

device and its package must also be accounted for as part of the resonant L-C tank. This implies that the transformer will be designed for a lower leakage inductance than the resonant L and external inductance will be introduced to obtain the precise amount.

The TO-247 package will be utilized for two reasons. First, it has lower parasitics and is better suited to high frequency applications than its TO-3 metal case counterpart. Second, it is simple to heatsink this flat package, which can be mounted in various configurations.

Unitrode UES3015S ultrafast 30 amp, 150 volt rectifiers were selected for the secondary input diodes. Typical performance characteristics are 35 ns reverse recovery times and less than 1 V forward drop at 30 A and 125°C junction temperature. The "freewheeling" diode used is a Unitrode UES1615S ultrafast type, with 16 amp dc capability and a forward drop of less that 0.85 V. It too exhibits a 35 ns reverse recovery time.

Power dissipation and heatsinking requirements for each device can be calculated using the secondary currents obtained previously in this power supply design. Snubbing of each diode will be left to the prototype stage when any parasitic circuit influences can be evaluated.

Main Transformer Design

The transformer design begins with a basic idea of the core geometry most applicable to the particular design. Off-line supplies lend themselves to low, wide winding windows, typical of the ETD geometry. This window shape provides adequate room to accommodate the creepage and clearance distances required for international safety specifications.

Switching of the transformer primary will occur at a maximum of 500 KHz, and standard ferrite materials will be utilized in this example. With numerous choices to consider, the 3C6A material was selected.

To begin this 150 watt design, a fair estimate is to keep the transformer losses around 1% of the total input power, or approximately 2 watts. In addition, the transformer temperature rise is desired to be less than 40°C for combined copper and core losses. A core size can be approximated knowing that its thermal resistance, R_t, needs to be in the neighborhood of 40°C/2W, or less than 20°C/W. This is useful as a first iteration to determine the approximate operating flux density required. The precise size will be calculated using the area product formula for core-loss limited conditions, typical in a high frequency power supply.

$$AP = \left[\frac{P_{in} \cdot 10^4}{120K\ 2f} \right]^{1.58} \cdot (K_h f + K_e f^2)^{0.66} \quad cm^4$$

where:

Pin - Input Power = 180 Watts
K - Winding Factor = 0.163 for half bridge
f - Transformer Frequency = 500 KHz
K_h - Hysteresis Coeff. (3C6A) = $4 \cdot 10^{-5}$
K_e - Eddy Current Coeff. (3C6A) = $4 \cdot 10^{-10}$

For this design,the area-product calculates to 0.543 cm^4, which is slightly less than the smallest standard core size, the ETD-34. Because the core volume is slightly larger than required, the actual core losses (per cm^3) will be lower than first estimated.

The manufacturers core data lists the thermal resistance of the ETD-34 core set as 19°C/W, with a core volume of 7.64 cm^3. Several methods of dividing the power losses between the core and copper can be used. The most common of these suggests an almost equal split between the two, allowing slightly more core than copper loss if possible. An even division of the total losses between the two will be utilized in this design as a first approximation. Later, an evaluation of the minimum number of turns and wire sizes may suggest that the 50/50 ratio be changed to favorably accommodate fewer turns, or less copper. The actual core power density, P_d, is calculated from the following equation, allowing a 20°C temperature rise, T_r, due solely to core losses.

$$\text{Power Density} = \frac{T_r}{R_t \cdot Vol} = \frac{20°C}{19 \cdot 7.64}$$

$$= 138\ mw/cm^3$$

Referencing the manufacturers data sheet for the 3C6A material at a power loss density of approximately 140 mW/cm^3 and a 500 KHz operating frequency, it is determined that an operating flux density of 300 gauss (0.030 T) be

used. The total flux density swing, ΔB, is twice that, or about 0.060 Tesla. The minimum number of primary turns is calculated assuming 5 V primary drops, low line conditions, and a cross-sectional core area, A_e, of 0.971 cm^2.

$$\text{Power Density} = \frac{V_{pri} t_{on} \cdot 10^4}{\Delta B \cdot A_e}$$

$$= \frac{105 \cdot 575 \cdot 10^{-9} \cdot 10^4}{.060 \cdot 0.971} = 10.3 \text{ turns (use 10)}$$

A turns ratio N of 5:1 was previously established for this design. Minimized leakage inductance is obtained by "sandwiching" the secondaries between the two primary halves. In this example, one-half of the primary turns will be wound first, closest to the core center leg. Then, the entire secondary is wound directly above the primary half. The final winding is the remaining primary half, as shown in Fig. 22.

Copper strip or foil will be utilized for each winding to minimize "build-up " which increases the distance between windings, hence increases leakage inductance. If the transformer leakage inductance is greater than the required resonant inductance, then the transformer must be redesigned for lower leakage.

The required primary and secondary copper cross-section areas are calculated using their respective currents divided by 450 amps/cm^2 for a low temperature rise. Other transformer specifics are calculated below.

Primary rms current, $I_{pri\ rms}$ = 2.78 A rms

Secondary rms current, $I_{sec\ rms}$ = 9.86 A rms

Primary copper area, $A_{xp} = I_{pri\ rms}/450 = .0062\ cm^2$

Secondary copper area, $A_{xs} = I_{sec\ rms}/450 = .022\ cm^2$

Pri. inductance, $L_{pri} = A_L N_p^2 = 190\mu H$

Sec. (half) inductance, $L_{sec} = A_l N_s^2 = 7.6\mu H$

The primary conductor area is approximately equal to the area of an AWG # 19 wire, while the secondary area is closest to AWG #14. Eddy current calculations show that the depth of penetration at 500 KHz is .0106 cm, or about the thickness of a number 37 AWG wire. The most practical technique to minimize the AC loss in a transformer winding is to use copper strip or foil, as in this design. Its width is determined by the bobbin width and safety creepage requirements of 8 millimeters as shown.

The required 8 mm primary to secondary spacing between winding ends will be subtracted from the bobbin width of 2.10 cm, leaving 1.30 cm (0.51 inch) for the copper strip width. Allowing for tolerances, standard 0.5 inch width foil will be used in this design. The strip thickness is calculated by dividing the required copper area by the 1.27 cm (0.5 inch) width.

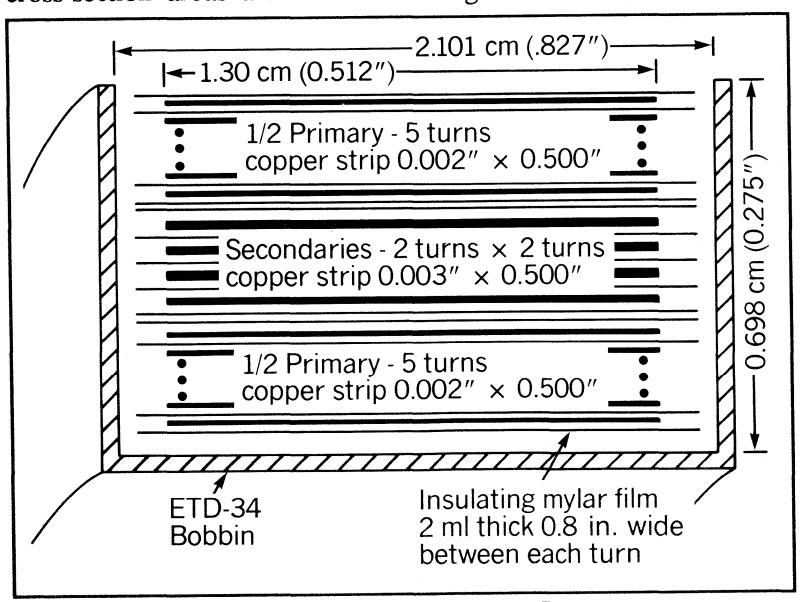


Fig. 22 - Transformer Winding Layout

Pri thickness = A_{xp}/Width = $6.18 \cdot 10^{-3}/1.27$
= .00475 cm, or .00187 in
Sec thickness = A_{xs}/Width = $21.9 \cdot 10^{-3}/1.27$
= .01685 cm, or .00663 in

Standard 2 mil (0.0051 cm) foil will be used for the primary. This is slightly larger than the required thickness of .00475 cm, and is less than 1/2 the .0106 cm penetration depth. Secondary penetration is from both sides because of the interleaved primary, so the calculated secondary thickness should be and is less than twice the penetration depth. Two paralleled 3 mil foils are used as secondary conductors.

The resistance and power loss of each winding is calculated from the following relationships, based on the resistivity of copper at 100°C, $\rho_{cu} = 2.29 \cdot 10^{-6}$ Ω-cm. Total copper and core losses are also highlighted, in addition to the total temperature rise at the maximum conversion frequency.

$$\text{Winding resistance} = \frac{\rho_{cu} \cdot \text{avg length/turn} \cdot N}{A_x}$$

$R_{pri} = 2.29 \cdot 10^{-6} \cdot 5.99 \cdot 10 / 6.18 \cdot 10^{-3} = 22.2\,m\Omega$

$R_{sec} = 2.29 \cdot 10^{-6} \cdot 5.99 \cdot 2 / 21.9 \cdot 10^{-3} = 1.25\,m\Omega$

$P_{loss\ winding} = I_{rms}^2 \cdot R$

$P_{loss\ pri} = 2.78^2 \cdot .0222 = 171$ mW

$P_{loss\ sec} = 9.86^2 \cdot .00125 = 121.5$ mW

$P_{loss\ copper} = 2 \cdot 0.171 + 0.1215 = 0.4635$ W

Total power loss = copper losses + core loss

$P_{total} = 0.464 + 1$ (approx) ≤ 1.5 W

Temp. rise = $Rt \cdot P_{total} = 19°C/W \cdot 1.5W$
= 28.5°C

Output Inductor Design

The output inductor will be designed for one amp of ripple current at the minimum conversion frequency of approximately 200 KHz. Due to the variable frequency operation, the ripple current will change inversely with operating frequency, as maximum load occurs, the ripple current is at its lowest. This mode of operation helps lower the overall losses at full load because with lower ripple the peak current that must be switched is less. In addition, it reduces the size of the output choke since the peak (DC+AC) and full load (DC) current are within one percent of each other.

$$L_o = [(V_{out} + V_{diode}) \cdot t_{off\ max}] \,/\, \Delta I_{out}$$

$$= 15.8V \cdot 5\ us \,/\, 1\ A = 80\ \mu H \text{ (approx)}$$

At the maximum conversion frequency and $t_{off\ min}$, the output ripple current reduces to:

$$\Delta I_{out} = [(V_{out} + V_{diode}) \cdot t_{off\ min}] \,/\, 80\,\mu H = .08\ A$$

Referring to Section M5 of the Unitrode Seminar Manual, core selection starts by calculating the area product:

$$AP = A_w A_e = \left[\frac{L_o I_{pk} I_{fl} \cdot 10^4}{420 \cdot K \cdot B_{max}}\right]^{1.31}$$

$$= \left[\frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10 \cdot 10^4}{420 \cdot 0.7 \cdot 0.3}\right]^{1.31} = 0.89\ cm^4$$

A PQ type geometry has been selected for the output choke application. The core set closest in size to the required area product is the PQ 32, which is available in either a 20 or 30 mm height. Of the two, the PQ32/20 size will be used because its height is similar to the ETD34 core set used for the main transformer. Its magnetic area is 1.70 cm^2.

$$N_{min} = \frac{L \cdot I_{pk}\, I_{fl} \cdot 10^4}{B_{max} A_e}$$

$$= \frac{80 \cdot 10^{-6} \cdot 10.08 \cdot 10^4}{0.30 \cdot 1.7} = 15.8 \text{ turns (use 16)}$$

The cores will require gapping to store the required energy without saturating. Gap length is calculated from the inductance formula:

$$\ell_g = (\mu_o \mu_r N^2 A_e \cdot 10^{-2}) \,/\, L = .068\ cm$$

using $\mu_o = 4\pi \cdot 10^{-7}$ and $\mu_r = 1$ (air)

Correcting the gap length for the fringing field, a gap of .082 cm (.032") should be used.

Again, copper strip is used to minimize losses. Winding resistance and power loss calculations are similar to those of the main transformer design,and total less than 1.5 W.

Output Capacitor

There are two components of ripple voltage which need to be considered in meeting the design goal of 100 mV. They are both caused by inductor ripple current. The first is simply:

$$\Delta V_{out} = \Delta Q / C_{out}$$

For a given ripple current, this component is minimized by increasing the capacitor value. If this were the only contributor, the minimum capacitance required is:

$$C_{outmin} = \frac{1}{2} \frac{\Delta I_{out}}{2} \frac{1}{2f} \frac{1}{\Delta V_{out}}$$

This component varies with frequency. At $f_{conv\ min}$, 6.25 µF are needed, but at $f_{conv\ max}$ (1MHz) only 0.1 µF is required to maintain the ripple voltage specification.

The second (and usually predominant) ripple voltage component is the voltage drop across the capacitor Equivalent Series Resistance (ESR) caused by the ripple current of ΔI_{out}. The maximum ESR allowable for 100 mV ripple is:

$$ESR_{max} = 100\ mV / 1.0\ A = 100\ m\Omega$$

The two ripple voltage components do not add directly as they are in quadrature. With electrolytic capacitors, the ESR component dominates the capacitor selection. The resulting capacitance value is so much greater than the minimum value required that the $\Delta Q/C_{out}$ term can be ignored. An added benefit of a large output capacitance is the improvement in load transient capability.

In this design, two 100 µF electrolytic units were used in parallel to achieve an ESR value of 3 to 15 milliohms - a broad range necessitated by the difficulty in getting specified high frequency data from capacitor manufacturers.

A final component added to the output filter is a good high frequency capacitor to bypass the inductive components of the electrolytics and shunt any switching spikes which might get to the output. Unitrode "P" type ceramic monolithic capacitors are used for this application. Different capacitor types and values can be paralleled to obtain a low impedance over a broad frequency range, useful in this variable frequency application.

Gate Drive Circuitry

The ideal gate drive circuit must deliver sharp turn-on and turn-off pulses to the high voltage power Mosfets. This is made possible by the UC3860 controller's high speed totem pole drivers. Delivering 3 amp peak currents, the drivers have typical rise and fall times of 25 ns into a 1 nF load.

Half bridge circuits require the use of a gate drive transformer to electrically isolate the "high-side" switching transistor from the control circuit. Driving both transistors from the same transformer 180° out of phase offers nearly identical drive signals to each transistor. This tends to balance the switching losses and maintain a narrower band of the associated transition EMI.

The drive transformer must have low leakage inductance to provide crisp edges during the transitions with little overshoot. This makes zener clamps and snubbing circuits unnecessary at the transformer outputs. A 0.50" O.D. toroid is used, fitted with three identical windings of ten turns each. This helps minimize the transformer magnetizing current and maximizes the peak current delivered to the FET gates.

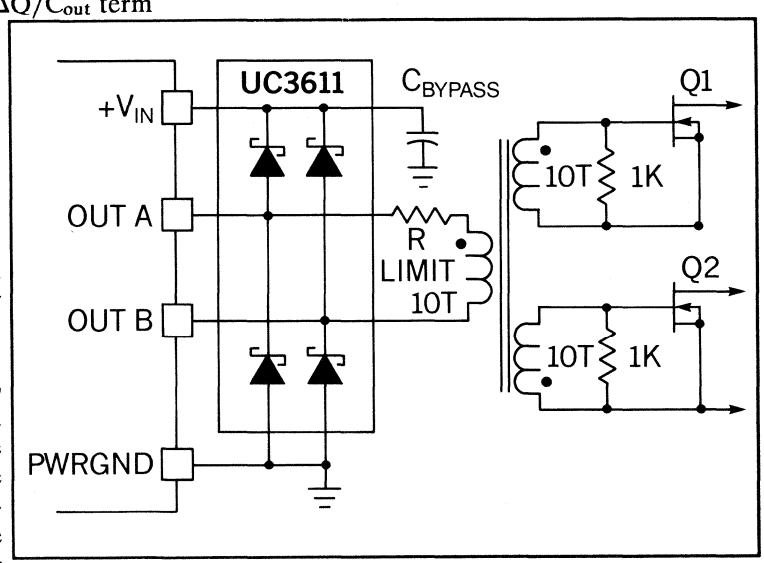


Fig. 23 - Gate Drive Circuit

Resistors from gate to source at each FET provide a fairly low impedance to prevent turn-on during start-up while the IC may still be in undervoltage lockout. During regular operation, these resistors have negligible impedance.

On the controller side, the UC3611 quad Schottky diode prevents the IC outputs from going below ground, avoiding substrate biasing problems. A series resistor limits the peak current to the 3 A rating, and the transformer is reset while both outputs are low, between cycles.

Zero Current Detection and Switching

The primary current is used for two important functions in this design, fault protection and zero current detection. A typical configuration is shown in Fig. 26. The generalized circuit starts with the use of a current transformer in series with the primary of the main transformer to detect primary current. A turns ratio of 1:25 reduces the switch current to a manageable level. It is full wave rectified by 1N4148 diodes (D_6-D_9) and converted to an appropriate unipolar voltage at the current sense resistor, R_{11}. In addition, zero current or zero voltage can be detected by using the UC3860 uncommitted comparator. Its open collector output can interface with the RC *on* timing pin of the one shot, pulling it below the turn off threshold at zero detection. As shown in Fig. 24, this reduces the *on* time of the one shot timer, allowing the Mosfets to switch at zero current for high efficiency.

Implementation requires shifting the noninverting input between two thresholds so that only the falling edge of primary current is an acceptable input for switching to occur. (See Fig. 25.) This is done to prevent a false output from the comparator during the beginning of the cycle, where zero current also occurs. Primary current sensing will be offset by the resistor divider network R_{21} and R_{16} from V_{ref} to ground. This is fed into the inverting

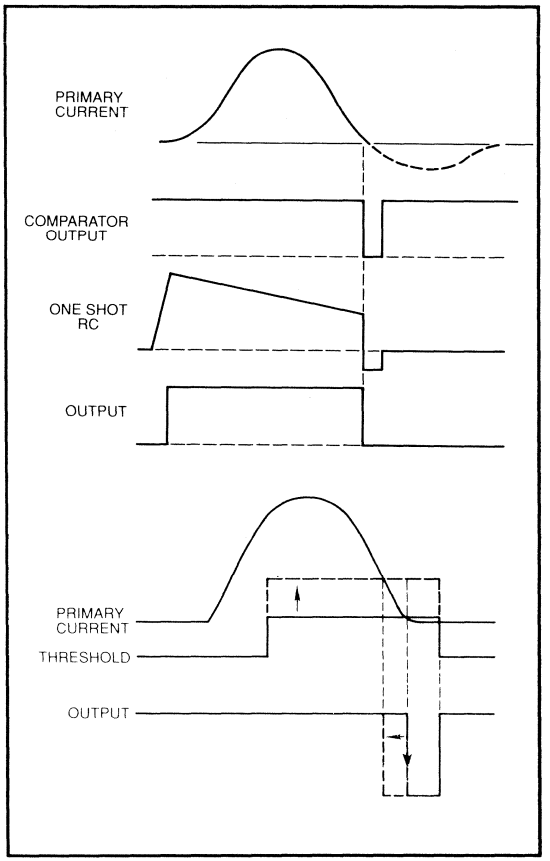


Fig. 24 & 25 - Zero Current Switching

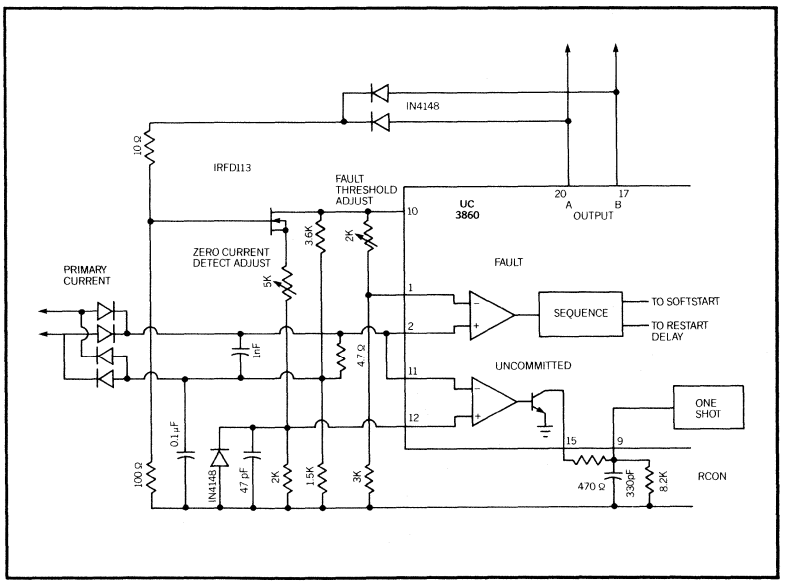


Fig. 26 - Zero Current Switching Circuitry

input of the uncommitted comparator.

In Fig. 26, adjustments can be made to provide a comparator output *just* prior to zero current by resistor R20. Propagation delays throught the IC and drive circuitry, although minimal, can effectively be "nulled-out" along with Mosfet delays by this technique.

The UC3860 Resonant Mode Control IC

The block diagram of the UC3860 in Fig. 27 displays several key building blocks which together provide the functions necessary for precise resonant mode control. To begin, the undervoltage lockout turn-on and turn-off thresholds are pre-programmed for 17 and 10 volts respectively and are used in their standard configuration. This allows ample time for start-up and bootstrapping to occur in an off-line supply while providing adequate Mosfet gate drive voltages. The UVLO can also be reprogrammed for other turn-on and off thresholds. Also, it functions as an alternate shutdown mechanism. While UVLO is invalid, the UC3860 reference voltage output is held low, deactivating the internal circuitry. The 1% accuracy 5.0 V bandgap reference is capable of driving ten milliamps maximum external loads.

The power supply output voltage will be divided down to deliver 3.0 volts at the inverting error amplifier input for the desired V_{out}. With its high gain-bandwidth of 5 MHz, this voltage type op amp also features controlled output voltage excursions. The error amp output swings from 0.0 to 2.0 V above the voltage at the VFO I_{osc} input and tracks this node over temperature. This mechanism facilitates the maximum conversion frequency clamp in addition to the voltage (or current) to frequency conversion gain.

Variable frequency operation commences with the error amplifier providing a variable output voltage. This is transformed to a variable current at the VFO variable current input, I_{vfo}. Internal circuitry mirrors this current to the VFO timing capacitor, C_{vfo} . Maximum fre-

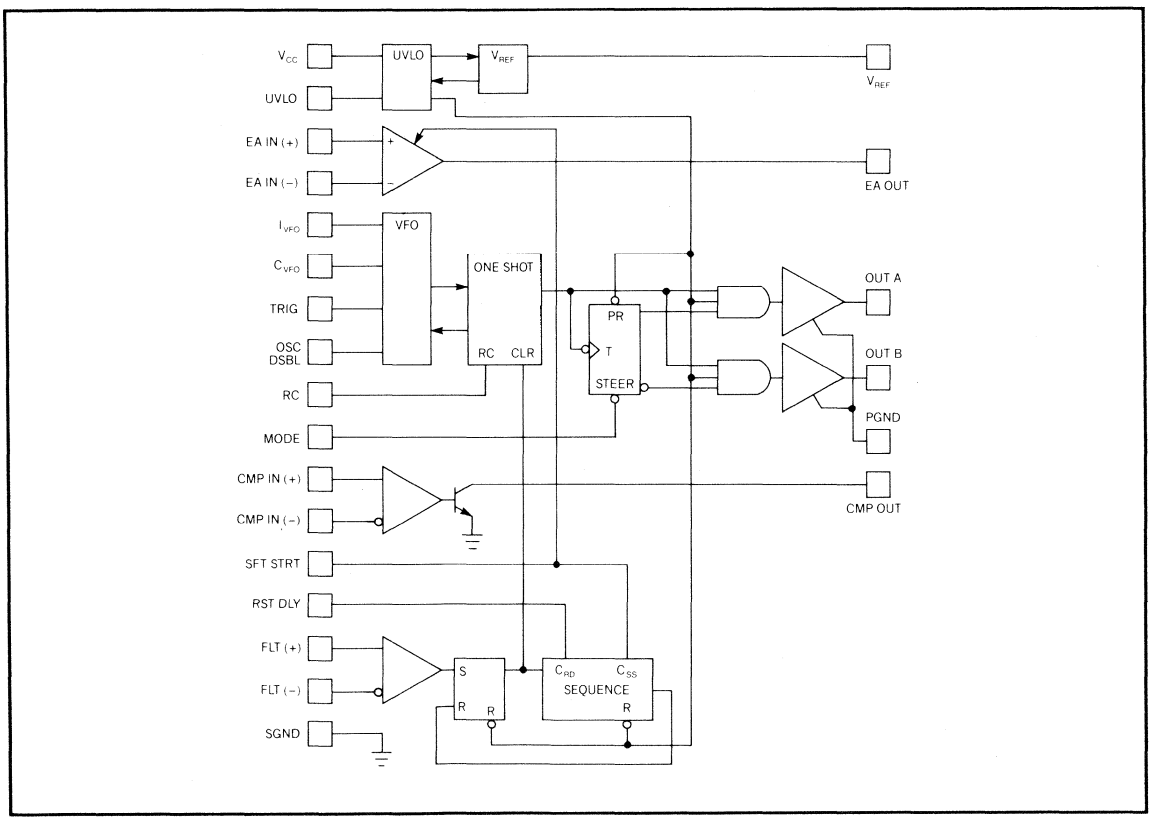


Fig. 27 - UC3860 Block Diagram

quency occurs at $2.0V/R_{vfo} \cdot C_{vfo}$, which coincides with the error amplifier upper clamp. Minimum frequency is also programmable via resistor R_m from V_{ref} to the I_{vfo} input. The frequency to voltage gain of the IC in MHz/V (or GHz/V) is also established by these timing components. Additionally, the VFO can be externally triggered and/or disabled at the respective input pin accommodations.

Fixed on-time pulse widths are generated by the programmable one-shot timing circuit. An RC network is charged by an internal source at the onset of a cycle, then self discharges during the on-time. This occurs between the precise thresholds of the one-shot's comparators. On-time can easily be shortened by an external influence used to discharge the RC components below the comparator's turn-off threshold. This architecture simplifies interfacing with various forms of zero voltage or zero current type switching. The output of the UC3860 uncommitted comparator is an open collector which can interface directly to the one shot (RC) timing pin.

Programming the VFO and One-shot:

Let C_{vfo} = 330 pF, $C_{oneshot}$ = 330 pF
f_{max} = 1.05 MHz, f_{min} = 200 kHz

1. $f_{max} = 2V/R_{vfo}C_{vfo}$;
   $R_{vfo} = 2/(1.05MHz \cdot 330pF) = 5.77\ k\Omega$

2. $f_{min} = 1V/R_mC_{vfo}$;
   $R_m = 1/(0.2MHz \cdot 330pF) = 15.15\ k\Omega$

3. $t_{on} = 0.22 \cdot R_{on} \cdot C_{on}$;
   $R_{on} = 600ns/(0.22 \cdot 330pF) = 8.26\ k\Omega$

The output from the one-shot feeds another programmable module, the toggle flip-flop. Logic selection at the Output Mode pin either alternates the outputs for dual-ended configurations, or unifies outputs A with B for single ended applications. As V_{ref} becomes valid, the toggle flip-flop is always steered towards the A output. While this may be of little concern in some designs, a predictable sequence of events upon power-up is always facilitated.

Each totem-pole output is specified for 3 Amp peak drive pulses, sufficient to insure abrupt transitions at the Mosfet switches. When operating in unison, a 6 A peak current is obtained. Rise and fall times into a 1 nF load are typically 20 nanoseconds. As seen in previous high power IC's, the totem pole power ground is terminated through a separate pin which isolates its power ground noise from that of the IC's signal ground.

Soft start is accomplished by limiting the amplifiers output voltage to that of the soft start pin, typical in most IC controllers. An internal 5 microamp current source from V_{ref} pulls up on the external soft start capacitor, which gradually increases the conversion frequency upon start-up, as opposed to widening the pulse width in conventional PWMs.

Fault protection and management circuits included in the UC3860 are fully user programmable. A fault comparator which has both inverting and non inverting inputs is used to drive a programmable sequence latch. The operation of this latch is controlled at the programmable Restart Delay (RST DLY) pin, and has three unique modes. First, it can be oriented to latch the outputs off until UVLO or V_{cc} are toggled, similar to firing a shutdown SCR. Secondly, it can be used to cease operation until the fault input is removed from the comparator, then recommence operation. The third and most popular mode is often referred to as "hiccup" mode. After receiving a fault, the outputs are turned off for a programmed time interval called the restart delay. Operation is then resumed, provided of course that the fault was removed. Implementation only requires a capacitor from RST DLY to ground.

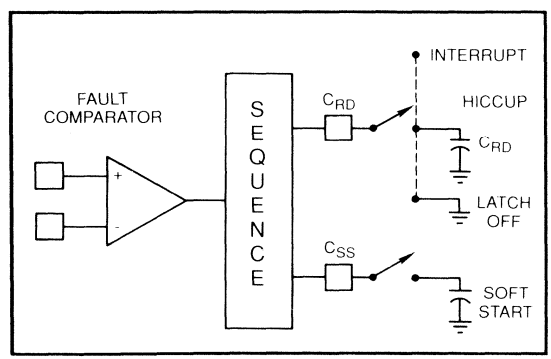


Fig. 28 - Fault Management Programming

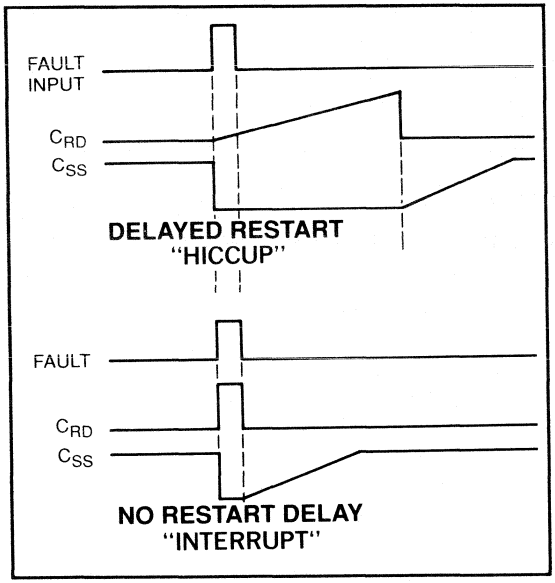


Fig. 29 - Fault Management Waveforms

Closing the Loop

There are several gain stages in the quasi-resonant control loop, and each will be examined to obtain good closed loop circuit response. The block diagram below displays the various gain stages.

Error Amplifier: A reference voltage is applied to the noninverting input of the error amplifier, and the power supply output voltage, through a voltage divider, is applied to inverting input. The error amplifier (E/A) output is commonly referred to as the error voltage V_e, which is an amplified signal corresponding to the deviation of the power supply output voltage from the desired level. The compensation network is designed last, after analyzing the other loop gain contributors. It will provide adequate phase margin at the desired zero dB crossover point to ensure circuit stability.

The varying E/A output voltage V_e is used to generate a variable current to the VFO current input pin, I_{vfo}. As this current is varied, so is the power stage conversion frequency. A higher V_e corresponds to a higher conversion frequency. These values are designed to track each other over temperature, and a linear voltage to current transformation can be assumed. The voltage to current gain into the VFO equals the 2 volt maximum output swing of the error amplifier divided by the VFO input resistor.

Variable frequency oscillator: The variable frequency converter stage accepts an input current at the I_{vfo} input and generates a proportional output frequency. The gain of this stage is programmed by the E/A output voltage with the I_{vfo} input resistor and the VFO timing capacitor, C_{vfo} . The VFO output frequency is approximated by:

$$f_{osc} = I_{vfo}/C_{vfo} \text{ , and } f_{max} = 2V/(R_{vfo} \cdot C_{vfo})$$

The minimum frequency is programmed by a resistor from V_{ref} to the I_{vfo} input, and the transformation of the error amplifier output voltage to frequency is quite linear.

Error amplifier voltage swing = 2 Volts

f_{conv} = 200 kHz min – 1 MHz max

VFO gain:

G_{vfo} = Δ800 kHz / Δ2 V = 0.4 MHz/V

Power stage: The small signal gain of the power stage is approximated by analysis of the charge transferred at various line and load combinations. An assumption is made that the power switch *on* time is constant, and any changes in frequency directly effect the *off* time, or resonant capacitor discharge time. In addition, both V_{IN} and I_{out} are assumed to be constant during the interval of interest.

Based on the relationship that the energy into the resonant circuit, W, equals the output power multiplied by the conversion period:

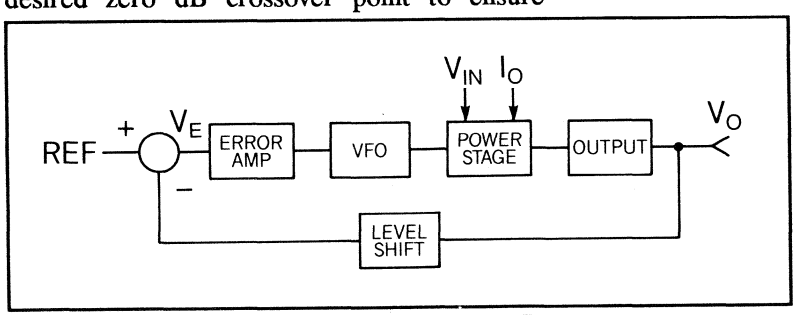


Fig. 30 - Control Loop Block Diagram

$$W = (Q_{in}V_{sec}/2) = \text{Power} \cdot t_{conv}$$
$$= V_{out}I_{out}/f_{conv}$$

therefore:

$$V_{out} = f_{conv}W/I_{out}$$

This term is assumed constant for the interval of interest.

Tabulated below at several points of interest are the values for the power stage gain, from the results of a previous section in this presentation. The gain (in volts per MHz) varies significantly over the input and output ranges, and the highest value will be used to approximate the worst case condition.

V_{IN} sec V	I_{out} A	W_{in} μJ/cyc	f_{conv} kHz	Gain V/MHz	Gain dB
22	2.5	50	450	9.0	19.1
38	2.5	140	180	10.1	20.1
22	5	60	730	8.76	18.9
38	5	160	320	21.4	26.6
22	7.5	78	900	19.3	25.7
38	7.5	185	450	22.6	27.0
22	10	91	1000	19.1	25.6
38	10	205	560	23.6	27.5

The worst case value of 23.6 V/MHz will be used for the power stage. Multiplying this by the VFO gain of 0.4 MHz/V results in a combined gain V_{out}/V_e of 9.44 (19.5 dB).

Output Filter Section: The output filter response is defined by :

L_{out} = 80 μH; C_{out} = 200 μF

R_{out} = 1.5 Ω min to 10 Ω max

ESR = 2 to 10 mΩ

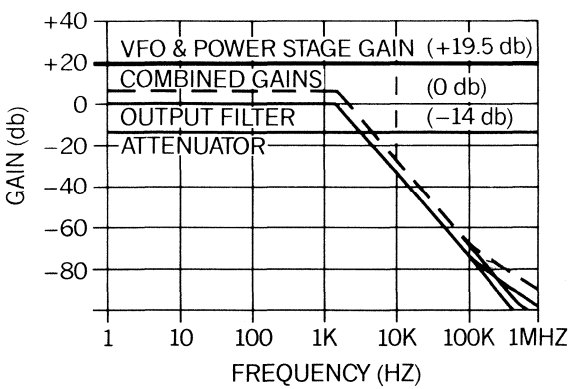


Fig. 31 - Gains vs. Frequency

$$\text{Pole frequency} = \frac{1}{2\pi(L_{out}C_{out})^{0.5}} = 1.25 \text{ kHz}$$

$$\text{ESR Zero} = \frac{1}{2\pi C_{out}\text{ESR}} = 79.6 - 398 \text{ kHz}$$

The output voltage divider shifts the level of the 15 V output to the required 3 V error amplifier input, resulting in a gain of -14 dB.

Compensating the quasi-resonant converter: The generalized approach to this compensation is to place the first pole at a low frequency, typically around one hertz. Two zeros are then introduced at approximately the output filter break frequency to compensate for its two pole rolloff. A second pole is placed at a fairly high frequency to roll off the loop gain in a predictable manner. Unlike their predecessors, the newer control ICs rarely run out of gain-bandwidth and require this high frequency pole.

Most of the previously described elements can be lumped together into one gain vs. frequency Bode plot of everything except the error amplifier, as shown in Fig. 31. The VFO, power stage and level shifting voltage divider have gains that are independent of frequency, and are easily combined. The output filter section response is then multiplied by the combined gain of the previous calculation. One curve now depicts the entire loop response from the error amplifier output around to its input.

The desired characteristic of the overall loop including its zero dB crossover frequency can be shown in a Bode plot, as in Fig. 32. The E/A compensation network will include two zeros near the output filter break frequency to cancel these two poles. Assume for now that the high frequency pole of this circuitry will be

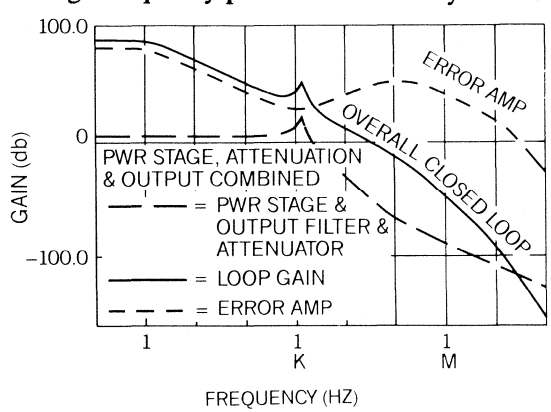


Fig. 32 - Closed Loop Elements

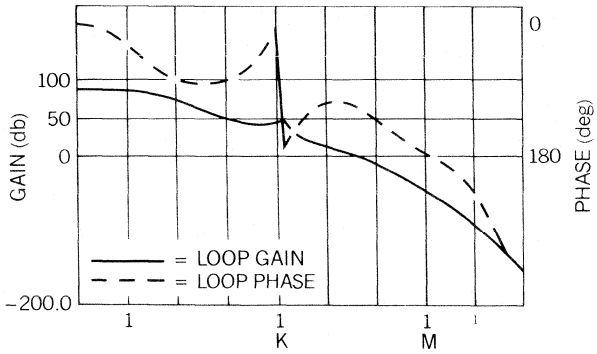


Fig. 33 - Loop Gain and Phase

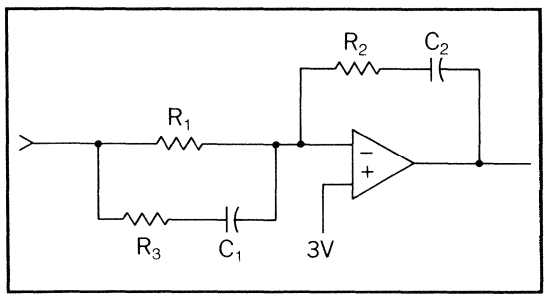


Fig. 34 - E/A Compensation Network

around or above the overall zero dB crossover point. The required error amplifier response can now be approximated graphically from the curve and points plotted.

In this example, two zeros will be introduced in the error amplifier response near the output filter break frequency of 1.25 kHz. A pole is located near the zero dB crossover point at 50 kilohertz. The actual gain and phase obtained in the overall loop is given in Fig. 33.

The error amplifier with its compensation network is shown in Fig. 34. It provides high gain at low frequencies and good transient response.

Zero 1 : $1/(2\pi R_1 C_1)$

Zero 2 : $1/(2\pi R_2 C_2)$

Pole 1 : $1/(2\pi R_3 C_1)$

Max Gain : $R_2/(R_1$ & R_3 in parallel)

Input impedance is the parallel combination of R_1, R_2, and R_3.

The compensation network is designed to produce:

Zero 1 and Zero 2 at 1.25 kHz

Pole 1 at 70 KHz

> 55 dB loop gain at 50 kHz

Using the previous equations and solving:

R_1 = 6.03K R_2 = 78.1K R3 = 100 Ω

C_1 = 22 nF C_2 = 1.7 nF

From the Bode plot of the closed loop response, the supply is compensated to cross 0 dB at approximately 35 kHz, with ample phase margin.

Power Supply Performance

This 150 watt power supply was evaluated while being exercised over various line and load conditions, and exhibited excellent regulation. Response to dynamic loading was well within reasonable limits with little overshoot. Short circuit input current is extremely low, due to the programmed restart delay time constant of 50 milliseconds and soft start of 5 milliseconds.

High efficiency (above 80 %) is achieved over the operating ranges. This is quite respectable for a high frequency, off-line power supply. The power stage was constructed on a double sided printed circuit board used for a previous high frequency example (1.5 MHZ current mode) in 1986.

The control circuit is constructed on the Unitrode UC3860 development PC board. The utilization of a ground plane precedes all circuit layout in megaHertz switch mode power designs, and is incorporated here. Coaxial cable interconnects the gate drive, current sense and output voltage signals between the control and power boards. Observation of the circuit waveforms requires the use of a UHF type scope probe socket, or chassis socket. Any length of ground or hook-up wire will distort the true waveforms.

Summary

Above several hundred kiloHertz, the square wave converter may not be optimal for off line designs. Losses associated with switching high voltages at high currents substantially reduce efficiency, power density and generate much EMI. The need for an alternative solution have resulted in various resonant and quasi-resonant approaches, each with a unique

set of merits, applications and control circuit requirements.

The UC3860 controller has integrated the numerous specific functions and "building blocks" required for resonant and quasi-resonant topologies. Configuration for fixed on-time, variable frequency operation is straightforward, and other adaptations are easily made possible. The uncommitted comparator interfaces well with zero current type switching arrangements. The UC3860's high speed logic, high power outputs and fault protection circuitry combine for an ideal mix of brains, brawn and speed.

REFERENCES

Unitrode Publications:

Unitrode Power Supply Design Seminar SEM-500:

A2 High Frequency Series Resonant Power Supply Design Review

M5 Power Transformer Design For Switching Power Supplies

M2 Winding Data

C1 Closing The Feedback Loop and Appendices

Other Unitrode Papers:

W. Andreycak, "3 Megahertz Resonant Mode Control IC Regulates 150 Watt Off-Line Supply", *High Frequency Power Conference*, 1988.

R. Mammano, "Resonant Mode Converter Topologies", *Unitrode Power Supply Design Seminar SEM600, Topic 1*", 1988

L. Wofford, "UC1860 - New IC Controls Resonant Mode Power Circuits", *Applied Power Electronics Conference,* 1988

Additional References:

P. Vinciarelli, "Forward Converter Switching At Zero Current", *U.S. Patent # 4,415,959*

Intertec Communications Press, "Recent Developments In Resonant Power Conversion", 1988 (628 pages - various papers and authors)

Resonant Circuits - "Rust Remover" and Appendix

The abrupt transition from conventional square wave conversion to a resonant or quasi-resonant approach can be softened by a review of certain fundamentals. Fig. A1 shows the sine and cosine waveforms along with the timing

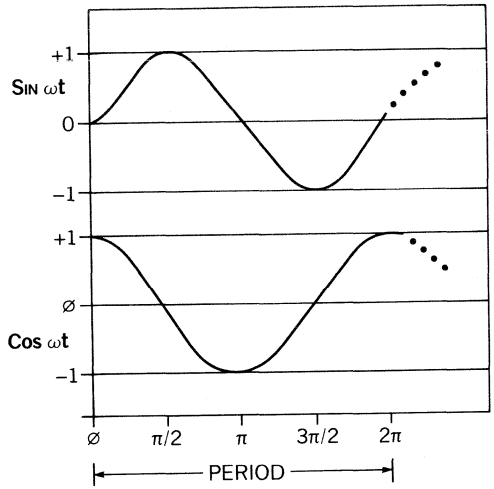


Fig. A1 - Sine, Cosine Relationships

relationships.

$$\text{Frequency} = \omega/2\pi$$

$$T_{period} = 1/f = 2\pi/\omega$$

More specific to power conversion, a series resonant LC network driven by a DC voltage source is presented with its corresponding waveforms and equations in Figs. A2 and A3.

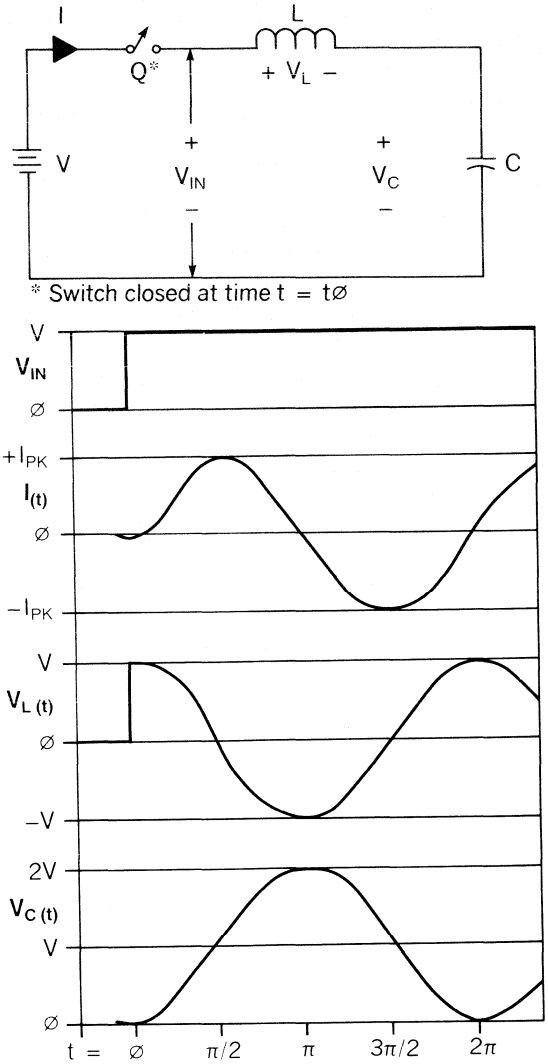


Fig. A2, A3 - Series Resonant Circuit

$$\omega = 1/(LC)^{1/2},\quad Z_r = (L/C)^{1/2}$$

$$i_{pk} = V_{IN}/Z_r$$

$$i = i_{pk}\sin(\omega t) = V_{IN}\sin(\omega t)/Z_r$$

$$v_L = V_{IN}\cos(\omega t)$$

$$v_C = V_{IN}\,[1-\cos(\omega t)]$$

Resonant circuit timing relationships and waveforms: The waveforms of a series resonant, parallel loaded circuit will be analyzed in detail and used to generate the relationships between time, current, charge and energy transfer in a resonant circuit application. Specifically, the buck topology will be used in this example, which can be applied to other topologies and configurations.

The cycle is initiated at time t_0. Switch Q_1 closes, delivering a rectangular voltage waveform to the resonant circuit. The input current rises linearly to I_{out} at a slope equal to V_{IN}/L_r. It reaches the constant output current level I_{out} at time t_1. The time for this to occur is $\Delta t_{10} = (t_1 - t_0)$. During this interval, all resonant inductor current is directed to the output and none delivered to the resonant capacitor, C_r.

At t_0:

$$i_{in} = 0,\ i_{Cr} = 0,\ v_{Cr} = 0$$

From t_0 to t_1,

$$i_{in} = V_{IN}t/L_r$$

At t_1, $i_{in} = I_{out}$

$$\Delta t_{10} = L_r I_{out}/V_{IN}$$

At time t_1, the input current equals the fixed current I_{out}. The resonant L_r & C_r tank components begin their resonant cycle at zero current, and the input current rises sinusoidally to its peak of $I_{out} + V_{IN}/Z_r$. It will later intersect the output current I_{out} again at time t_2, corresponding to 1/2 the resonant tank period, π radians.

At t_1:

$$i_{in} = I_{out},\ i_{Cr} = 0,\ v_{Cr} = 0$$

From t_1 to t_2:

$$i_{in} = I_{out} + (V_{IN}/Z_r)\sin\omega(t-t_1)$$

$$\Delta t_{21} = \pi/\omega = 1/(2f) = 1/\pi(L_rC_r)^{1/2}$$

$$i_{Cr} = \frac{V_{IN}}{Z_r}\sin\omega(t-t_1)$$

$$v_{Cr} = V_{IN}(1-\cos\omega(t-t_1))$$

Once the input (inductor) current crosses I_{out} at time t_2 it continues sinusoidally until it reaches zero at time t_3. At this point, switch Q_1 is turned off to facilitate zero current switching. The time required to reach zero current from

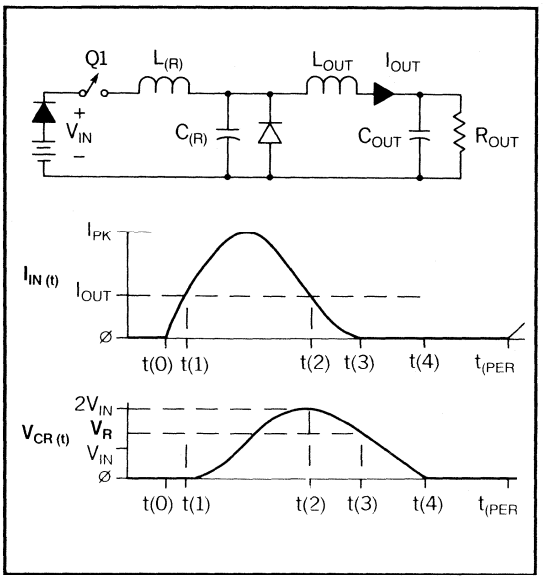


Fig. A4, A5 - Quasi-Resonant Buck Converter

I_{out} is Δt_{32}, and depends upon the amplitude of I_{out} and V_{IN}.

At t_2:

$$i_{in} = I_{out},\ i_r = 0,\ v_{Cr} \approx 2V_{in}$$

From t_2 to t_3:

$$\Delta t_{32} = \frac{1}{\omega}\sin^{-1}\left[\frac{I_{out}Z_r}{V_{in}}\right]$$

$$i_{in} = I_{out} + \frac{V_{IN}}{Z_r}\sin\omega(t-t_1)$$

$$v_{Cr} = V_{IN}(1-\cos\omega(t-t_1))$$

The resonant capacitor voltage v_{Cr} discharges linearly during the interval of Δt_{43}, beginning at time t_3. The capacitor voltage and Δt_{43} are determined from the following equations:

At t_3:

$$i_{in} = 0,\ i_{Cr} = 0$$

From t_3 to t_4:

$$v_{Cr} = v_{Cr(t3)} - I_{out}(t - t_3)/C_r$$

$$\Delta t_{43} = C_r v_{Cr(t3)}/I_{out}$$

Evident from the previous equations is the need to vary the output *on* time to respond to the various line, load and resonant tank circuit influences.

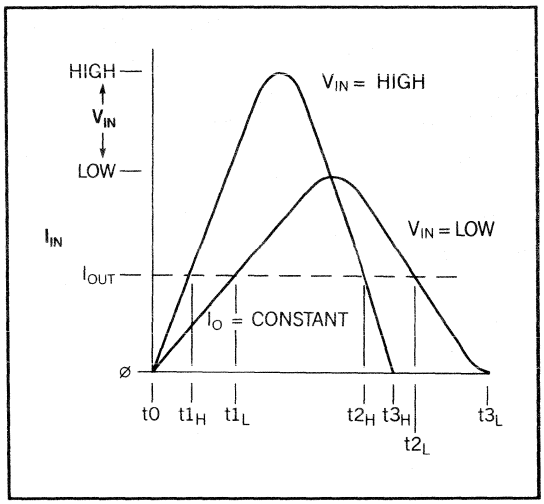


Fig. A6 - i_{in}, t_{on} vs. Line Variation

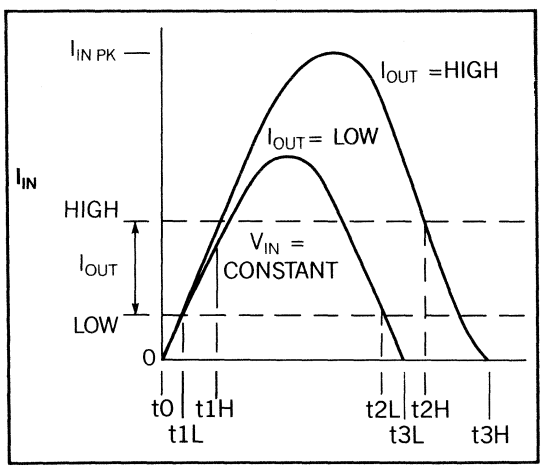


Fig. A7 - i_{in}, t_{on} vs. Load Variation

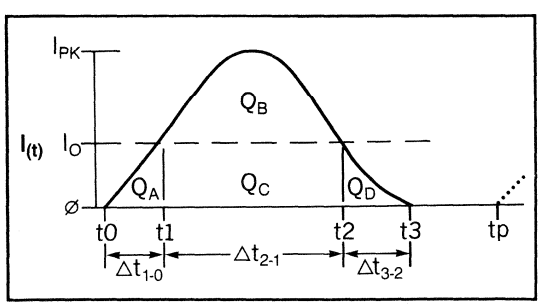


Fig. A8 - Charge Transfer

The conversion frequency or repetition rate at the input switch is approximated following some intermediate calculations for total energy transfer from input to output, as follows:

Charge Transfer in the Resonant Circuit

During each resonant cycle a specific amount of charge (Q) is taken from the input supply and transferred to the output load. The corresponding energy (watt-sec) transferred is simply the charge (Q) multiplied by the input voltage V_{IN}. This relationship will be used to approximate the conversion frequencies required to regulate an output voltage for various ranges of input voltages and output currents.

The input current waveform will be divided into four specific intervals to simplify the calculations. The charge transferred in each interval will be calculated by integrating the current waveform throughout the interval.

Q_a: The charge transferred during the time interval from t_0 to t_1 is calculated from the equation for the area of the triangle formed:

$$\Delta t_{1\text{-}0} = LI_o/V_{IN}$$

$$Q_a = \Delta t_{1\text{-}0} I_o/2 = LI_{out}^2/(2V_{IN})$$

Q_b: During this resonant half-period, the sinusoidal portion of the input current waveform is integrated over the interval t_1 to t_2.

$$i_{in} - I_{out} = (V_{IN}/Z_r)\sin\omega(t-t_1)$$

$$Q_b = \frac{V_{IN}}{Z_r}\int_{t1}^{t2}\sin(\omega(t\text{-}t_1))dt$$

$$Q_b = \frac{V_{IN}}{Z_r\omega}\left[-\cos\theta\right]_0^{\pi}$$

$$1/Z_r\omega = C_r$$

$$\therefore\ Q_b = 2V_{IN}C_r$$

Q_c: The rectangular area of charge delivered to the output during interval t_1 to t_2 is:

$$Q_c = I_{out}\Delta t_{21}, \text{ where } \Delta t_{21} = \pi/\omega$$

$$Q_c = \pi I_{out}/\omega$$

Q_d: The sinusoidal current decreases from I_{out} to zero during the t_2 to t_3 interval. The charge transferred is calculated by subtracting the sinusoidal component from the rectangular region formed by I_{out} and t_3.

$$Q_d = I_{out}\Delta t_{32} + I_r\int_{t2}^{t3}\sin(\omega(t-t_1))dt$$

$$Q_d = I_{out}\Delta t_{32} - \frac{V_{IN}}{Z_n\omega}\left[\cos\theta\right]_{\pi}^{\pi+\omega\Delta t_{32}}$$

$$Q_d = I_{out}\Delta t_{32} - V_{IN}C_r[\cos(\pi+\omega\Delta t_{32}) - \cos\pi]$$

$$\Delta t_{32} \approx (1/\omega)\sin^{-1}(I_{out}Z_n/V_{IN})$$

For practical purposes, this area can be represented by a linear approximation without a significant compromise in accuracy. The area formed by $I_{out}\Delta t_{32}/2$ is a reasonable estimate of the area, resulting in approximately 1% error in the total charge transferred.

$$Q_d \approx I_{out}\ \Delta t_{32}/2 = (1/2\omega)I_{out}\sin^{-1}(I_{out}Z_n/V_{IN})$$

Q_t: The total charge transferred from the input to the output per cycle is the summation of charges Q_a through Q_d.

$$Q_t = Q_a + Q_b + Q_c + Q_d$$

$$Q_t = \frac{LI_{out}^2}{2V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega} + \frac{I_{out}}{2\omega}\sin^{-1}\frac{I_oZ_n}{V_{IN}}$$

The approximation made to simplify the calculation of charge Q_d also allows the substitution of charge Q_a for Q_d, thus reducing the total charge transfer to the following:

$$Q_t = 2Q_a + Q_b + Q_c$$

$$Q_t = \frac{LI_{out}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}$$

Energy Transfer During the Resonant Cycle

The energy per cycle, W, can be calculated by multiplying the input voltage V_{IN} by the total charge Q_t transferred from the input to the output. Dividing the energy per cycle W by the output power P_{out} unveils the conversion period – the inverse of the switching frequency.

$$T_{conv} = \frac{W/cycle}{P_{out}} = \frac{V_{IN}\ Q_t}{V_{out}I_{out}}$$

$$= \frac{V_{IN}}{V_{out}I_{out}}(Q_a+Q_b+Q_c+Q_d)$$

$$= \frac{V_{IN}}{V_{out}I_{out}}(2Q_a+Q_b+Q_c)$$

$$T_{conv} \approx \frac{V_{IN}}{V_{out}I_{out}}\left[\frac{L_rI_{out}^2}{V_{IN}} + 2V_{IN}C_r + \frac{\pi I_{out}}{\omega}\right]$$

Switching Power Supply Components

Unitrode Integrated Circuits
Semiconductor Products
Switch-Mode Capacitors
Micro Networks

TOPIC 3

Switching Power Supply Components

Unitrode Product Spectrum

Linear Integrated Circuits

PULSE WIDTH MODULATORS

- Regulating PWMs
- Advanced Regulating PWMs
- Current Mode PWM Controllers
- Programmable Primary Side PWMs
- High Frequency PWM Controllers

VOLTAGE REGULATORS (THREE TERMINAL)

- Second-Source to Popular Industry Types
- Enhanced Versions of Fixed Regulators
- Adjustable, Fixed, Positive and Negative
- High Efficiency Regulator (<.5V $V_{IN} - V_{OUT}$)
- Military Versions Available

Power Supply Support Functions

- Supervisory Circuits
- MOSFET Drivers
- Isolated Feedback Generators
- Quad Supply and Line Monitors
- High Efficiency Linear Regulator
- Mag Amp Controller
- Low Cost Regulating Controllers Fixed/Adjustable
- Military Versions Available

Unitrode Product Spectrum – Continued

Analog Integrated Circuits
"Specialists in Power Management Functions"

Power Supply Circuits
Linear Regulators
Pulse Width Modulators
Supervisory Functions
Interface Drivers
Special Function Circuits

Unitrode Product Spectrum – Continued

Linear Regulators

Precision Three Terminal:
UC7800A/UC7900A

Adjustable Three Terminal:
UC317/UC337/UC350

High Efficiency:
UC3834/UC3885

Unitrode Product Spectrum – Continued

Pulse Width Modulator Circuits

Conventional PWM:
UC3524 Early dual output
UC3525A/3527A Totem pole outputs
UC3526 Premier Dual output

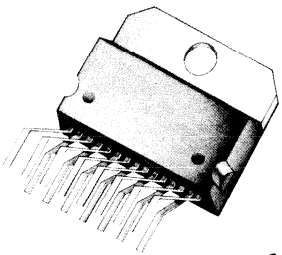
Improved Performance Versions:
UC3524A Easier applications
UC3526A Less circuit delays
UC494A/495A Greater precision

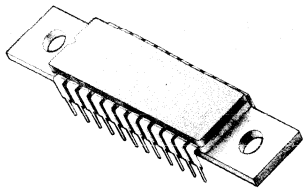
Off-Line Primary Controllers
UC3840/41 Full protection included
UC3842/3844 Low-cost

Current Mode Control
UC3842/3843 Single-ended
UC3844/3845 Single-ended
UC3846/3847 Dual output
UC3825 Current or voltage mode dual output
UC3823 Single ended

High-Frequency Control
UC3823/3825 Megahertz Operation

C Packaging for Power or Size

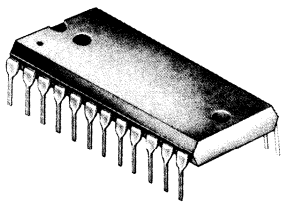


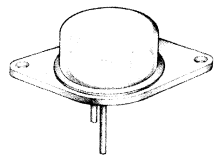


25W
24 Pin DIL
Power Package

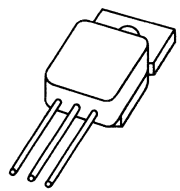
TO-3

25W
15 Pin
Plastic

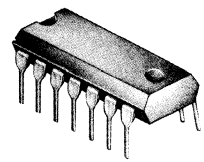




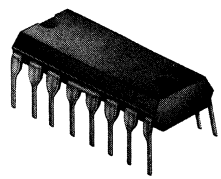
24 or 28
Pin DIL*

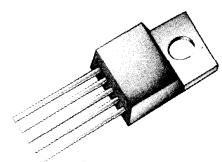


1W 14/16/18
Pin*



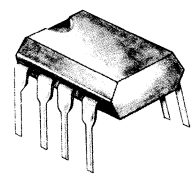
Hermetic
3 Pin
TO-220





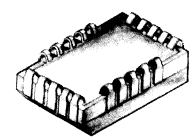
10W
5 Pin
TO-220

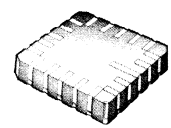
2W
16 Pin Plastic

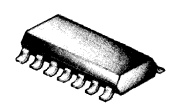


20 Pin
PLCC*

8 Pin
Mini
Dip







20 Pin
LCC*

16/20 Pin
SO (300 MIL)

* 28 Pin LCC and PLCC also available.

Unitrode Product Spectrum — Continued

Switching Transistors and Darlingtons

- Planar Construction
- Metal Can, Plastic Packages
- Up to 300V (V_{CEO}), Up to 10A
- Industrial and Military Versions

Switching Regulator Output Circuits

- Darlington/Fast Recovery Rectifier Combinations (Hybrids)
- Up to 20A, 100V
- Designed and Characterized for Switching Regulator Applications

Unitrode Product Spectrum — Continued

Fast Recovery Rectifiers

- Silicon (UES) and Schottky
- Up to 75A, 60KV
- Axial, Plastic, Metal Can, Modules
- Singles, Duals, Multi-Junctions
- Industrial and Military Versions
- Recovery Times Down to 20 Nanoseconds (Silicon P/N)

Rectifier Bridges

- Standard and Fast Recovery
- Up to 40A, 30KV
- High Performance Industrial and Military Versions

Unitrode Product Spectrum — Continued

Surface Mounted Power Semiconductors

- MELF Package version of Unitrode "A" & "B" Body Components
  - — Products Include Rectifiers, Zener Diodes, TVS Diodes, PIN Diodes
  - — Available Screened to MIL-S-19500
- Power Ceramic Leadless Chip Carriers (CLCC)
  - — Products Include Rectifiers, Schottky Rectifiers, Zener Diodes, TVS Diodes, Transistors
  - — Two (2) Packages: 300 × 300 MIL and 450 × 450 MIL
  - — Available Screened to MIL-S-19500

Custom Packaging

- Most Unitrode Chips Available For Custom Packaging
- Industry Standard Packages
- Unitrode Developed Custom Packages
- Customer Supplied Packages

Functional Modules

- Assemblies of Unitrode Power and Logic Surface Mount Components on a Substrate
- Standard Building Blocks to be Offered
- Custom Designs Available

Switch Mode Capacitors

- Monolithic Ceramic Construction
- Capacitance Values to 100 Microfarads
- Available in DIL, SMT, and Radial Packages

Unitrode Product Spectrum — Continued

Thyristors

- SCRs (Up to 6A, 100V)
- PUTs (Up to 8A Peak, 40V)
- High Performance Industrial and Military Versions

Transient Voltage Suppressors

- Glass Encased Hermetic Packages (Up to 300V, 300W Peak Pulse Power)
- Plastic Packages (Up to 24V, 500W Peak Pulse Power)

Other Unitrode Products

- Standard Recovery Rectifiers (Up to 1000V, 12A)
- High Voltage Assemblies (Up to 6KV, 7A)
- Power Zener Diodes (Up to 400V, 10W)
- Switching and General Purpose Diodes
- Sensistors (PTC Silicon Thermistors)
- High Power PIN Diodes
- Monolithic Ceramic Capacitors
- Motor Control Circuits

Significant New Unitrode Products — Continued

Unitrode Switch Mode Capacitors

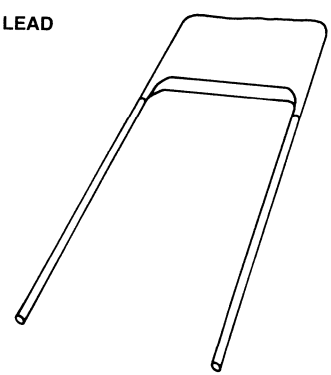
DESCRIPTION

- MLC X7R and Z5U Dielectrics for Input/Output Filtering
- NPO (COG) Dielectric for Resonant Mode Applications
- Ratings from 50 to 500 VDC
- Choice of Package Configurations
- Capacitance Values to 100 Microfarads
- Available with Hi-Rel Screening
  - — DESC Specification 87106 (X7R Types)
  - — DESC Specification 88011 (NPO Types)

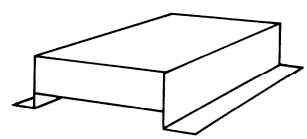
FEATURES

- Extremely Low ESR
- Extremely Low ESL
- High Volumetric Efficiency
- High Ripple Current Capability

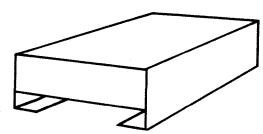
R LEAD



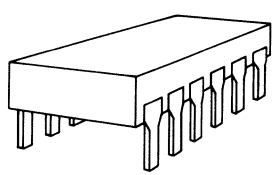
L LEAD



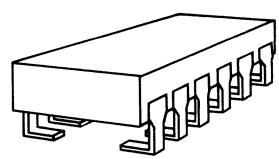
N LEAD



M LEAD



J LEAD



Significant New Unitrode Products—Continued

HVPlus Rectifiers

DESCRIPTION

- Voltage Ratings from 200 to 1000 Volts
- Current Ratings
  - — 2A "A" Body UHVP202-UHVP210 (Industrial)
    1N6620-1N6625 (Military)
  - — 4A "B" Body UHVP402-UHVP410 (Industrial)
    1N6626-1N6631 (Military)
- Trr = 30NS Max (20NS Typ) for Devices to 600V
  = 50NS Max (40NS Typ) for 800-1000V Devices
- Very Fast Tfr
- Vf = 1.6V Max for Devices to 600V
  = 1.8V Max for 800-900V Devices
  = 1.95V Max for 1000V Devices
- Available with MIL-S-19500 Screening (1N6620-31)
- Military Specification to be Generated

FEATURES

- Fastest High Voltage Rectifiers Available
- Optimum Combination of Speed and Vf
- Unitrode Glass Package

Significant New Unitrode Products — Continued

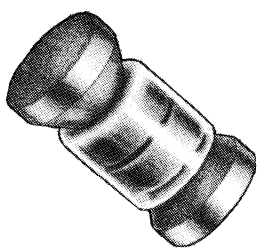
Surface Mounted Power Semiconductors

DESCRIPTION

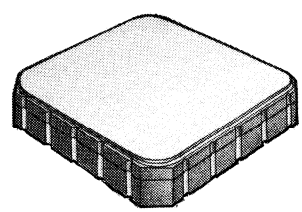
- MELF Package Version of Unitrode "A" & "B" Body Components
  - — Products Include Rectifiers, Zener Diodes, TVS Diodes, PIN Diodes
  - — Hermetic Package with Square Electrodes
  - — Thermal Characteristics Superior to Axial Leaded Devices
  - — Available Screened to MIL-S-19500
- Power Ceramic Leadless Chip Carriers (CLCC)
  - — Products Include Rectifiers, Schottky Rectifiers, Zener Diodes, TVS Diodes, Transistors
  - — Two (2) Packages: 300 × 300 MIL and 450 × 450 MIL
  - — Thermal Impedance to Less Than 0.8C/W (450 × 450 MIL Package)
  - — Available Screened to MIL-S-19500

FEATURES

- Hermetic SMD (MELF & CLCC)
- Pretested Power Components in Standard Packages
- Square Electrodes (MELF)
- Greatly Improved Assembly Yields, (Compared to Chips) in Hybrids
- Very Low Profile (0.1 Inch) for CLCC
- Low Package ESL & ESR



A/B Body Melf



20-Pin PLCC

Significant New Unitrode Products — Continued

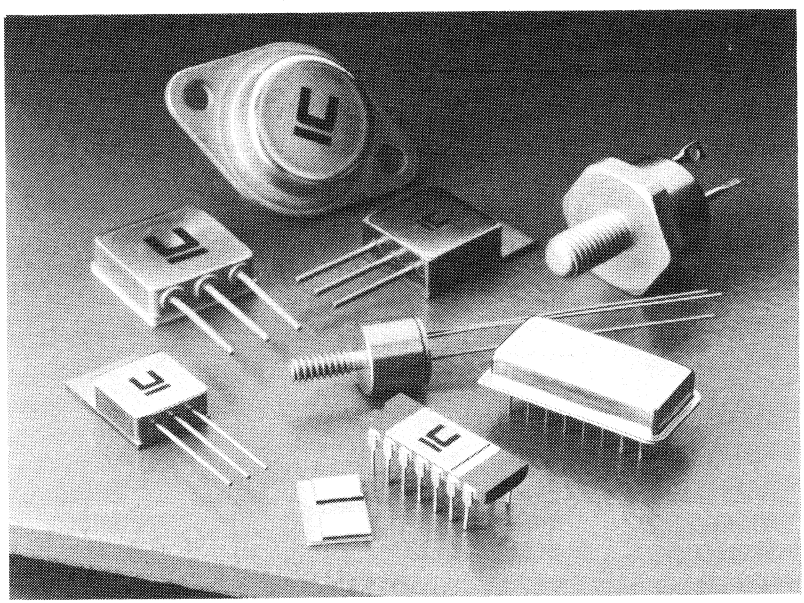
Custom Packaging

DESCRIPTION

- Most Unitrode Chips Available for Custom Packaging
- Industry Standard Packages
  - — 14 Pin Ceramic
  - — Standard CLCC
  - — TO-61
  - — Most Unitrode Catalog Packages
- Unitrode Power CLCC
  - — 300 x 300 MIL
  - — 450 x 450 MIL
- Hermetic TO-220 & TO-247
- Airpax® Power Package (6 to 12 Leads)
- Customer Supplied Packages

FEATURES

- Packaging can be Customized for Specific Customer Requirements
- Packages can be Supplied Mounted on BeO, Alumina or Moly
- High-Rel Screening is Available



Significant New Unitrode Products — Continued

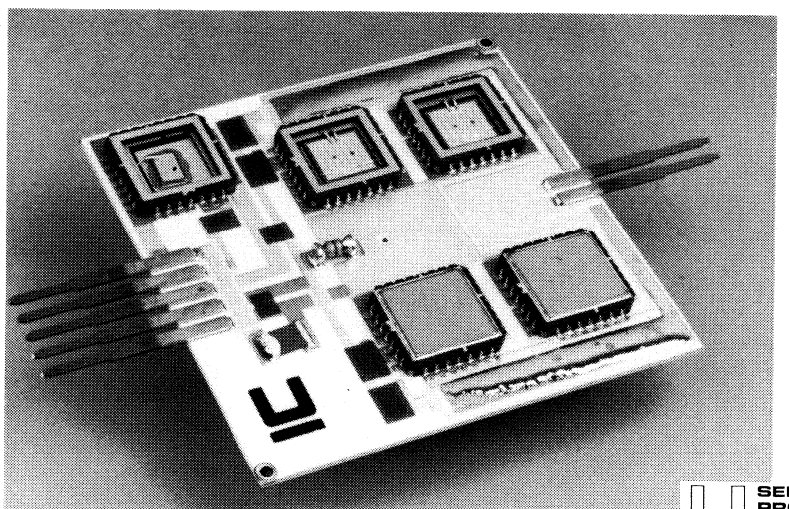
Functional Modules

DESCRIPTION

- Assemblies of Unitrode Power Surface Mount Components on a Substrate
  - — Additional Components Include CLCC IC Control Chips, Film Resistors, Chip Resistors & Capacitors, and Low Profile Magnetics
  - — Available on Alumina and Polyimide Coated Cu-Invar-Cu & Cu-Moly-Cu Substrate
- Standard Building Blocks to be Offered
- Custom Designs Available
- Typical User Designed Circuits Include
  - — Buck Regulators
  - — Half Bridge/Forward Converters/Push-Pull Converters
  - — Crowbar Circuits
  - — H-Bridge Plus Control for Motor Drive

FEATURES

- Low Profile
- High Density
- Thermally Matched Substrate
- Components Individually Tested and, Optionally, Screened Before Assembly
- Lower Cost, Higher Reliability Option to Power Hybrids
- Building Block Approach Reduces Design Time for Power Systems



Significant New Unitrode Products

BISYN™ Synchronous Rectifier

DESCRIPTION

- BISYN is a Bipolar Junction Transistor Optimized to Act as a Fast Recovery High Efficiency Rectifier
- Exhibits Lowest V_F of Any Semiconductor Device at Rated Current (Approximately .3V)
- At Load Voltages Below 5V, The BISYN Has Half The Losses of a Comparable Schottky Rectifier
- Programmable
- Modified TO-3 Package (UBS430), or TO-220 (UBS421)

FEATURES

- Very Low On-Resistance — 7 Milliohms (Typical) at 30A (UBS430)
- Reverse Blocking Voltage = 40V
- Low Temperature Coefficient of On-Resistance
- Can Be PWM Controlled to Provide Regulated Voltage to Load
- Fast Switching Times (T_R, T_F = 120ns)
- High Gain Minimizes Base Losses

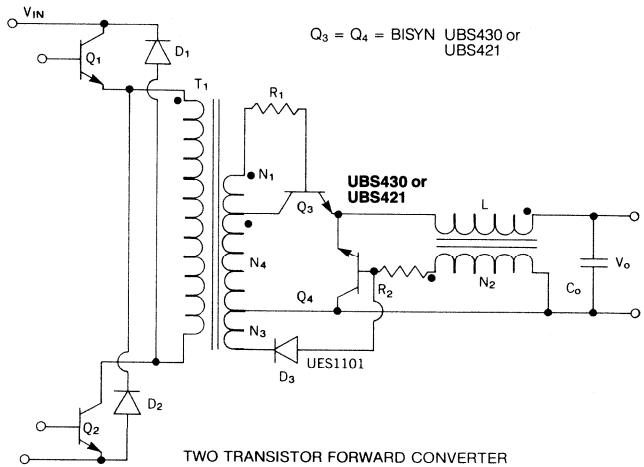
NEW BISYN™ Synchronous Rectifier — UBS421

FEATURES

- Low, On-Resistance — 12 Milliohms (Typical) at 20A
- 20A Continuous Forward Current Rating
- 40V Reverse Voltage Capability
- Cost Effective TO-220 Package

BISYN™ is a trademark of Unitrode Corporation

BISYN™ Typical Application



SEMICONDUCTOR PRODUCTS
UNITRODE

Significant New Unitrode Products — Continued

Low Current Hermetic Schottkys — USD245 Family

DESCRIPTION

- Voltage Ratings to 45 Volts
- Current Rating — 4A
- Three Product Types: Single Chip, Center-Tap and Reverse Center-Tap.
- TO-39 Package
- Available with MIL-S-19500 TX Type Screening.

FEATURES

- First Low Current Hermetic Schottky Product
- Useful as an Output Rectifier, Catch Diode, or in PWM Output Protection.

Significant New Unitrode Products — Continued

Low V_F Schottkys — USD7525 Series

DESCRIPTION

- V_F Only .425V @ 60A, 125°C T_J (Compared to the Industry Standard of .6V @ Rated Load)
- Voltage Ratings to 25 Volts
- DO-5 Package

FEATURES

- Ideal for Low Voltage (Less than 5 Volts) ECL or VSLI Logic Computer Power Supplies
- Reduces Output Power Losses by 30%

Significant New Unitrode Products — Continued

TO-247 Power Plastic Rectifiers

DESCRIPTION

- Product Families Include Very Fast Recovery (<50ns) Silicon PN Junction Rectifiers and Schottky Rectifiers
- Current Ratings up to 45A, Single or Center Tap
- Voltage Ratings up to 45V (Schottky) and 200V (Silicon PN).

FEATURES

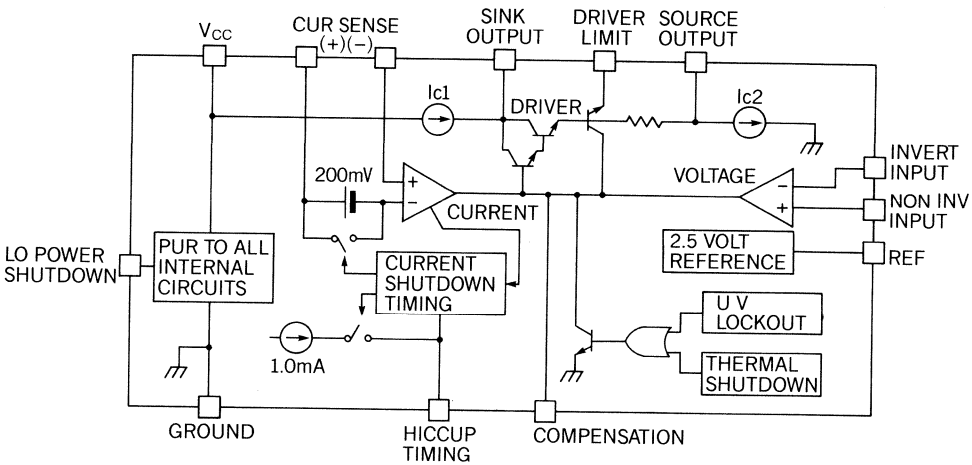
- Preferred Plastic Package (Similar to TO-218 Except has Isolated Mounting Hole and Clip Lead Mounting)
- Broad Product Family (Largest From Any Manufacturer)
- 30% Less Expensive Than Metal Can Equivalents

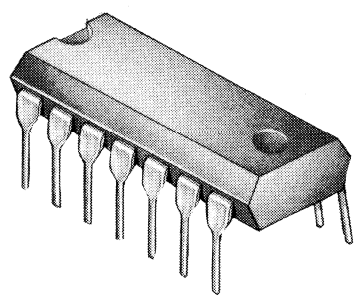
Significant New Unitrode Products — Continued

UC1832 Precision Linear Controller

FEATURES

- Precision (0.8%) Reference
- Current Limiting Accurate to 5%
- Programmable Hiccup Mode Fault Response
- 4.5V to 40V Operation
- Under-Voltage Lockout
- Source or Sink Output Drive
- Max Drive Current Programmable to 200 mA
- Low Current "Off" State





14-Pin Plastic DIL Package

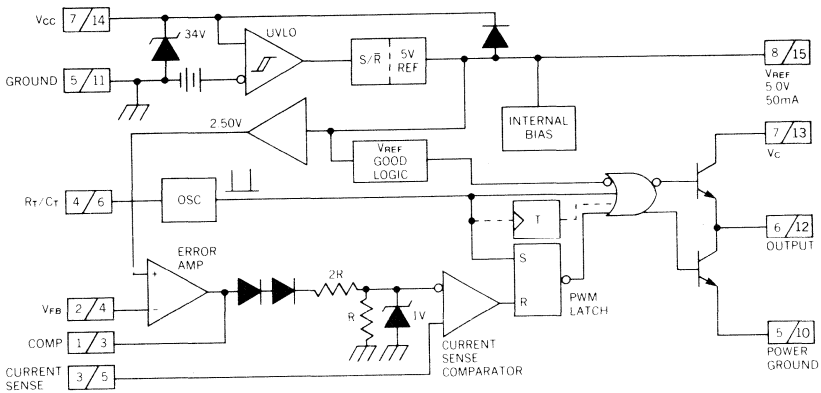
INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products — Continued

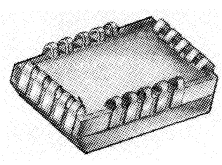
Improved Versions of UC1842/3/4/5 Series
UC1842A/43A/44A/45A

FEATURES

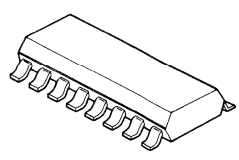
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (<0.5 mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp
- Trimmed Oscillator Discharge Current



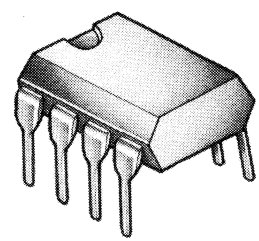
Note: 1. A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
2. Toggle flip flop used only in 1844 and 1845.



20-Pin Plastic PLCC
Q Package



16-Pin Plastic SO IC
DW Package



8-Pin Minidip

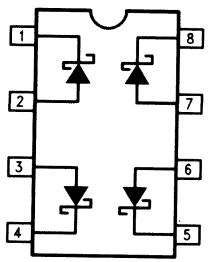
INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products—Continued

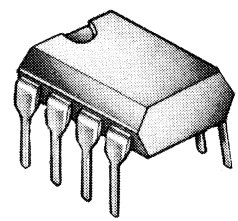
UC3611 Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available
- 3 Amp PK Current
- 50V P.I.V. (Per Diode)

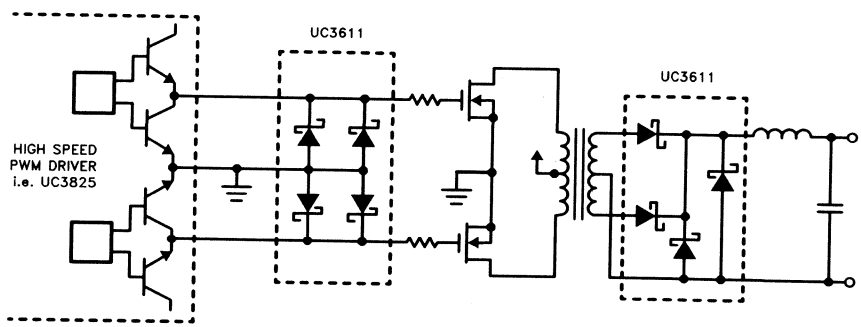


DIL-8 (Top View)
J or N Package



8-Pin DIL Package

Typical Applications



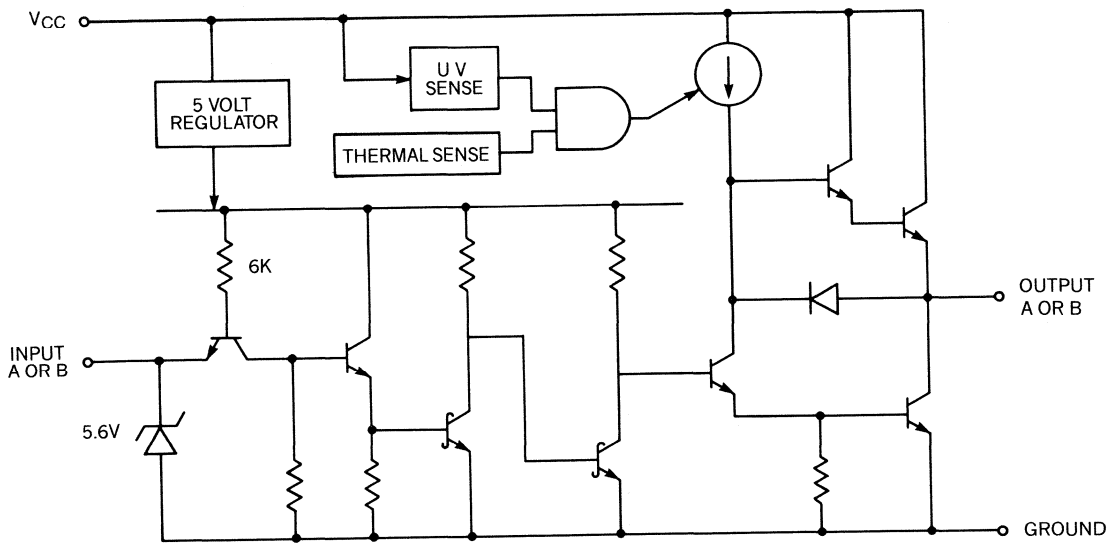
INTEGRATED CIRCUITS
UNITRODE

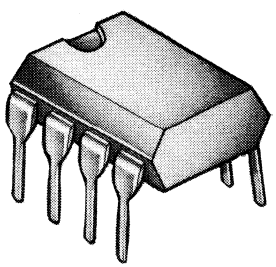
Significant New Unitrode Products — Continued

UC3709 Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection
- 8-Pin Minidip Package





8-Pin Minidip Package

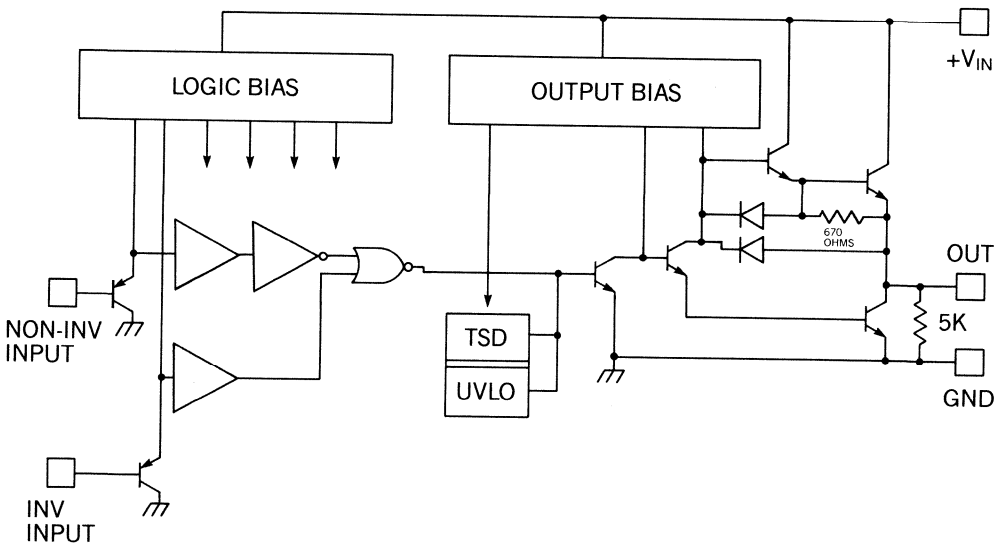
INTEGRATED CIRCUITS
UNITRODE

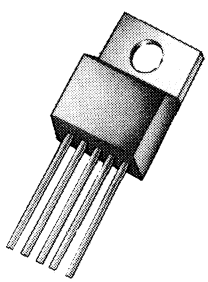
Significant New Unitrode Products — Continued

UC3710 6 Amp Power FET Driver

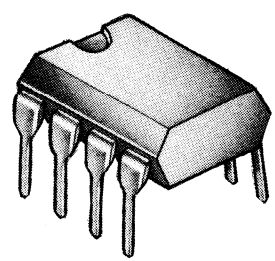
FEATURES

- 10A Drive Capability
- 40 nsec Rise, Fall, Delay (1nF)
- Inverting and Non-inverting inputs
- Under Voltage Lockout and Thermal Shutdown
- Minidip and Power Packages
- Low Saturation Voltage





5-Pin TO-220 Package



8-Pin DIP Package

INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products — Continued

UC3825/UC3823 1 MHz PWM Controllers

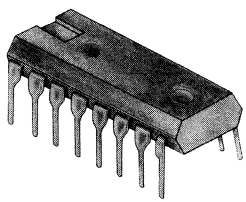
DESCRIPTION

- Optimized for High Frequency SPS Applications
- Can be Used in Either Current Mode or Voltage Mode with Feed Forward
- Totem-pole Outputs
- 16-Pin DIP

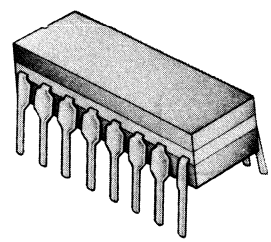
FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation to Frequencies Above 1 MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem-pole Outputs (1.5A Peak)*
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V + 1%)

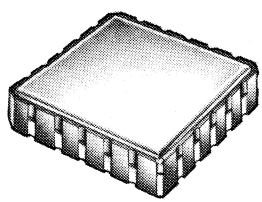
*NEW UC3823 Single-ended version also available



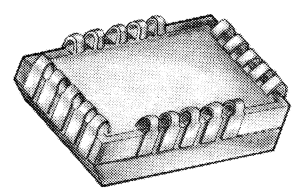
16-Pin DIP



16-Pin DIP



20-Pin L



20-Pin PLCC

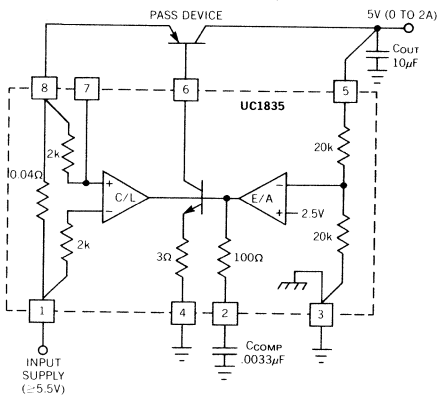
Significant New Unitrode Products — Continued

UC3835/3836 Low Cost High Efficiency Regulators

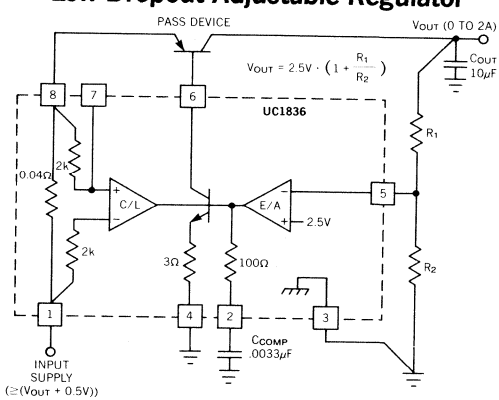
FEATURES

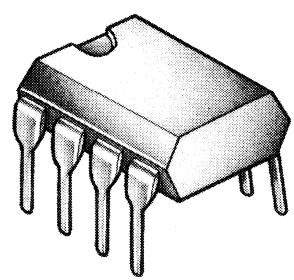
- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- Packaged in an 8-Pin Mini-Dip

UC1835 — Typical Configuration for a 2A, Low Dropout 5V Regulator



UC1836 — Typical Configuration for a 2A, Low Dropout Adjustable Regulator





8-Pin DIP

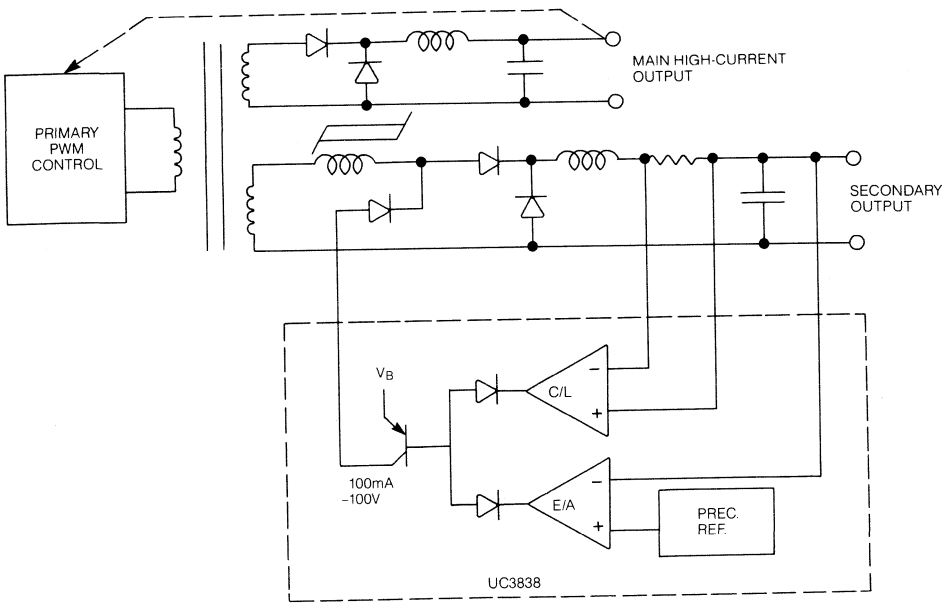
INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products — Continued

UC3838 Mag Amp Control

FEATURES

- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with −100V Capability
- 5V to 40V Analog Operation
- 5W DIL Package



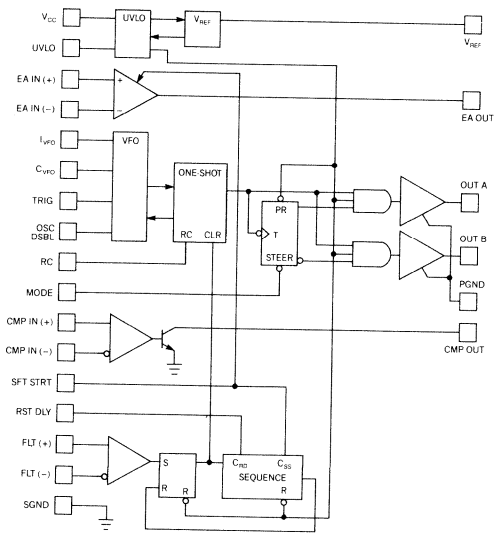
INTEGRATED CIRCUITS
UNITRODE

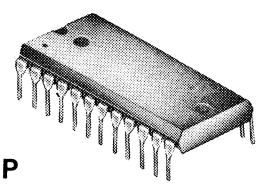
Significant New Unitrode Products — Continued

UC3860 Resonant Mode Power Supply Controller

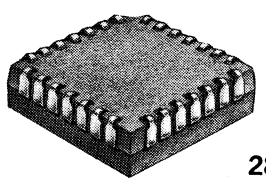
FEATURES

- 3 MHz VFO Linear Over 100:1 Range
- 5 MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator





24-Pin DIP



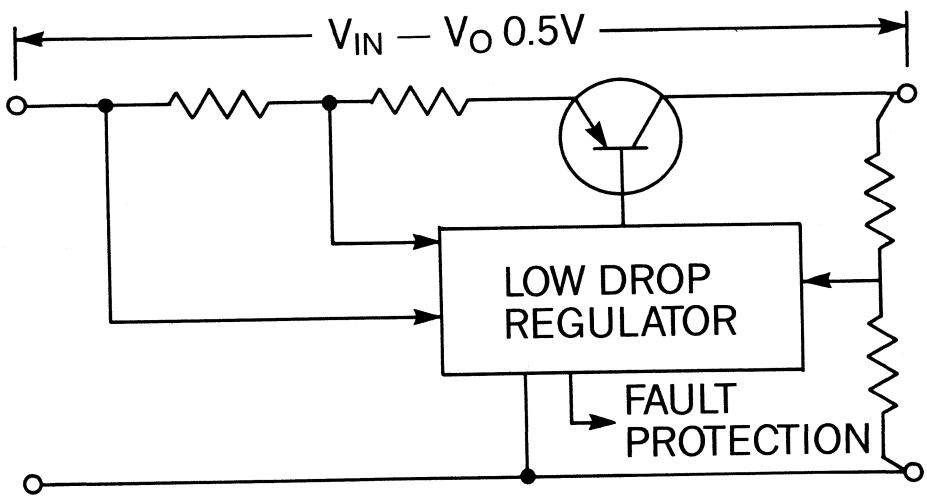
28-Pin PLCC

INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products — Continued

Low Drop Regulator Controllers

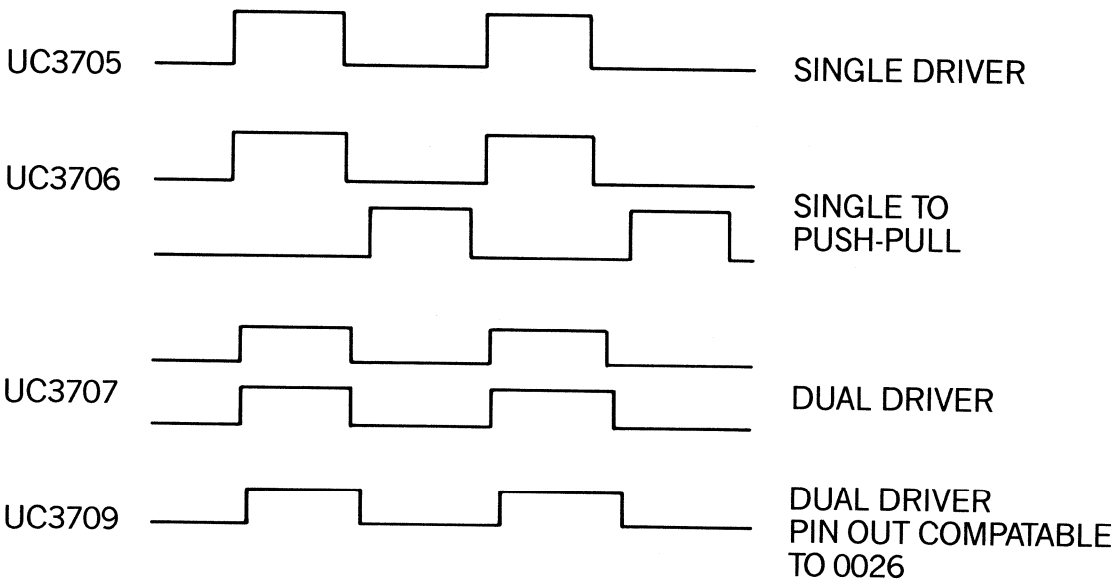
P/N	DESCRIPTION	PACKAGE
UC3834	FULL FEATURE VERSATILE USE	16 PIN DIL
UC3835	LOW COST—FIXED VOLTAGE	8 PIN DIL
UC3836	LOW COST—ADJUSTABLE VOLTAGE	8 PIN DIL
UC3832	PRECISION LINEAR CONTROLLER WITH "HICCUP" CURRENT LIMITING	14 PIN DIL + 8 PIN DIL



INTEGRATED CIRCUITS
UNITRODE

Significant New Unitrode Products — Continued

Power Fet Driver I.C.s



P/N	PEAK CURRENT	RISE TIME	SUPPLY CURRENT
UC3705	1.5A	40NS	8MA
UC3706	1.5A	40NS	10MA
UC3707	1.5A	40NS	12MA
UC3709	1.5A	40NS	12MA

INTEGRATED CIRCUITS
UNITRODE

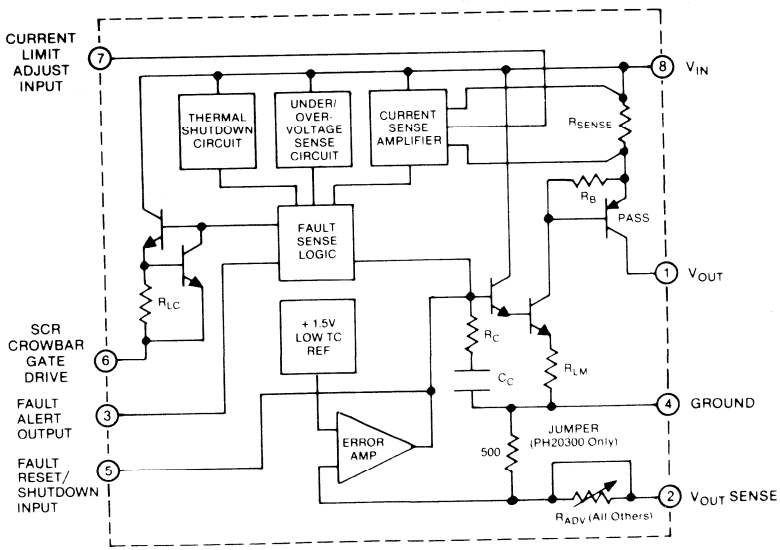
PH20300 SERIES
POWER HYBRID DEVICES

LOW DROPOUT VOLTAGE
POSITIVE OUTPUT
LINEAR REGULATORS

FEATURES

- **5.0A Output Current**
- **Ultra-low Dropout Voltage (0.75V @ 5.0A Output Current) (0.25V @ 2.0A Output Current)**
- **Minimum External Components Required**
- **Short Circuit, Fault and Thermal Overload Protection**
- **40W Power Dissipation**
- **Compact 8-pin TO-3 Package**
- **Output Voltage Set With 1 External Resistor (PH20300 Only)**
- **Output Voltage Adjustment-Free (PH20305 through PH20315)**
- **Electrically Isolated Case**

BLOCK DIAGRAM



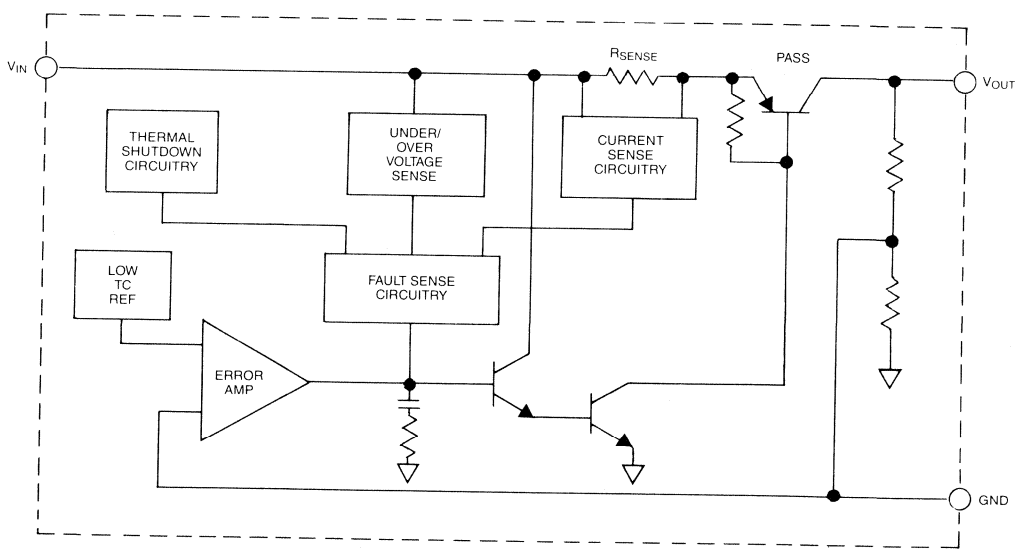
PH20400 SERIES
POWER HYBRID DEVICES

LOW DROPOUT VOLTAGE
POSITIVE OUTPUT
LINEAR REGULATORS

FEATURES

- **Ultra-low Dropout Voltage**
  (0.75V @ I_O =5A)
  (0.20V @ I_O =2A)
- **Hermetic TO-247 Package**
- **Low Thermal Impendance**
  1.3°C/W
- **Fixed Output Voltages**
  5V, 8V, 10V, 12V or 15V
- **Adjustment-free Usage**
- **Electrically Isolated Case**
- **−55°C to +125°C (case)**
  Operation
- **Optional Screening to**
  MIL-STD-883C

BLOCK DIAGRAM



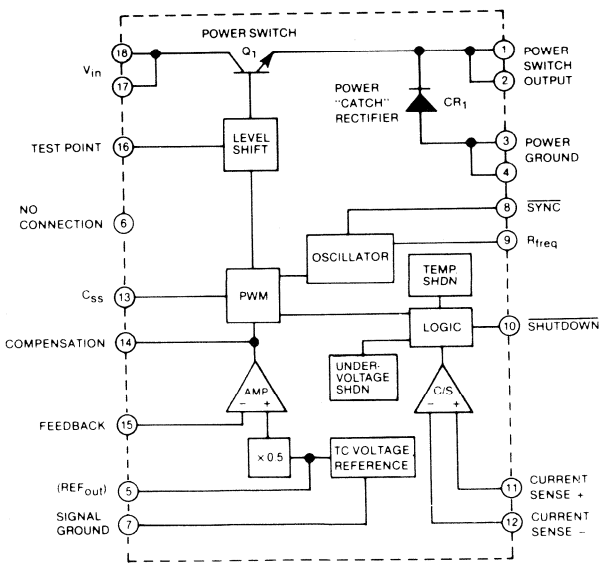
PH22780 SERIES
POWER HYBRID DEVICES

STEP-DOWN (BUCK)
SWITCHING VOLTAGE REGULATORS

FEATURES

- **8A Output Current**
- **Very High Efficiency (80% typ. @ $I_O = 2A$ and $f_O = 20kHz$)**
- **Minimum External Components Required**
- **80V Maximum Input Voltage**
- **Adjustable Output Voltage: 5V to 20V**
- **Pulse-by-Pulse Current Limit Amplifier**
- **Frequency Preset to 25kHz, Adjustable up to 150kHz with 1 External Resistor**
- **Built-In Shutdown, Sync and Soft-Start Capability**
- **Small 18 Pin Metal DIP or Small 18 Pin Power Flatpack**
- **– 55°C to 125°C (Case) Specified Temperature Range**
- **Optional Screening to MIL-STD-883C**

BLOCK DIAGRAM



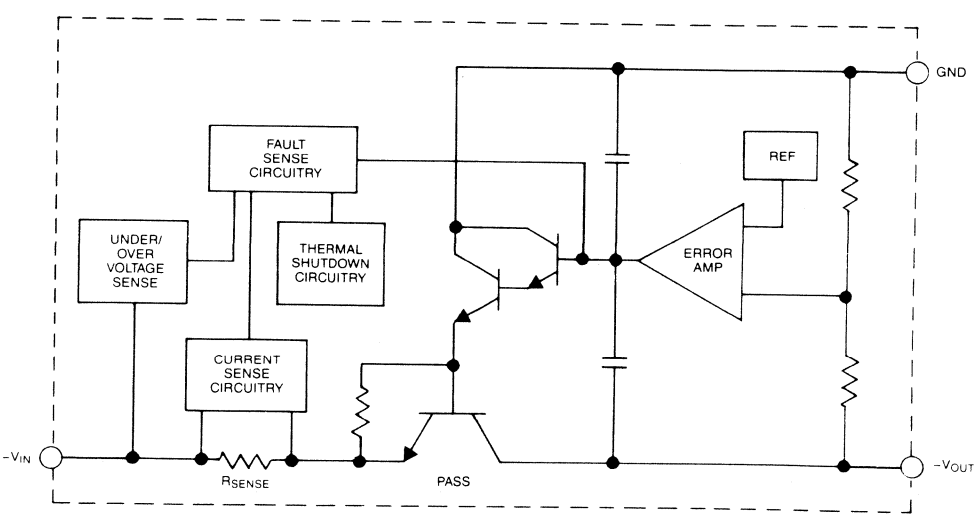
PH21300 SERIES
POWER HYBRID DEVICES

LOW DROPOUT VOLTAGE
NEGATIVE OUTPUT
LINEAR REGULATORS

FEATURES

- **Ultra-low Dropout Voltage**
  (0.75V @ I_O = 5A)
  (0.20V @ I_O = 2A)
- **Hermetic TO-247 Package**
- **Low Thermal Impendance**
  1.3°C/W
- **Fixed Output Voltages**
  −5V, −8V, −10V, −12V or −15V
- **Adjustment-free Usage**
- **Electrically Isolated Case**
- **−55°C to +125°C (case)**
  Operation
- **Optional Screening to**
  MIL-STD-883C

BLOCK DIAGRAM



Multilayer Ceramic Filter Capacitors in Switching Power Supplies

by Duane Clemmer

TOPIC 4

Multilayer Ceramic Filter Capacitors in Switching Power Supplies

Duane Clemmer

Introduction

Capacitors are very important components in switching power supplies. Switcher output filters have traditionally used very large tantalum or aluminum electrolytic capacitors to reduce ripple voltage. Today's higher frequency switching allows the use of smaller values of capacitance. These smaller capacitance values can be utilized in practice with ceramic dielectrics, but not with electrolytics, because the ESR of electrolytics in the areas of interest is too high for proper circuit operation.

Multilayer ceramic technology produces components with capacitance values in the 10 to 100 microfarad range with the ability to handle high rms ripple currents. Ceramics can do this with high reliability because the series resistance is very low, minimizing losses and their attendant heating.

Inductance is a major problem at high frequencies. Capacitor series inductance can be minimized by using multilayer ceramics instead of electrolytics, and also by proper circuit layout, as will be shown.

These characteristics of the multilayer ceramic capacitor make it a near ideal filter element in high frequency switching power supplies.

Purpose

This paper will show some specific practical applications where ceramic capacitors can be used in high frequency switching power supplies. Comparisons of ceramic, tantalum and aluminum electrolytics are given.

Basic switching power supply topologies are analyzed with respect to voltage and current waveforms which appear across the output capacitor. These waveforms are further broken down to show the magnitudes of voltage and current seen by the capacitor's equivalent series resistance (ESR) and equivalent series inductance (ESL) during switcher operation.

A 10 μF multilayer ceramic capacitor with representative values of ESR and ESL is analyzed in the output filter position in buck regulator, flyback and resonant converter circuits. The effects of ESR and ESL on the resultant output ripple voltage are shown under various conditions of load current. Frequency effects on circuit operation are pointed out.

Construction

The multilayer ceramic (MLC) capacitor consists of one or more individual rectangular chips which are connected to external wires or lead-frames, usually with high temperature solder. Each chip is a stack of ceramic layers with metallized electrodes connected in parallel with a low resistivity termination material. The ceramic chip is shown in Fig. 1.

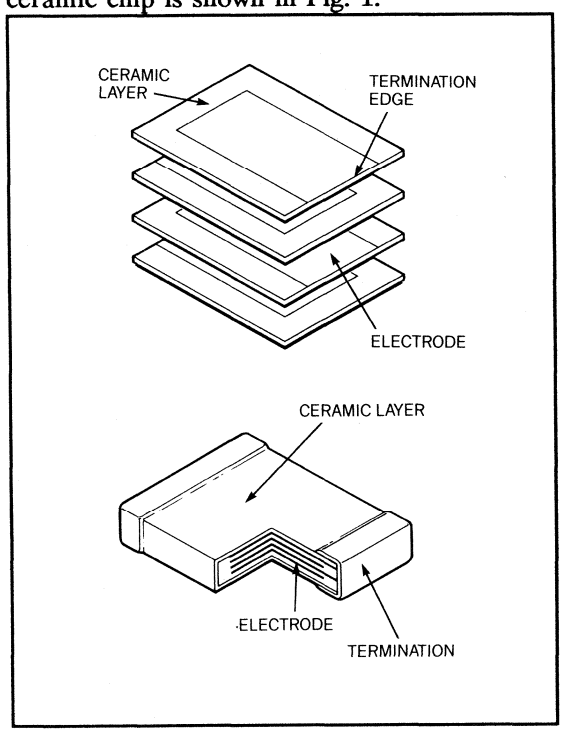


Fig. 1 - Ceramic Capacitor Construction

Electrical Properties of Capacitors

A convenient way to examine the electrical properties of capacitors is by means of a series equivalent circuit as shown in Fig. 2:

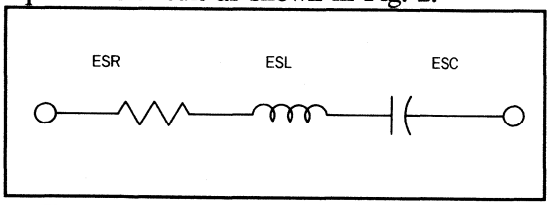


Fig. 2 - Capacitor Series Equivalent Circuit

The equivalent series resistance ,ESR, is composed of several elements, some of which are frequency dependent. The equivalent series capacitance, ESC, and the ESL can be considered constant with respect to frequency, for purposes of this discussion.

Definition of ESR

ESR includes such elements as the resistance of the leads, the electrodes, the capacitor chip terminations and the solder connecting the leads to the terminations. It also includes the resistance of the solder used to connect the capacitor to the power supply circuit. All of these elements of ESR are easily measured, are independent of frequency, and can be considered to represent the true series resistance of a capacitor in the circuit.

But other components of ESR are not so easily defined because they are frequency dependent. The resistive loss within the capacitor dielectric is an example. The parallel or DC resistance of the dielectric and any insulating coating is another. The effects of parallel resistance are negligible under AC conditions in ceramic capacitors, but they are significant in electrolytics to the extent that they adversely affect high frequency performance.

While the true series resistance of any capacitor is constant with respect to frequency, the frequency dependent effects also act as series resistances in that they contribute to heating and power loss in the same manner. So ESR is the summation of all of these effects and must be defined at a specific frequency to have meaning.

ESR and Power Loss

Since ESR is the only dissipative element in the series equivalent circuit, it is what determines power loss and temperature rise of the capacitor in any application. In the case of the output filter application, the capacitor conducts the ripple current, which is the ac component of the output current. The power loss, P, in the output capacitor is:

$$P = I^2R$$

where I = rms ac ripple current, A
R = capacitor ESR, Ω

This power loss is dissipated in the form of heat, which is an important factor in both the operation and the reliability of any capacitor. Capacitors are designed with a temperature rating which takes into consideration the effects of temperature on capacitance, insulation resistance and dissipation factor. All of these parameters will change with temperature. The ESR of ceramic capacitors drops with increasing temperature throughout its range of operation, so that heating effects (power loss in the preceding equation) at a given current level are stable. The ceramic capacitor can then be rated in terms of its rms current capability to assure reliable operation. An important factor in establishing the current rating is the temperature rise measurement of a component. Ceramic capacitors can normally withstand at least 20°C (measured on the outer surface of the device) above ambient without deleterious effect. Electrolytic capacitors, due to their construction, have poorer thermal conductivity than ceramic capacitors. This limits their temperature rise capability. Heat also severely limits the life of electrolytics by increasing the rate of ionic depletion and evaporation of the electrolyte, two inherent characteristics of these devices.[1] It has been estimated that a 10°C increase in temperature will halve the useful life of an aluminum electrolytic capacitor.[2]

ESR Comparison with Electrolytics

The ESR of ceramic capacitors is significantly lower than that of aluminum electrolytics or tantalums. It will be shown that, for ceramics, the ESR is low enough to be negligible in many practical power supply applications. On the other hand, ESR dominates the impedance of aluminums and tantalums at frequencies above 1 to 20 kHz. ESR is in fact the basis for electrolytic capacitor selection in switching

power supplies. Large tantalums or aluminums have been selected for these applications not for the capacitance value, but mainly to obtain an ESR level which will allow the circuit to operate properly.[3] A 10 μF ceramic device will typically exhibit ESR less than 10 mΩ, while an aluminum will require a value of more than 1000 μF in order to approach this same 10 mΩ. Since ESR becomes a limiting factor in power handling capability, it is an important consideration in the choice of the output capacitor in a switching power supply.

Reliability

An indication of the relative reliability of capacitor types can be obtained by comparing failure rates listed in Mil-HDBK-217D. For similar operating conditions at high temperature (85°C, 50% rated voltage, ground mobile environment), the following failures per million hours can be calculated:

Ceramic, general purpose (Mil-C-39014)	.068
Solid tantalum (Mil-C-39003)	.084
Wet slug tantalum (Mil-C-39006)	.218
Aluminum oxide (Mil-C-39018)	.960

Inductance (ESL)

ESL primarily affects high frequency operation. It can be considered constant for any given capacitor since it is a function of size and configuration. So, generally, a smaller capacitor will have a lower inductance than a larger one. Inductance is primarily a function of 1) the loop area enclosed by the capacitor and 2) the conductor spacing. The loop area can be envisioned by looking at cross-sections parallel to the termination leads of a small capacitor and a large capacitor as in Fig. 3.

The cross-hatched area indicates the loop area enclosed by the magnetic field between the leads of the two devices. Note that the large capacitor has a larger loop area due to the larger height dimension, such as might be obtained by placing two chips in parallel. The larger parallel capacitor has consequently higher inductance, which is contrary to the popular wisdom of two inductors in parallel having a lower overall inductance. Another example of inductance would be a length of wire formed into a loop. Fig. 4 shows the same length of wire formed into two different shapes which have much different inductances.

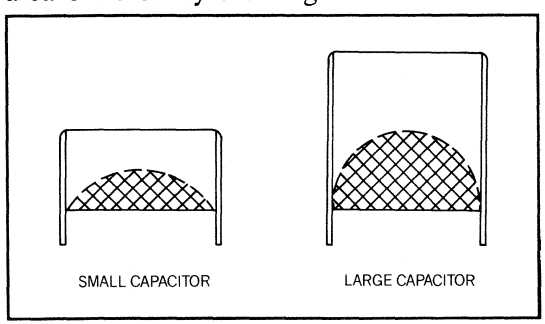


Fig. 3 - Small & Large Capacitor Loop Area

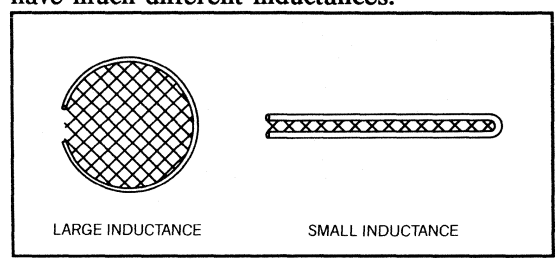


Fig. 4 - Inductance Dependance on Loop Area

The cross-hatched areas again represent the loop areas which are proportional to inductance. The circuit external to the capacitor also contributes significantly to the overall inductance. For example, take the case of a radial-lead flat ceramic capacitor mounted in the usual manner on a PC board. Merely bending the mounted device down to a position flat on the pc board can measurably reduce the inductance due to the smaller effective "loop area" as in Fig. 5. This assumes parallel circuit traces and sufficient board space to do this.

In general, rectangular flat or tab leads are better than round conductors for minimizing the inductance of the capacitor itself. The same principles apply to the layout of the circuit.[4]

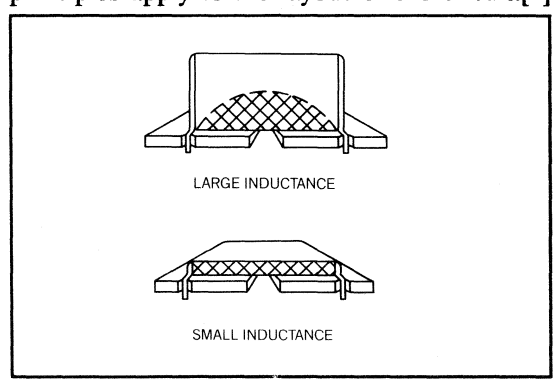


Fig. 5 - Inductance vs. Position

Short, wide ground planes should be used and components should be mounted as close to the ground plane as possible. Circuit leads and traces should be kept as short as possible. Minimize the loop area enclosed by wire carrying high frequency current. When possible, use copper straps/foils for high current. Using capacitors with low inductance and optimizing circuit layout and component mounting with these principles in mind will improve the high frequency performance of the power supply.

Impedance Analysis

A convenient visual way to display the three basic capacitor parameters ESR, ESL and ESC is by means of a plot of impedance versus frequency as in Fig. 6:

The left hand portion of the curve shows the negative slope of impedance due to the effects of capacitive reactance, which is dominant at low frequencies. The right hand portion of the curve is the inductive reactance, which dominates at high frequencies. The dip in the curve at the middle section is the point of series resonance of the capacitor, where the inductive reactance equals the capacitive reactance. At this resonance frequency the impedance is made up entirely of the ESR, since the reactive components cancel each other out. Two curves

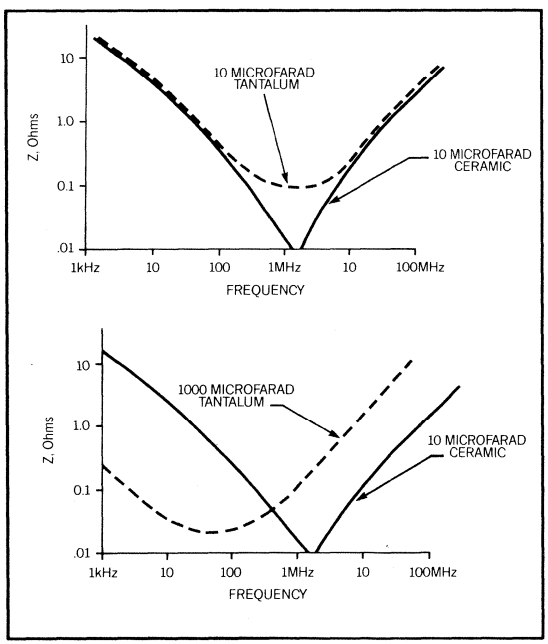


Fig. 6 & 7 - Capacitor Impedance vs. Frequency

are given–one for a typical 10 μF ceramic, the other for a typical 10 μF tantalum capacitor. The comparison shows clearly the difference in ESR.

If a larger tantalum is utilized (say 1000 μF) in order to achieve the ESR level of the 10 μF ceramic, then the curve will look like Fig. 7. Notice how the low frequency impedance is improved (lower) due to the higher capacitance value. The minimum ESR frequency is also lower. But the high frequency impedance is *much worse* because the larger capacitor has inevitably greater inductance. These factors make ceramics more effective than electrolytics for high frequency operation.

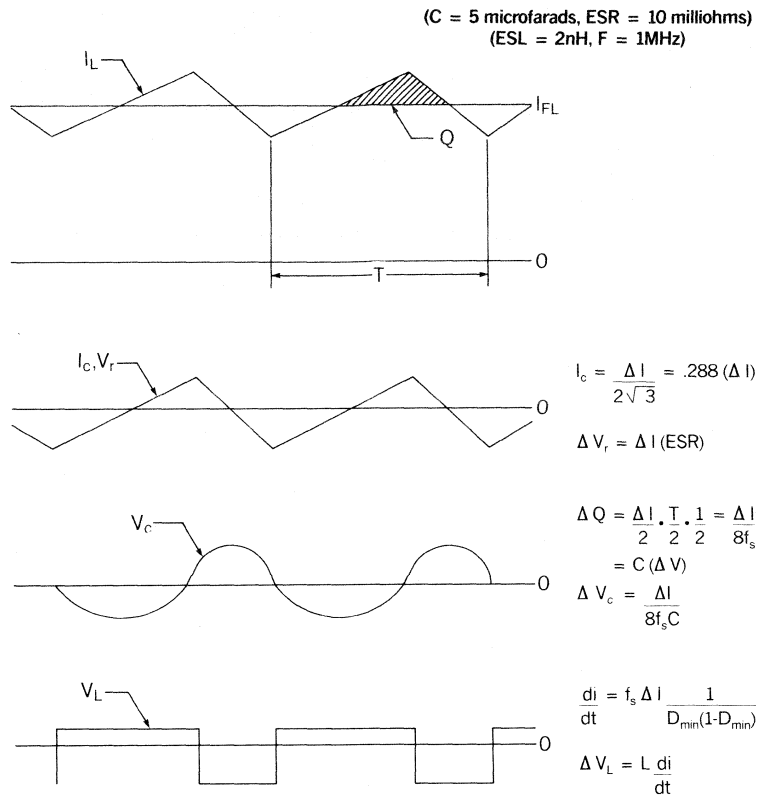
Ceramic filter capacitors are much better able to handle the large high frequency harmonic content of square wave switchers, even at switching frequencies as low as 200–500 kHz.

Power Supply Requirements

Figures 8-11 show the basic waveforms which are found in the output capacitor of several basic switching power supply (SPS) topologies.[5] These represent a cross section of SPS technology and pretty much a min/max situation for the capacitor requirements.

The output capacitor should be considered to be the series circuit composed of ESR, ESL and ESC discussed previously. The voltage and current waveforms are those which would be seen by these three separate elements of the output capacitor. The nomenclature of the subscripts identifying each waveform relate to the particular capacitor element. Thus V_L is the voltage appearing across the capacitor ESL; V_r is the voltage across the ESR, etc. V_c is the basic component of the ripple voltage due to the actual capacitance value. I_{FL} refers to the full load current at the output and the "Δ" terms mean the changes in that particular parameter. The capacitance must be chosen so that the total voltage across the capacitor is within acceptable limits. It is important that V_c, V_r and V_L all be below the desired limits of ripple voltage for satisfactory filtering.

In each topology the calculations use a 5 μF ceramic capacitor for illustrative purposes. It is assumed to exhibit 10 mΩ ESR and 2 nH ESL



Assume $\Delta I = 0.2 I_{FL}$, Min duty cycle (D=0.2)

I_{FL}	ΔI	$I_{c\,(rms)}$	ΔV_r	ΔV_c	ΔV_L
10A	2A	0.6A	.02V	.05V	.03V
20A	4A	1.2A	.04V	.1V	.05V
50A	10A	3.0A	.1V	.25V	.13V

Fig. 8 - Buck Regulator Waveforms

(typical of ceramics). The operating frequency is 1MHz.

Buck Regulator

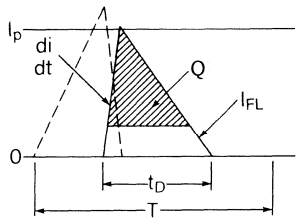
In the example in Fig. 8 the ESR contribution to the output ripple voltage is negligible because ΔV_r is smaller than ΔV_c (See table) and because the two are in quadrature. The only values which change with frequency are ΔV_c and ΔV_L. At 500 kHz ΔV_c doubles and ΔV_L halves. At 2 MHz ΔV_c halves and ΔV_L doubles. The ESL ripple voltage is less than that across the capacitor ESC portion and is not a major factor until frequencies in excess of 1.5 MHz are utilized.

Note also that the rms current seen by the output capacitor is much less than the load current. So a capacitor with as little as a 3 ampere rating is sufficient to handle a 50 A load in this topology.

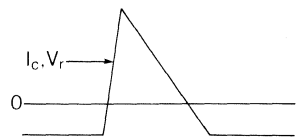
Discontinuous Flyback

Referring to Fig. 9, here again the ESR contributes to no significant voltage effect at any frequency. ESL is more important and ΔV_L will become dominant above 1 MHz. A second stage filter on the output is the most effective way to further reduce ripple.

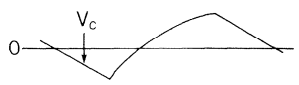
(C = 5 microfarads, ESR = 10 milliohms)
(ESL = 2nH, F = 1MHz)



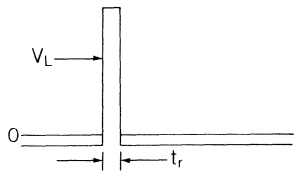
Let $D_D = t_d/T$
$I_{FL} = I_p D_D/2$
$\Delta I = I_p = I_{FL}(2/D_D)$
$I_{(rms)} = I_p (D_D/3)^{1/2}$



$\Delta V_r = \Delta I (ESR) = I_p (ESR)$
$I_{c\,(rms)} = \sqrt{I_{(rms)}^2 - I_{FL}^2}$ (AC only)



$\Delta Q = (t_D I_p/2)(1\text{-}D_D/2)^2$
$= I_p D_D/(2f)(1\text{-}D_D/2)^2$
$= I_{FL}/f(1\text{-}D_D/2)^2$
$\Delta V_c = \Delta Q/C$



$\frac{di}{dt} = I_p/t_r$; $V_L = L\frac{di}{dt} = I_p L/t_r$

Assume $t_D = 0.5T$ ($D_D = 0.5$), $t_r = 0.1T$

I_{FL}	I_{pk}	$I_{(rms)}$	$I_{c\,(rms)}$	ΔV_r	ΔV_c	ΔV_L
2.5A	10A	4.08A	3.23A	0.1V	0.28V	0.2V

Fig. 9 - Discontinuous Flyback Waveforms

Continuous Flyback

ESR is even less a problem in the continuous mode, as shown in Fig. 10. ESC and ESL are of greatest concern.

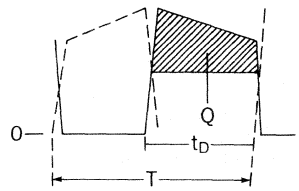
Resonant Converter (Full Wave)

Waveforms that might be encountered in a resonant converter are shown in Fig. 11.

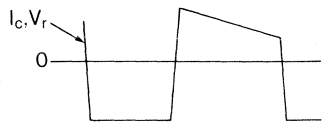
Power Supply Requirements Summary

The preceding calculations show specific examples where a ceramic capacitor can be effectively used as the output capacitor in switching power supplies. By similar means it can be shown that input filters in DC/DC converters can also utilize a ceramic capacitor. Higher voltage, low loss NPO multilayer ceramic capacitors are attractive alternates to mica in high current applications such as resonating capacitors. X7R and NPO ceramics are being utilized in snubber applications. It is even feasible in certain situations to use an economical combination of electrolytic and ceramic capacitors by putting them in parallel to take advantage of the properties of both types. Obviously ceramics will be more important as the operating frequencies get higher and where reduction in size and weight are important. In

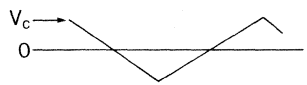
(C = 5 microfarads, ESR = 10 milliohms)
(ESL = 2nH, F = 1MHz)



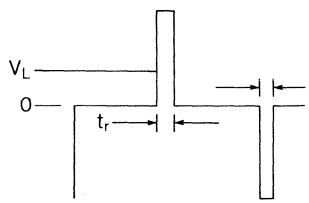
Let $D_D = T_d/t$
Approx. I_p = Avg. peak diode current
$I_{FL} = I_p D_D$
$\Delta I = I_p = I_{FL}/D_D$
$I_c = I_p\sqrt{D_D(1-D_D)}$



$\Delta V_r = I_p(ESR)$



$\Delta Q = (I_{FL}/f)(1-D_D)$
$\Delta V_c = \Delta Q/C$



$\frac{di}{dt} = I_p/t_r$
$\Delta V_L = 2L\frac{di}{dt} = 2I_p\frac{L}{t_r}$

Assume t_D = 0.5T (D_D =0.5), t_r =0.1T

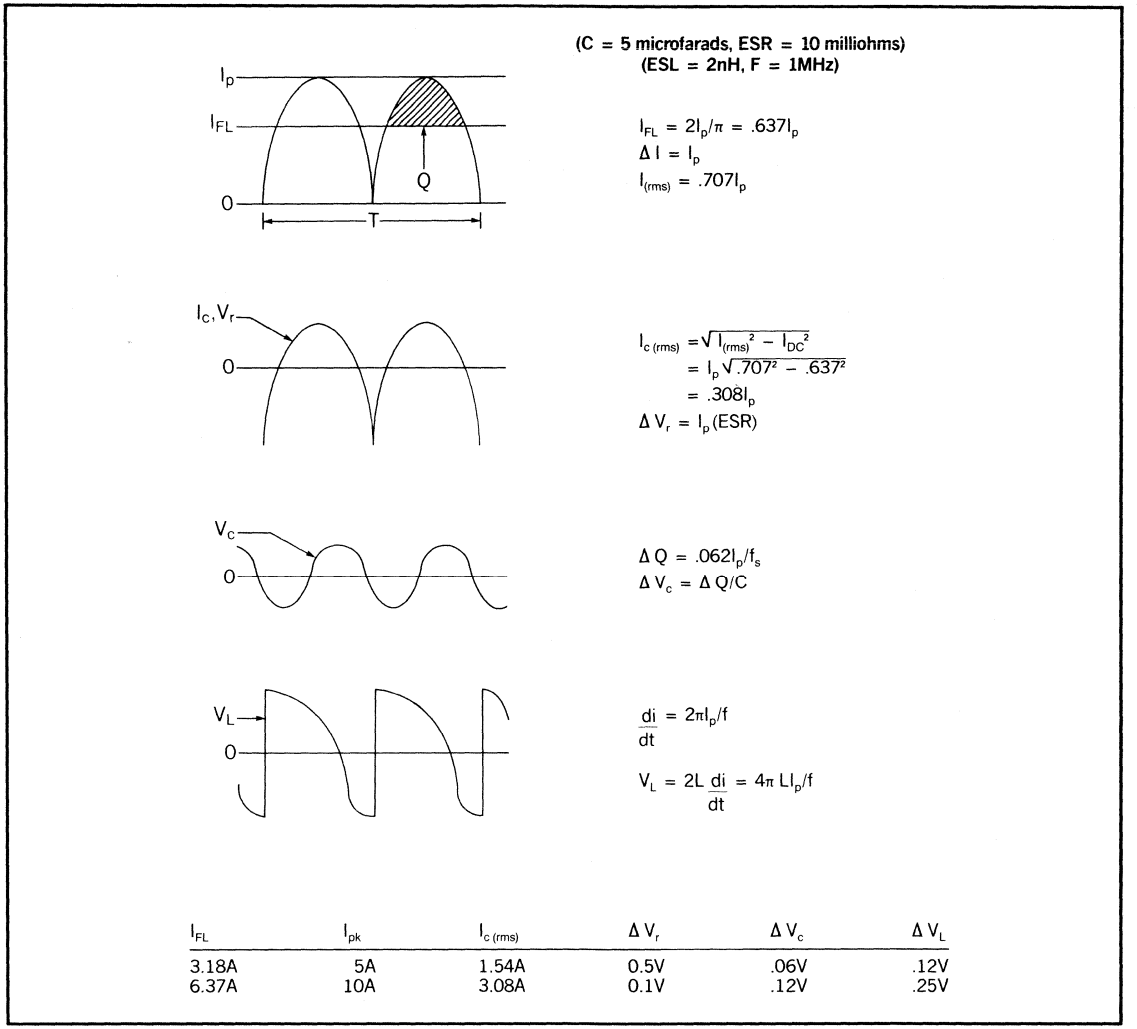
I_{FL}	I_{pk}	$I_{c\,(rms)}$	ΔV_r	ΔV_c	ΔV_L
2.5A	5A	2.5A	.05V	.25V	.2V
5.0A	10A	5.0A	.10V	.50V	.4V

Fig. 10 - Continuous Flyback Waveforms

any practical application, it is necessary to consider not only the steady state conditions, but the effects of a sudden change in load current. Ringing, and voltage overshoot can be problems in certain configurations due to the resonant effects of circuit inductance and capacitance when the load suddenly changes. The extra capacitance usually found in designs with electrolytics (to get the ESR down) can minimize these effects. But to avoid some of the other problems associated with electrolytics other means of accomplishing this can be used. Lowering the inductance of the circuit and the capacitor is one means. Other circuit modifications such as adding second stage filtering can be helpful, as well.

Conclusion

The choice of a capacitor for a specific application should take into consideration all of the points discussed previously. The topology, the size, operating frequency, circuit board layout, ambient operating conditions and the expected switching power supply reliability will be factors. The ESR and ESL advantages of ceramics compared to electrolytics at higher frequencies have been shown. These and other specific electrical properties of ceramic capacitors make them the logical choice in



I_{FL}	I_{pk}	$I_{c\,(rms)}$	ΔV_r	ΔV_c	ΔV_L
3.18A	5A	1.54A	0.5V	.06V	.12V
6.37A	10A	3.08A	0.1V	.12V	.25V

Fig. 11 - Full Wave Resonant Converter Waveforms

many new designs.

References

[1] B. Margolin, "Aluminum Electrolytic Capacitors for Power Supply Applications", *Powertechnics Magazine,* p.14, March 1987.

[2] B. Cordingly, "Ceramic Capacitors in SMPS Output Filters", *PCIM,* p.12, April, 1987.

[3] G. Granath and S. Westerland, "Capacitors for Power Electronics", *Proceedings of CARTS-Europe* 1987, p.60, 1987.

[4] R. Patel and R. Adair, "High Frequency Series Resonant Power Supply- Design Review", *Unitrode Power Supply Design Seminar Manual (SEM-500),* Unitrode Corp., p.A2-8, 1986.

[5] L. Dixon, Jr., "Switching Power Supply Topology Review", *Unitrode Power Supply Design Seminar Manual (SEM-500),* Unitrode Corp., pp. P1-1 to P1-12, 1986.

Selecting and Applying Rectifiers for Optimum Performance in Switching Power Supplies

by Fred Blatt

TOPIC 5

Selecting and Applying Rectifiers for Optimum Performance In Switching Power Supplies

Fred Blatt

Abstract:

Rectifier behavior pertaining to switched mode power supply applications is examined. Characteristics important to rectifier selection and other relevant factors are reviewed in the context of several important applications.

General Perspective

To achieve smaller and less noisy power supplies, switching power converters are being designed with shorter transition times and higher switching frequencies. Historically this has required overcoming various limitations which have impeded progress. These usually appeared sequentially; solving one problem allowed a step-wise advance. Each step might allow increasing the switching frequency or power level until another limiting cause arose. In this process the limiting characteristics of various components have eventually been overcome. Power supply circuits have also been improved and new topologies developed. Some of the advances that have taken place are:

- faster, more efficient bipolar transistors
- high efficiency ultra-fast recovery rectifiers
- power Mosfets
- integrated control circuits
- rugged Schottky rectifiers
- low ESR output capacitors
- surface-mount construction
- resonant converter designs
- high voltage ultra-fast rectifiers

Rectifier Limitations

As switching frequencies increase (and as output power at a given frequency increases), rectifiers may be a limiting component. Their recovery times can impose an extra burden on the Mosfet switch during turn-on. In resonant converters a similar situation may exist, but at much higher frequency. Clamp diodes (in bridge inverters, etc.) and output rectifiers for medium and high voltage supplies can have losses or noisy transient voltages which are more important than DC losses. These problems and their causes are reviewed herein, and some solutions are discussed.

Forward conduction losses: One limitation of swithcing power supply output rectifiers is that of forward losses. In the popular full-wave configuration, rectifiers are conducting either alternately or together at all times. The rectifiers in any buck derived topology, including push-pull and forward converters, conduct the full output current, I_O. Thus the DC loss equals $V_F \cdot I_O$. Forward conduction losses are higher in flyback converters, since conduction is for only a fraction of each cycle so that peak current (and associated V_F) are necessarily higher.

Forward conduction losses limit the overall power conversion efficiency. This is a substantial limitation when the output voltage, V_O, is low. Even a Schottky rectifier, with typical V_F of 0.6V, introduces a loss of 12% of the output power in a 5V supply, 20% in a 3V output. Designs covering the military range of input voltages typically specify a peak inverse voltage rating of 7 times V_O. This limits the use of most Schottkys to 5V outputs--those with PIV above 45V are less popular and have higher V_F approaching the high efficiency, ultra-fast PN junction devices which have the additional benefits of lower reverse loss, lower capacitance and higher operating temperature.

When used in a 15V output, a conventional fast recovery type (1.2V forward) loses 8%; the high efficiency PN loses 5.3%. In higher voltage applications, forward current is usually lower, so this DC loss is of less concern than losses from other components. However, other rectifier losses, transient voltages, and noise generation may be more significant.

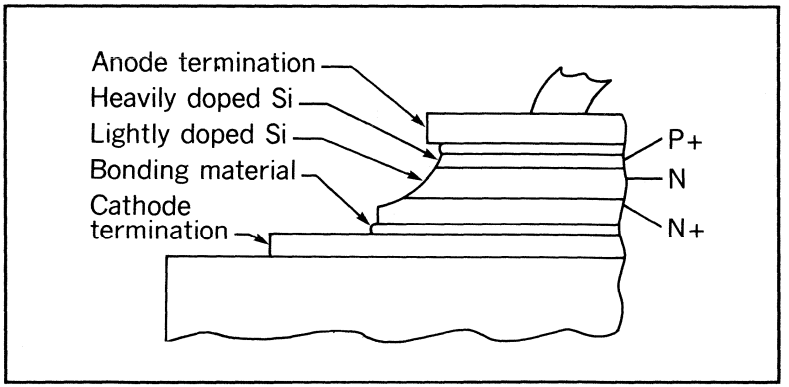


Fig. 1 - Section of Typical Power Rectifier

Reviewing semiconductor rectifier basics: In metals typically used for wiring or interconnections, electrical conductivity is high. Current flows readily because electrons move freely under the influence of a very small electric field associated with a small potential across the conductor.

Semiconductor materials such as silicon have resistivities that are *much* higher than a metal. The high resistance region of a rectifier is shown in Fig. 1 as N type silicon, and in the model of Fig. 5 as "r_v",- a variable resistance. (The N+ and P+ regions in Fig. 1 are heavily "doped" which greatly reduces their resistance.) The resistance, r_v, changes dramatically as a function of applied forward current. When a positive voltage is applied to the P+ (anode) region, minority carriers ("holes" from the P+) are injected into the N layer, greatly reducing its resistance. This mechanism is called "conductivity modulation"--it creates an excess of minority *and* majority carriers in the N region. Semiconductor devices would not be practical without this fundamental benefit.

A penalty must be paid for this benefit, however. The minority carriers contribute a charge, $Q_F = I_F \cdot t_L$, which is stored in the high resistivity N region. This charge must be removed either by recombination or by sweep-out before the device can subsequently achieve a reverse blocking capability. When the forward current (anode +) is terminated, the excess majority and minority carriers will gradually decay by recombining. The time constant of charge recombination is called the "lifetime", t_L, of the minority carriers. This lifetime will depend on the device design and wafer processing. Stored charge removal can be hastened by applying a reverse current to the device. This "sweeps out" stored charge by mechanisms opposite to those which created the charge with forward current flow.

Referring to Fig. 2, both recombination and sweep out are at work during interval t_a if appreciable reverse current, I_{RM}, is present. During interval t_b, recombination is the dominant mechanism.

Reverse recovery behavior: Popular power circuit topologies impose *current* through the rectifier which ramps up and down as a function of external circuit values. The ramp-down in current during the forward to reverse transition is shown in Fig. 2, as well as the resulting voltage across the device. This is an example of the general case where I_{RM} is limited by the rectifier lifetime, rather than by other circuit constraints. The effects of this behavior on a typical circuit (catch diode, output rectifier, high voltage clamp etc.) are discussed by analyzing the waveform in three parts: t_f, t_a, and t_b.

t_f interval: During time t_f, the *circuit* typically switches from forward to reverse polarity but the rectifier will not feel reverse voltage until near the end of t_a. di/dt and t_f are determined by circuit inductance and transistor fall time.

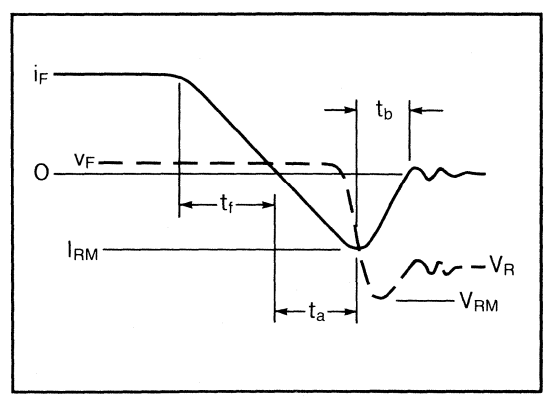


Fig. 2 - Reverse Recovery I/V Waveforms

t_a interval: During t_a the current has reversed, but the rectifier remains a very low resistance. Charge (minority carriers) stored before and during t_f must be swept out before reverse voltage can appear across the device.

During t_a the switch turns on while current is highest (output current plus I_{RM}). In a buck-derived regulator, this occurs with high voltage across the switch, causing high peak power dissipation. It will help to reduce I_{RM} by:

a. Using a faster rectifier (If not characterized under conditions similar to the intended use, be sure to compare devices under identical test conditions), and
b. Increasing t_f. This is done by not turning the Mosfet on any faster than necessary. It is often better to have more power dissipated in the switch and avoid the high I_{RM}.

Keeping I_{RM} low has the additional benefit of reduced snubber needs, lower transient voltage generation, and reducing the switch drive requirements.

With a moderate switching time relative to the recovery time of the rectifier, I_{RM} will be less than I_F. Under these conditions t_a is constant, equal to the lifetime, and not varying with di/dt, or even with I_F if the device temperature is constant. I_{RM} will thus be proportional to di/dt.

Significantly faster switching will make I_{RM} much greater than I_F and approach the condition where Q_a equals Q_F, the charge stored by I_F. In this case t_a will decrease somewhat and, although I_{RM} may be undesirably high, it will not increase as fast as di/dt.

For various switching conditions it is helpful to characterize I_{RM} vs. di/dt (or vs. current rise time), as in the data sheets for the recently introduced UHVP types. Measurements require current sensors with extremely low inductance, otherwise I_{RM} will appear incorrectly high.

t_b interval: The characteristic waveshape, soft or abrupt, as shown in Fig. 3 during t_b, will affect device heating and circuit behavior (generation of transient voltages and circuit noise). The waveshape is influenced by both device design and circuit interaction.

Device effect: Diffusion profiles including concentration gradients, resistivity and width of the high resistance region have a major influence on the t_b value and shape. Soft recovery is more common in high voltage rectifiers, where it is more difficult to implement an abrupt design .

An example of device design for a specific purpose is the "multiplier diode": long lifetime (t_a) and an abrupt characteristic are combined to produce a device capable of shock exciting a resonant tank circuit, which then rings, providing output at a multiple of the pulse driving frequency.

Although soft recovery is desireable relative to damping transients it causes more device heating which in turn increases t_a and I_{RM}. It is important that total dissipation be compatible with available heat sinking to maintain thermal stability.

Abrupt recovery devices have the advantage of dissipating less power during recovery and should thus be operable at higher frequencies than otherwise equivalent soft types. However more electrical noise may require filtering and cause a higher peak voltage, V_{RM}, which must be examined to ensure it will not impair the reliability of the switch or the rectifier by driving them into the breakdown region. These problems are controllable by snubbing; energy is then absorbed in a resistor instead of heating the rectifier, or the snubber energy is partly returned to the circuit.

Whether the goal is a soft or an abrupt characteristic, a trade-off in other features is to be expected--refer to Fig. 3.

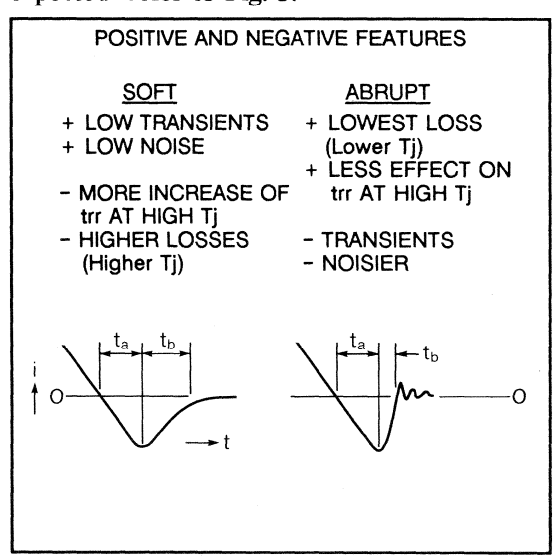


Fig. 3 - Recovery Characteristics and Features

Circuit effect: The circuit layout (loop inductance, other parasitics) influences t_b appreciably; lower inductance decreases it, making the device appear more abrupt. Transients will not increase, however, because less energy is stored in the lower inductance. Ringing frequency, where loop inductance resonates with device capacitance, will be higher.

Measurements of t_b are difficult to duplicate on different test kits. This is partly due to differences in the circuit layout, and to the choice of reverse voltage. Higher voltage results in appropriately higher t_b values. For good test repeatability, reverse voltages of 30 to 50V are often used, even though t_b may be less than expected in high voltage circuits.

TABLE I

Rectifier Power Dissipation during Reverse Recovery

Device Type	A	V	IRM Apk	t_a ns	t_b ns	Total power pulse P_{rr} Wpk	Total power avg P_{rr} Wavg	Reactive power C_j pf	Reactive power P_{xc} Wavg	$\frac{P_{xc}}{P_{rr}}$
UES	2.5	150	1.5	15	5	45	.022	5	.0036	.16
UHVP	2	900	3	30	10	540	0.54	1.5	.039	.072
UES	6	150	4	40	12	120	0.14	15	.011	.077
UES	70	150	7	75	25	210	0.52	150	.11	.21
USD	75	45	6	60	60	54	0.32	4700	.30	.95

Conditions: I_F = rating, di/dt = 100 A/μs.
V_{RM} = 0.8 rated PIV -- no overshoot.
f = 100kHz. Typical t_{rr} such that I_{RM}, t_a, and t_b will be as noted.

Estimating P_D during t_{rr}: Dissipation during reverse recovery occurs during time t_b, causing device heating. It may be computed by integrating the instantaneous recovery power during a typical recovery interval:

$$p_{rr} = \frac{1}{t_b}\int^{t_b} i \cdot v \, dt$$

Approximating with triangular waveforms this simplifies to:

$$\text{Pulse power, } p_{rr} = i_{RM} \cdot v_{RM}/4 \quad (1)$$

$$\text{Avg. power, } P_{rr} = p_{rr} \cdot t_b/T = p_{rr}t_bf \quad (2)$$

where f = rectifying frequency

$$T = 1/f = \text{period}$$

This P_{rr} value is the total apparent power. It includes the energy stored per cycle in the junction capacitance which is returnable to the circuit. In practice this returnable energy is usually dissipated in the transistor and snubber resistor. The power dissipated in the rectifier, P_D, is P_{rr} minus this "reactive power". For PN junction devices this will not be an appreciable part of the total. Table I shows examples for several fast devices, including a Schottky rectifier (USD). The I_{RM} for the Schottky is largely due to its high capacitance.

Note that C_j is dependent on V_R. A reasonable simplification uses $C_{j(avg)} = C_{j(@10V)}/N$, where N = 3 for UES types, 4 for UHVP, and 0.75 for Schottky USD.

$$\text{Reactive power, } P_{xc} \approx C \cdot V^2 \cdot f/2. \quad (3)$$

Snubber design: Snubbers reduce V_{RM}, noise, and device heating. Peak recovery voltage, V_{RM}, is a result of the series resonant circuit composed of device capacitance and circuit inductance. For a Schottky rectifier in a full-wave output circuit, C is C_j and L is the transformer leakage inductance referred to the *full* secondary. In PN junction devices, charge recovered from minority carriers is a major portion of the effective C.

An optimum RC snubber can be designed for critical damping—with a loaded Q_L = 0.5. Using the optimized approach to compute the snubber component values, R_{snb} and C_{snb},

$$Q_L = R_{snb}/X_L = 0.5.$$

where X_L is the inductive reactance.

$$R_{snb} = \frac{1}{2}\left[\frac{L}{C}\right]^{1/2} \quad (4)$$

The snubber capacitor, C_{snb} is used to block the dc voltage present (refer to Fig. 4). Its value should be at least ten times the junction capacitance:

$$C_{snb} = 10 \cdot C_j \quad (5)$$

To transfer the power effectively from the input source to the output load, the time constant ($R_{snb}C_{snb}$) should be less than 1/10 the minimum pulse width of the converter. Since

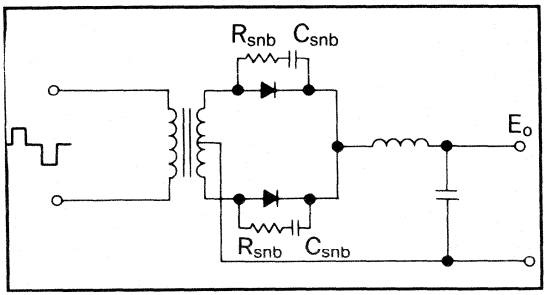


Fig. 4 - Output Circuit Snubbers

this occurs at maximum input voltage, $V_{in\ max}$,

$$R_{snb}C_{snb} \leq (V_{in\ min}/V_{in\ max})/(20f) \quad (6)$$

and the power dissipated in the resistor is, for a half bridge:

$$P_R = \tfrac{1}{2}C_{snb}f(V_{in\ max}/n)^2 \quad (7)$$

where n is the transformer turns ratio. In the general case where L is not known, or with any functional circuit, an experimental approach to defining snubber values may be practical. This is especially true for abrupt PN devices, where t_b is much less than t_a.

However, measuring (transient) V_{RM}, I_{RM}, and t_b can help to implement an optimum design. The loop inductance and effective capacitance, including stored charge effects, can be computed:

$$L = V_{RM} \cdot t_b/i_{RM} \quad (8)$$

From $Q = C \cdot V = I \cdot t$ and simplifying by assuming a triangular waveform,

$$C = \tfrac{1}{2}I_{RM}(t_a + t_b)/V_{RM} \quad (9)$$

This is the effective Cj.

Equations (4) and (5) may be used to compute the snubber values with L and C values from (8) and (9). Some fine tuning may be necessary. The intent is to increase t_b without significantly increasing i_{RM}, thus reducing v_{RM}.

Forward recovery behavior -- cause, effect and optimization: The resistance of a semiconductor diode, in the general steady state case, is dependent on the bias developed by the circuit. Resistance is lowest when conducting high forward current and highest when blocking reverse voltage.

However, if a steeply rising forward biasing current is applied to the circuit, a PN junction device will initially have a high resistance, $r_{(t)}$, the limit of which depends on device design. The forward voltage during this transient interval:

$$v_F = i_{(t)} \cdot r_{(t)}$$

The value of $r_{(t)}$ decreases with time because as soon as current starts to flow conductivity modulation begins. This is the process of injecting minority carriers -- the resistance is lowered very quickly such that the instantaneous forward voltage in many practical circuits often has little, or no, overshoot. The maximum initial $r_{(t)}$ value is:

$$r_{(t)\ max} = \rho \cdot w/A \quad (11)$$

where ρ = resistivity of the lightly doped (or bulk) region.
w = width of the region where the resistivity = ρ
A = area of the plane through the w region.

The complete rectifier model is shown below. During the forward recovery period r_v has a major influence. L_{pkg} and C_j can play an additional, usually minor, role.

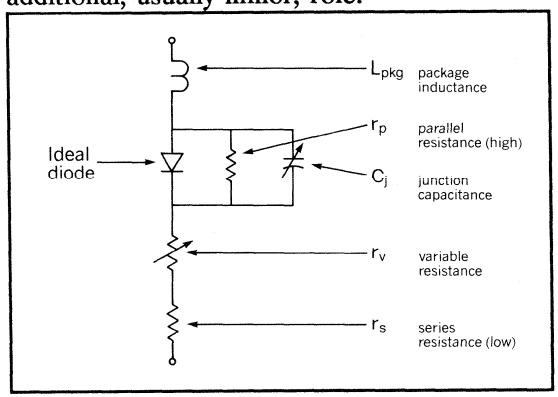


Fig. 5 - Rectifier Model

When the circuit driving forces are significant (high compliance voltage, low inductance and fast switching rate) the current turns on quickly (e.g. over 50 mA/ns) and a transient forward voltage exceeding the usual measured dc V_F value will decay to nearly this dc value during the "forward recovery time". This is usually between 10 and 200 ns, depending on device design. Forward recovery time is usually less than the reverse recovery time, although

not directly related to it. Fig. 6 shows the forward recovery characteristic.

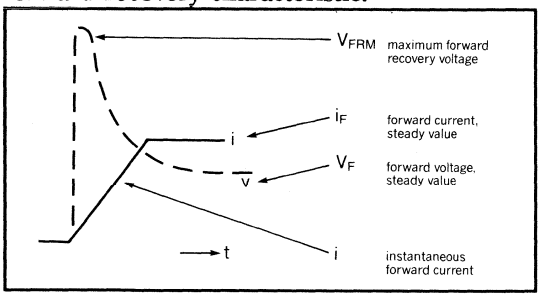


Fig. 6 - Forward Recovery Waveforms

where:

v_{FRM} = maximum forward recovery voltage
I_F = forward current, steady value
V_F = forward voltage, steady value
i = instantaneous forward current

In low voltage, low energy applications, or in circuits with compliance voltage less than v_{FRM}, this phenomenon can even delay the rise of forward current until sufficient charge has been injected (conductivity modulation) to reduce v_F. Generally this condition is limited to fast, low voltage logic circuits or to poorly chosen devices in medium power circuits.

In well-designed rectifier circuits the limiting v_{FRM} is well below the compliance voltage so there is no delay in current rise time attributable to the rectifier. This is even true for most low voltage output circuits (5V), where higher pulsed compliance voltage is available due to the inductance of circuit elements (output inductor, transformer inductances, etc).

Devices with high forward recovery voltage: Equation (11) shows that wide base width and high resistivity worsen the forward recovery characteristic. However, these are device design parameters required to achieve high reverse breakdown voltage. Fortunately these factors can be optimized for particular requirements; This is not normally done for reasons of device standardization and lower manufacturing costs.

It is particularly important to optimize ultrafast reverse recovery, high voltage device types because reducing minority carrier lifetime may significantly increase v_{FRM}. Unitrode recently introduced the UHVP product line, with optimized forward recovery and other features.

Applications likely to have forward recovery problems: Rectifier applications which experience high di_F/dt and which require high reverse blocking voltage capability are most likely to have significant forward voltage overshoot. An example is the clamp diode in an "off-line" half-bridge (or full bridge) inverter, particularly when transistor switches with fast current rise times are used.

Misapplications (usually unintended), where the best device has not been chosen, are also candidates for high v_{FRM}. It is common semiconductor industry practice to "downgrade" devices that are really designed for higher PIV. Also, users seeking high reliability often specify higher voltage devices than required. These practices cause problems not only in the high voltage clamp application—they also generate undesirable transients in low voltage output rectifier and catch diode applications. This, in turn, requires higher voltage switches and/or wider use of turn-off snubbers or transient suppressing components.

Selecting the Best Device

This section focuses on those characteristics which will optimize performance in a specific application. Thus, when there is a range of devices with appropriate current and voltage ratings to choose from, the circuit designer can rank the desireable characteristics for each major usage. First, however, we should review the effects of each characteristic:

- Low forward voltage, V_F. Keeps losses low, and efficiency high—most relevant to high current, low voltage applications.
- Low peak recovery current, i_{RM} , *and* the related (low)
- Reverse recovery time, t_{rr}. Limits Transistor peak drain/collector current and dissipation during turn-on. Important when the diode is reversed directly from

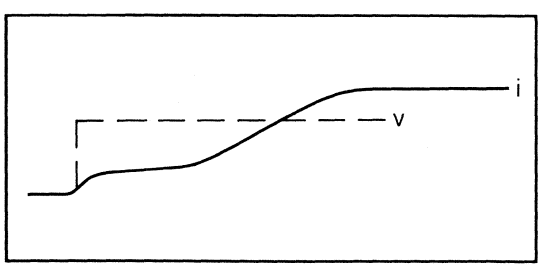


Fig. 7 - Turn-On with Low Compliance Voltage

forward conduction with high di_F/dt.

- Recovery softness factor, RSF, defined as t_b/t_a. High values result in smaller voltage transients and less noise generation but more dissipation; low values give less device heating (most relevant to high voltage applications) but more snubbing may be needed.
- Low forward recovery voltage, v_{FRM}. Limits forward voltage peak when forward current is applied rapidly. Most relevant in clamp functions, especially with high PIV devices and with some ultra-fast types.
- Reverse (leakage) current, I_R. Of concern only at high junction temperature in high voltage applications. The added dissipation may cause thermal runaway or raise the junction temperature to the point where t_{rr} or reliability is undesirable.

Typical applications are shown below. Voltages in common practice are noted, relevant characteristics are ranked, and recommended device families are given.

Device Family Descriptions

UBS: Synchronous rectifier ("BISYN")

USD: Schottky rectifier. USDx45, 1N6391-2, 1N6492. USD7525 is low V_F, 25V.

UES: High efficiency ultra-fast rectifier. Families to 200V & 400V, including 1N5802 – 1N5816, 1N6304 – 1N6306.

UHVP: High voltage (families to 1000V), ultra-fast (35, 50 ns), with low v_{FRM}, low high-temp I_R, and softer recovery than UES. Includes 1N6620 – 1N6631.

Rectifier Comparisons

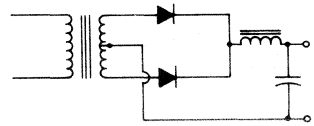
	UBS	USD 25V	USD 45V	UES 150V	UES 400V	UHVP
PIV	5-6	5	4	3	2	1
V_F	1a	2	3	4	5	6
t_{rr}	6	1b	1b	1	2	2-3
V_{FRM}	---	1	1	2	6	3-5
I_R	3	4c	5c	2	6c	1

Grade 1 is best

a. Above continuous IF rating, USD is lower.
b. Effective recovery time for Schottkys.
c. High temp leakage--can result in lower max operating temp. at high voltages.

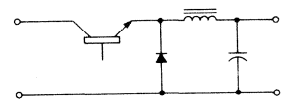
Rectifier Applications

OUTPUT RECTIFIER:



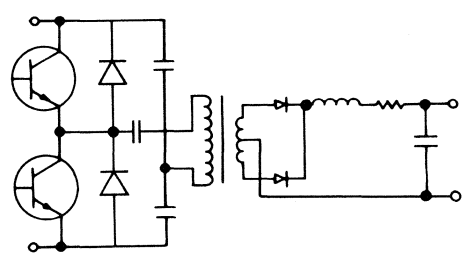
V_{out} = req. PIV:	4V 25	5 45	24 150	48 400	Higher 600+
Rank:	V_F t_{rr}	V_F t_{rr} V_{FRM}	t_{rr} RSF V_{FRM} V_F	t_{rr} V_{FRM} RSF	t_{rr} I_R RSF V_{FRM}
Pref. Types:	UBS USD	USD	UES	UHVP UES	UHVP

CATCH DIODE:



V_{in} = req. PIV:	25V 45+	85 150+	150+ 300+
Rank:	t_{rr} V_F	t_{rr} V_{FRM} RSF	t_{rr} RSF V_{FRM} I_R
Pref. Types:	USD UES	UES	UES UHVP

CLAMP DIODE:

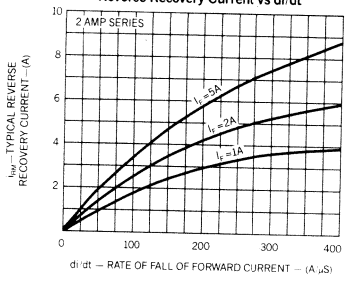


Bus Volts = req. PIV:	350-700V >1.3•BusV
Rank:	V_{FRM} I_R t_{rr}
Pref. Types:	UHVP

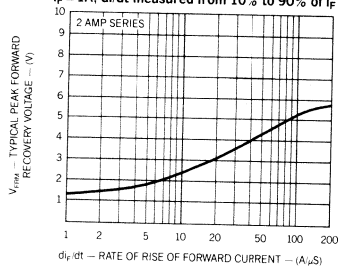
EXAMPLES OF DESIRED CHARACTERISTICS FOR RECOMMENDED DEVICES:

I_{RM}, V_{FRM}, and I_R of 600V, 2A UHVP (AXIAL TYPES)

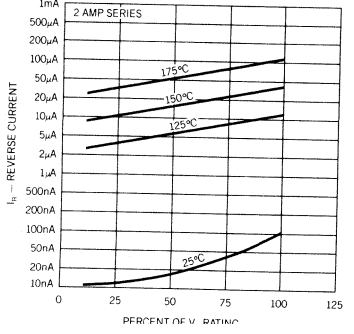
Reverse Recovery Current vs di/dt



Typical Peak Forward Recovery Voltage vs di_F/dt
i_F = 1A, di/dt measured from 10% to 90% of i_F

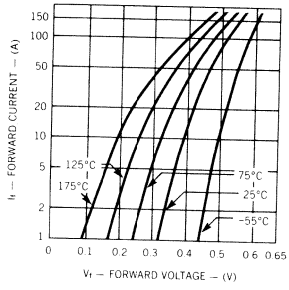


Typical Reverse Current vs Applied Reverse Voltage

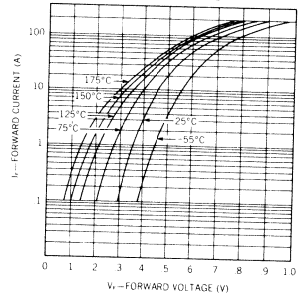


V_F of USD and UBS (CASE MOUNT TYPES)

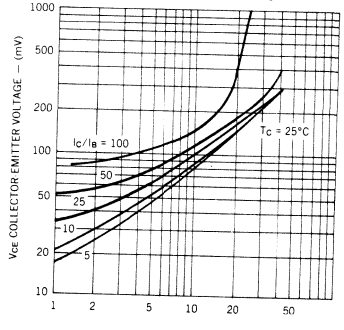
USD 545 **Typical Forward Current vs Forward Voltage**



USD 7545 **Typical Forward Current vs Forward Voltage**



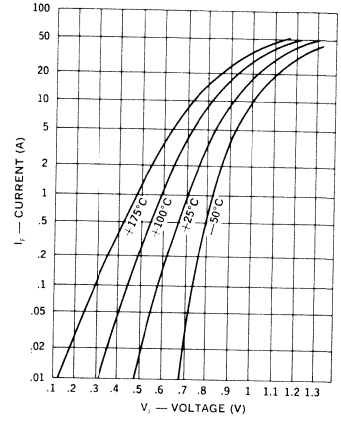
UBS 430 **Collector-Emitter Voltage vs Collector Current at Various Forced Gains**



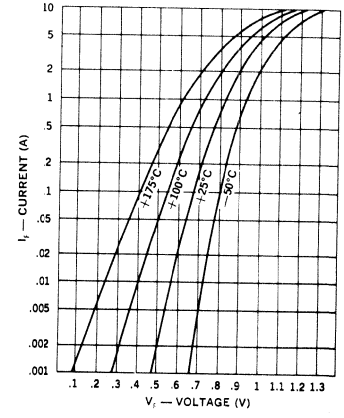
EXAMPLES OF DESIRED CHARACTERISTICS FOR RECOMMENDED DEVICES:

V_F of UES (CASE AND AXIAL MOUNT) and I_R (AXIAL)

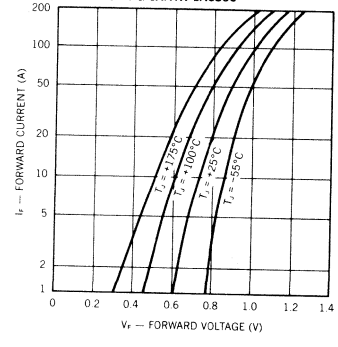
Typical Forward Current vs. Forward Voltage JAN & JANTX 1N5807-5811



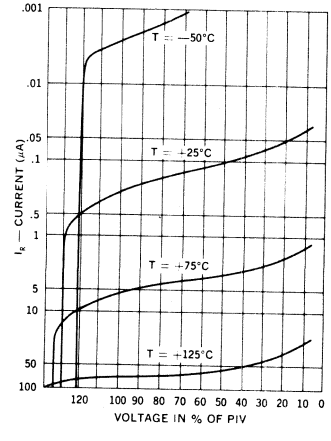
Typical Forward Current vs. Forward Voltage JAN & JANTX 1N5802-5806



Forward Current vs. Forward Voltage JAN & JANTX 1N6306



Typical Reverse Current vs. Voltage JAN & JANTX 1N5802-5806



High Power Factor Preregulator for Off-Line Power Supplies

by Lloyd Dixon

TOPIC 6

High Power Factor Preregulators for Off-Line Power Supplies

Lloyd H. Dixon, Jr.

hpf.wp

Introduction

Off-line switching power supplies usually employ a rectifier bridge or doubler with a simple capacitor input filter to draw power from the ac line. The "bulk" filter capacitor charges to nearly the peak ac line voltage, supporting an unregulated dc bus powering the downstream switching converters. This bulk capacitor must be *large*. It alone supplies total power during most of each half-cycle while instantaneous line voltage is below the dc bus, (or for longer time, depending on hold-up requirements).

Unfortunately, with a capacitor input filter, the line current waveform is non-sinusoidal—a narrow pulse with very high peak current. Input power factor is only 0.5 – 0.65 and the high harmonic content causes line noise. The rms line current may be twice the equivalent rms sine wave. A 120V, 15A line may not be able to supply even 1 kW of input power without tripping the line circuit breaker. With lower wattage systems, perhaps twice as many high power factor supplies could operate from the same line. For these reasons, high power factor is becoming a requirement in many power supply specifications.

The high power factor switching preregulators described in this paper are interposed between the input rectifier bridge and the bulk filter capacitor. Switching at a frequency *much* higher than the line, the preregulator is programmed to draw a half-sinusoid input current, in phase with the line voltage. The current is controlled by the deviation of the dc bus voltage from the desired value. The result is:

1. Improved input power factor: .95 to .999
2. Reduced harmonics (< 3%, if necessary)
3. Tapless/switchless operation over the full 90V – 270V line voltage range.
4. Crudely regulated bulk capacitor voltage. The resulting narrow dc bus voltage range permits the downstream converters to be designed for lower cost and greater reliability and efficiency.
5. Smaller bulk capacitor size and cost.
6. Reduced rms charging current resulting in improved capacitor reliability.

Basic Preregulator Operation

Throughout this paper, a preregulator switching frequency, f_s = 100 kHz, and a line frequency, f_L = 60 Hz are assumed.

Referring to Fig. 1, to achieve an input power factor approaching 1.0, the preregulator is programmed to draw input current which varies in direct instantaneous proportion to the input voltage half sine wave. Thus the voltage and current waveforms on the input side of the rectifier bridge are in-phase sine waves. This is of course what a simple resistive load does, and an active preregulator circuit performing this function is often called a "resistor emulator".

The input current programming signal may be obtained by multiplying a half-sinusoid

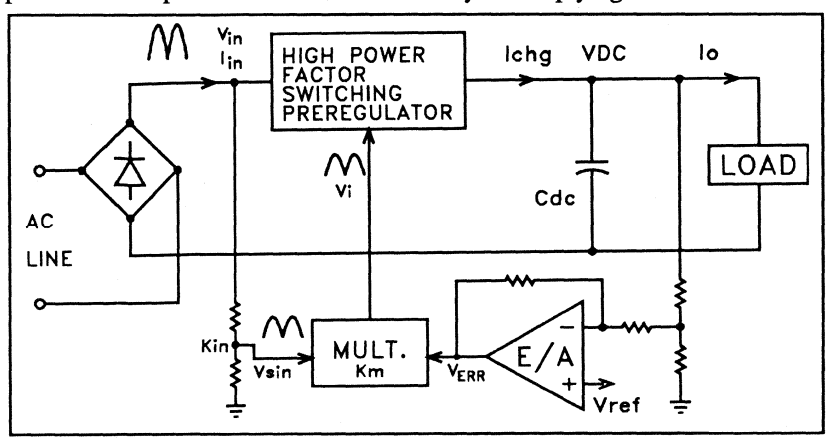


Fig. 1 - High Power Factor Preregulator

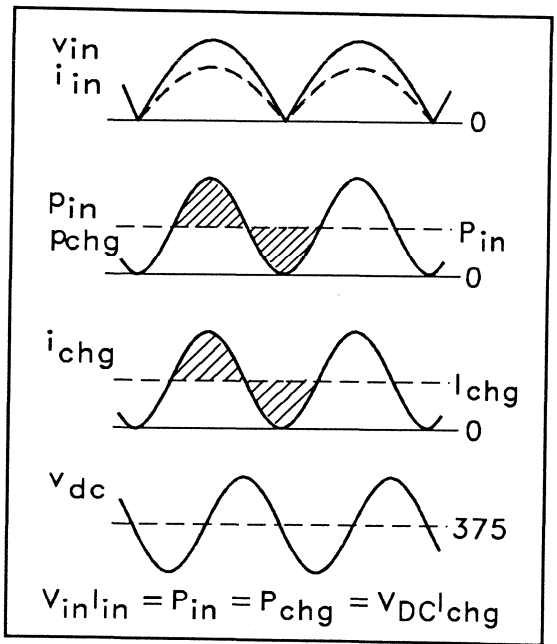


Fig. 2 - Preregulator Waveforms

(usually derived from the rectified line voltage waveform) by a control voltage, V_{ERR}, which must be constant during each half-cycle. Thus V_{ERR} controls the rms input current, governing the power drawn from the line during each half cycle. V_{ERR} represents the deviation of V_{DC} from its desired value, amplified and inverted at the error amplifier output. When V_{DC} is low, V_{ERR} is large, calling for increased input power to make up the energy deficit in the bulk filter capacitor, C_{DC}, across the dc bus.

Power transfer: Although the preregulator input current waveform is a half-sinusoid, its output current i_{chg}, which charges C_{DC}, is a sine squared function (see Fig. 2). Considerable operational insight can be gained by thinking in terms of the preregulator *power input* and *power output*, rather than input/output voltages and currents—see Fig. 2. Assuming the preregulator operates with high efficiency and at a switching frequency very much greater than the line (100 kHz vs. 50-60 Hz), the amount of energy stored or dissipated within the preregulator can be considered negligible at the line frequency. (Inductive energy stored in the preregulator is usually more than the energy transferred during one *switching* frequency cycle, but totally negligible compared to energy transfer during one *line* half-cycle.) Thus on a time scale relevant to the line frequency, the instantaneous power output to C_{DC} equals the power input, and the cumulative energy delivered to C_{DC} during each line half-cycle equals the energy drawn from the line.

With high power factor (1.0), the line voltage and current waveforms are in-phase sine waves, by definition. Thus, during each half-cycle, the instantaneous input power, p_{in}, (and p_{chg}, the power output to C_{DC}) is a $\sin^2$ function:

$$p_{chg} = p_{in} = 2\,V_{in}I_{in}\sin^2\omega_L t \qquad (1)$$

where V_{in} and I_{in} are rms values and $\omega_L = 2\pi$ times line frequency.

Since $2\sin^2 x = 1 - \cos 2x$, then

$$p_{chg} = p_{in} = V_{in}I_{in}(1 - \cos 2\omega_L t) \qquad (2)$$

C_{DC} is usually large enough to hold the dc bus voltage V_{DC} fairly constant. Thus the charging current is nearly proportional to the instantaneous power, and:

$$i_{chg} \approx p_{chg}/V_{DC}$$

$$\approx V_{in}I_{in}(1 - \cos 2\omega_L t)/V_{DC} \qquad (3)$$

$$I_{CHG} = V_{in}I_{in}/V_{DC} \qquad (4)$$

(4) is the average of (3)

As shown in Fig. 2, the ac component of i_{chg} produces a small ripple voltage, v_{dc}, at $2f_L$ (with 90° phase lag) on the dc bus, depending on capacitor size. i_{chg} is not perfectly sinusoidal because the ripple component of V_{DC} makes Eq. 3 an approximation, but the error is negligible in practice.

For a minimal C_{DC} value (providing ½ cycle hold-up), the ripple voltage on a 400 V dc bus will be approximately 10 to 20 Vp-p at full load. If C_{DC} is too small, the dc bus ripple voltage will be larger, but more importantly, bus voltage regulation against line and load changes will be very poor and hold-up capability will be inadequate.

Note that in the entire preceding discussion, the specific power circuit topology was not mentioned. Indeed, the input/output voltage, current and power waveforms and magnitudes are fundamental to the preregulator's task of maintaining good input power factor, charging C_{DC} and regulating the dc bus voltage, totally independent of the specific power circuit used.

Power Circuit Topology

Three basic power circuit topologies—Buck, Flyback, and Boost—that might be used in the high power factor switching preregulator are shown in Fig. 3. Each circuit has its advantages and disadvantages which are summarized in Fig. 4.

Boost topology: This is the most popular HPFP configuration. Boost circuits require that the output voltage, V_{DC}, must always be greater than instantaneous line voltage, v_{in}. A boost circuit designed for a V_{DC} level exceeding the maximum peak line voltage can operate over the full line voltage range, from zero to the max. peak value. V_{DC} of 380–400V allows operation over a span of 90V to 270V rms line without range switching. However, because V_{DC} must exceed v_{in}, the boost topology is not compatible with a standard 300 V_{DC} bus from a 220V line. Unfortunately, a 400V bus requires higher voltage ratings for the devices used in the downstream converters.

In the boost configuration, the input current is not switched and di/dt is low because of the inductor location. This minimizes line noise and EMI. In addition, line spikes are absorbed by the inductor, increasing circuit reliability.

With continuous mode operation, the input location of the inductor also makes it easy to use current mode control to program the input current half sine. (Current mode control actually controls inductor current.)

The circuit location of the transistor switch makes it easy to drive the gate/base, since the source/emitter is referenced to the control circuit and C_{DC} common. The maximum voltage applied to the transistor equals the output voltage, V_{DC}.

Probably the greatest disadvantage of the boost topology is its *inability to limit current*, because there is no series switch between input and output. Overload or startup overcurrent conditions cannot be controlled or limited. While it can be argued that the downstream switching power converters will provide the necessary current limiting to protect the preregulator, failure of the bulk capacitor or converter transistors is not covered.

Furthermore, the boost topology can not function with V_{DC} less than the instantaneous line voltage. This occurs every time the supply is turned on, and after line voltage interruptions of sufficient duration. Soft start is useless because the boost circuit does not function under these conditions. The transistor switch will remain *off*, but input current will rise to a peak value several times greater than normal maximum levels, saturating the input inductor and causing failure unless *additional* current limiting circuits are provided. This will be discussed fully later in this paper.

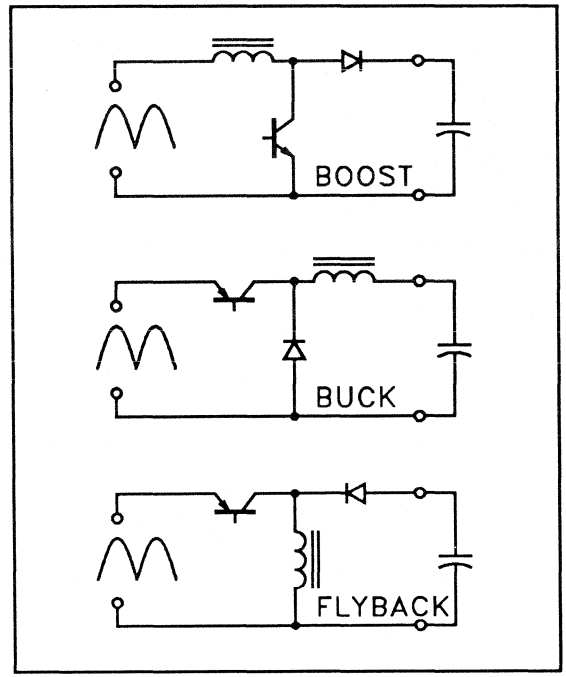


Fig. 3 - Basic Preregulator Topologies

Slope compensation is required with continuous mode operation to avoid instability at duty ratios > 0.5, occurring whenever instantaneous v_{in} is less than $V_{DC}/2$. Slope compensation is difficult to accomplish with the boost topology because the inductor current downslope (which determines the compensation required) varies considerably with v_{in}. This problem can be avoided by reducing the bandwidth of the inner current control loop so that the *average* inductor current is directly controlled, rather than the *peak* current intercept. There is plenty of room to reduce the current loop bandwidth without affecting circuit performance because the switching frequency is so much higher than the line frequency.

BOOST - Constant Frequency, Continuous Mode

ADVANTAGES:
1. Input current is not chopped - little EMI
2. Inductor current *is* input current - current mode control is ideal to program input current waveform.
3. Switch voltage ratings = V_o
4. Inductor at input absorbs line voltage spikes
5. Easy to drive switch - source/emitter at zero ref.

DISADVANTAGES:
1. No control when $V_{in} > V_o$ - start-up, line overvoltage
2. Cannot limit overcurrent - load fault, start-up.
3. V_o higher than max. peak V_{in} requires higher voltages in downstream converter.
4. Slope compensation required - changes with V_{in}

BUCK

Unsuitable for high power factor preregulator except as supplement to Boost preregulator for current limiting.

FLYBACK - Constant Frequency, Continuous Mode.

ADVANTAGES:
1. V_o can be greater or less than peak V_{in}
   a. 300V bus - eases voltage requirements of downstream converter.
   b. Can control start-up current inrush and load fault.
2. Easy to provide isolation in preregulator rather than in downstream converter transformers.

DISADVANTAGES:
1. High switch voltage ratings: $V_o + V_{in}$
2. Chopped input current - hard to filter - EMI
3. Difficult to program input current half sine with current mode control
4. Slope compensation required

Discontinuous Flyback — PRO'S & CON'S
1. Automatic current half-sine by programming and fixing the "on" time during each line half-cycle.
2. No slope compensation required.
3. Peak current nearly twice continuous mode flyback

Fig. 4 - Preregulator Topology Advantages/Disadvantages

The discontinuous inductor current mode is impractical for the boost topology in the high power factor preregulator because at peak V_{in} the inductor current downslope is very shallow, so ripple current is small. But in a high power factor preregulator at peak V_{in}, line current is at its peak. With high peak current but low ripple, inductor current must be continuous.

Buck Topology: In the buck configuration, V_{in} must be greater than V_o. This makes it unsuitable for high power factor preregulator use because it cannot function on the skirts of the input half sine when v_{in} is less than V_{DC}. However, the buck topology can be very useful to provide current limit support to a boost preregulator.

Flyback Topology: The flyback (buck-boost) configuration overcomes two of the boost topology disadvantages: The flyback circuit can control and limit start-up inrush current and load overcurrent. Also, the output voltage may be *greater or less* than the instantaneous input voltage, making it possible to provide a 300V bus from a 220V rms line.

In the basic flyback circuit, output voltage must be opposite in polarity from the input voltage. This may be inconvenient. But the circuit location of the inductor provides a unique possibility for the flyback: the inductor could have primary and secondary windings. This can provide polarity independence and also input-output isolation in the preregulator, relieving the downstream converters of this isolation requirement. The converter transformers can be simplified and leakage inductance reduced because creepage and insulation are eliminated. Isolated feedback can also be eliminated in the downstream converters, making it easy and inexpensive to achieve good regulation.

However, the chopped input waveform of the flyback circuit results in more noise and EMI than the comparable boost topology, requiring more input filtering.

The location of the transistor switch makes it difficult to drive the gate/base—a small drive transformer is normally used.

The transistor voltage rating must be greater than max peak $v_{in} + V_{DC}$, much higher than with the boost configuration.

Finally, it is more difficult to program the required input current half-sine wave with the flyback preregulator and current mode control. This is because current mode control actually controls *peak inductor* current, which is almost the same as the *average inductor* current with continuous mode operation (with any topology). The inductor current *is* the input current in the boost topology, but not in flyback circuits. The relationship between flyback input current and inductor current changes considerably with v_{in}, which complicates input current programming. Also, slope compensation is required with continuous mode operation.

Both of the above problems can be overcome by using *average input* current mode control, sacrificing some current loop bandwidth, as discussed earlier with the boost circuit.

Discontinuous mode flyback: Input current can be easily programmed in the constant frequency, discontinuous operating mode if the "on" time, or duty ratio, is made proportional to the control voltage, V_{ERR}. Peak and average currents at 100 kHz will then be proportional to the instantaneous line voltage waveform, automatically providing high power factor during each half cycle. No slope compensation is required with discontinuous operation.

The main disadvantage of the discontinuous mode is that the triangular shaped input waveform has nearly twice the peak current of the comparable continuous mode waveform. This increases noise problems and transistor current rating requirements.

The Control Loop

The basic control circuit as shown in Fig. 1 is independent of the specific power circuit topology used. It involves an inner current control loop and an outer voltage control loop. The current in the inner loop is programmed according to the output voltage error sensed and amplified by the outer loop. Thus the control circuit operates exactly like any current mode control system—with two exceptions:

1. The current control loop programs the *input* current, not the output current.
2. The programmed current is proportional to the control voltage, V_{ERR}, *multiplied by a half sine derived from the rectified line voltage.*

These two control system elements assure that the input current is a half sine wave in phase with the rectified input voltage, i.e., the input power factor approaches 1.0.

However, there are several significant and limiting problems with this basic control system approach. To set the stage for this, consider the following:

The load power demand on the switching preregulator does not change with input rms line voltage, for two reasons:

1. The preregulator maintains a fairly constant output bus voltage V_{DC}.
2. The downstream switching converters draw constant power regardless of V_{DC} variation.

Since the switching preregulator operates with high efficiency, the *input power drawn from the line does not change with rms line voltage*, but only with downstream load changes.

Therefore, when rms line voltage varies:

a. *rms* line current must be *inversely proportional* to the *rms* line voltage to maintain constant power input.

But *within each half-cycle*:

b. *Instantaneous* current must be *directly proportional* to *instantaneous* line voltage in order to have a good power factor.

Poor open loop line regulation: Criteria (a) and (b) above conflict with each other in the basic control circuit. If control voltage V_{ERR} is fixed (open control loop), instantaneous current programmed by the multiplier is directly proportional to instantaneous line voltage, thus satisfying (b) and providing good power factor. However, in contradiction to (a), rms line current will also vary *directly* with rms line voltage. Thus, although power input should not change, it will actually vary with the *square* of the rms line voltage. This results in very poor open loop line regulation, and requires strong closed loop intervention to correct. But it will be shown that the control loop bandwidth must be much less than 120 Hz. This causes considerable change in dc bus voltage when the line voltage changes rapidly. Without current limiting, input current may be excessive for several half-cycles.

The usual solution to this problem caused by low bandwidth is to add considerable additional control circuitry to sense and limit input current and/or power and to sense and limit over and under-voltage on the dc bus. These auxiliary circuits override the slow main control loop to achieve quick corrective intervention. Whenever this occurs, the input waveform is clipped and the power factor is low for several half-cycles while the main control loop slowly adapts to the new conditions.

A much better solution uses *input voltage feed-forward* to provide the main control circuit with good inherent open-loop line regulation. With input voltage feed-forward, the control circuit can respond to a line voltage change within one half cycle, maintaining low power factor and eliminating most of the additional control circuitry.

Control loop bandwidth limitation: As discussed previously, with a bulk filter capacitor of acceptable cost and size, there will be 120 Hz ripple voltage on the dc bus, perhaps $10V_{p-p}$ on a 380V bus at full load. This results in a 120 Hz control voltage component at the error amplifier output, which will oppose and reduce the ripple on the dc bus, depending upon the control loop gain at 120 Hz. While this ripple reduction is a laudable goal, the 120 Hz control voltage component will distort the half-sine current programming waveform and the input current, as shown in Fig. 5. This can make it impossible to achieve the desired power factor.

To prevent this distortion, *the control voltage must not be allowed to change significantly during each line half-cycle.* Control loop bandwidth must be much less than 120 Hz to keep the input sine wave distortion to an acceptable level. Circuit simulation shows that to achieve P.F. = .96, the *maximum* crossover frequency, f_c, is about 20 Hz at max. V_{in}. At lower V_{in}, f_c will be *much* less. This low bandwidth severely impairs the control loop dynamics. The dc bus voltage will respond very slowly to line or load changes,making it difficult to keep the dc bus voltage within desired limits. If a power factor greater than .98 is required, control loop bandwidth must be very low. (3% harmonic distortion requires P.F. = .999)

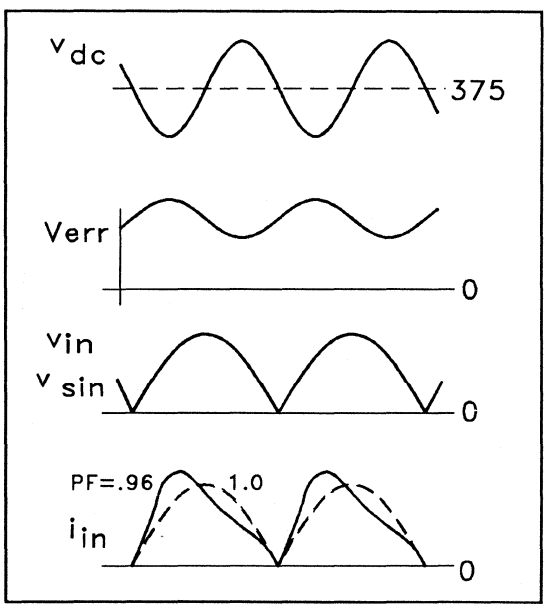


Fig. 5 - Input Current Distortion, PF = .96

Another technique that totally eliminates input current waveform distortion, achieving very high power factors without requiring extreme low bandwidth, is to *sample and hold* the control voltage, V_{ERR}, every half cycle when the line voltage crosses zero. Although the power factor is excellent with the sample and hold (S/H) technique, the crossover frequency is limited to about 20 Hz (one fifth the 120 Hz sampling frequency) for stability reasons.

So whether or not S/H is used, to maintain the dc bus voltage within desired limits requires either (a) extensive override control circuits or (b) input voltage feed-forward, which greatly improves the dynamics by making fast open-loop correction for line voltage changes.

Control loop gain and bandwidth variation: As shown in Eq. (5), the small signal gain from control to output (part of the overall voltage control loop gain) varies with the *square* of the rms input voltage:

$$\frac{v_{dc}}{v_{ERR}} = \frac{kV_{in}^2/V_{DC}}{j\omega C_{DC}} \qquad (5)$$

Thus, the loop gain with V_{in} = 90V is only 1/9 (-19dB) of the loop gain with V_{in} = 270V.

The crossover frequency f_c is also directly proportional to the gain because the gain characteristic has a single pole (-20dB/decade) slope through crossover. Therefore f_c at 90V is also 1/9 of f_c at 270V.

Consider the difficulty covering this span of input voltages (the combined 120V – 220V range limits) without tap switching. The error amplifier gain is set to obtain f_c = 20 Hz maximum crossover frequency at the 270V high line. (A much higher f_c is desired but not possible because of input current distortion.) If the supply is then operated at the 90V low line condition, f_c drops to only 2.2 Hz. Control dynamics become unacceptable. The dc bus voltage, V_{DC}, drops well below the desired regulation range at 90V input because the low frequency loop gain is inadequate.

Again, the proper application of line voltage feed-forward can make the loop gain independent of line voltage variation. This makes it easy to achieve 90V – 270V operation with good dynamics and good dc bus regulation without range switching.

Power/current limit variation: The relatively slow control loop is unable to keep pace with rapid line or load changes. If load power increases rapidly, the control circuit will belatedly try to make up the energy deficit in C_{DC} by drawing excessive current and power from the line for several half-cycles, unless limiting circuitry is provided. Otherwise, line current limits are violated, device current ratings may be exceeded, and excessive power can cause the dc bus voltage to overshoot.

The peak input current is naturally limited because the current programming voltage is clamped by the output voltage capability of the multiplier. The design should set this current programming limit so that 110 - 120% of full load power can be drawn from the line under minimum line voltage conditions.

When the line voltage is high, a fixed current limit allows excessive power input, and dc bus voltage will overshoot with line or load change. A fixed power limit requires the rms current limit to vary *inversely* with V_{in}. This is hard to accomplish without voltage feed-forward.

For example, for the same maximum power, max. rms input current I_{in} should be only 1/3 as much with 270V input as with 90V. But if the peak current limit is set for max. I_{in} needed at 90V, I_{in} at 270V actually increases 30%. This is because V_{sin} at the multiplier input calls for 3 times *larger* current, but the waveform at the multiplier output is clipped at the *peak* input current limit, becoming rectangular in waveshape. Thus the power limit is 4 times larger at 270 V than at 90 V line.

This situation is obviously intolerable, even with a much more limited input voltage range. Additional, rather elaborate control circuits are required to limit current and power, unless input voltage feed-forward is used.

Input Voltage Feed-Forward

It should be apparent by now that input voltage feed-forward is almost a panacea in eliminating a variety of serious problems inherent in the basic high power factor preregulator.

First, without feed-forward, the circuit of Fig. 1 applies voltage V_{sin}, derived from the line input, to one input of the multiplier. This generates a half sine voltage, V_i, patterned after the line voltage waveform and proportional to the amplified output error voltage, V_{ERR}. V_i programs the input current half sine.

$$V_i = k_m V_{sin} \cdot V_{ERR} = k_m k_{in} V_{in} \cdot V_{ERR} \quad (7)$$

where k_m is the multiplier gain factor, and k_{in} is the input voltage divider ratio.

The current control loop (part of the preregulator block in Fig. 1) establishes I_{in} according to programming voltage V_i and current sense resistor R_{sense}. Vi is attenuated by factor k_i (which equals R_1/R_2 in Fig. 7).

$$I_{in} = k_i V_i / R_{sense}$$

Combining with (7) and let $k_1 = k_m k_{in} k_i$:

$$I_{in} = k_1 V_{in} \cdot V_{ERR} / R_{sense} \quad (8)$$

Assuming reasonably high power factor, with rms values:

$$P_{chg} = P_{in} = I_{in} V_{in} = k_1 V_{in}^2 V_{ERR} / R_{sense} \quad (9)$$

the instantaneous version:

$$p_{chg} = k_1 V_{in}^2 (1 - \cos 2\omega_m t) V_{ERR} / R_{sense} \quad (9a)$$

Eq. (9) shows clearly that "gain" P_{chg}/V_{ERR} varies with V_{in}^2, causing all of the problems mentioned earlier. It also points the way to apply input voltage feed-forward to eliminate this V_{in}^2 dependency: divide Eq. (9) by a voltage proportional to rms V_{in}^2, thus cancelling the V_{in}^2 term in the numerator, as in Eq. (10). The method of implementation is shown in the block diagram of Fig. 6., where terms are defined.

From (9) with the divider added:

$$P_{chg} = \frac{k_1 k_d V_{in}^2 V_{ERR}}{k_s k_f^2 V_{in}^2 R_{sense}} = \frac{k_1 k_2 V_{ERR}}{R_{sense}} \quad (10)$$

where $k_d/(k_s k_f^2 V_{in}^2)$ = divider gain
$k_2 = k_d/(k_s k_f^2)$

The feed-forward voltage must be *constant* during each half cycle. This fixes the divider gain during the half cycle in inverse proportion to V_{in}^2 to make the overall loop gain and bandwidth independent of V_{in}. But voltage $V_{sin} = k_{in} V_{in}$ applied to the multiplier is a half sine wave to serve as a pattern to obtain the desired high power factor current waveform.

It must be noted that any 120 Hz ripple in the feed-forward voltage applied to the divider will effectively add to the 120 Hz ripple from the error amplifier to increase the input current waveform distortion, reducing the power factor.

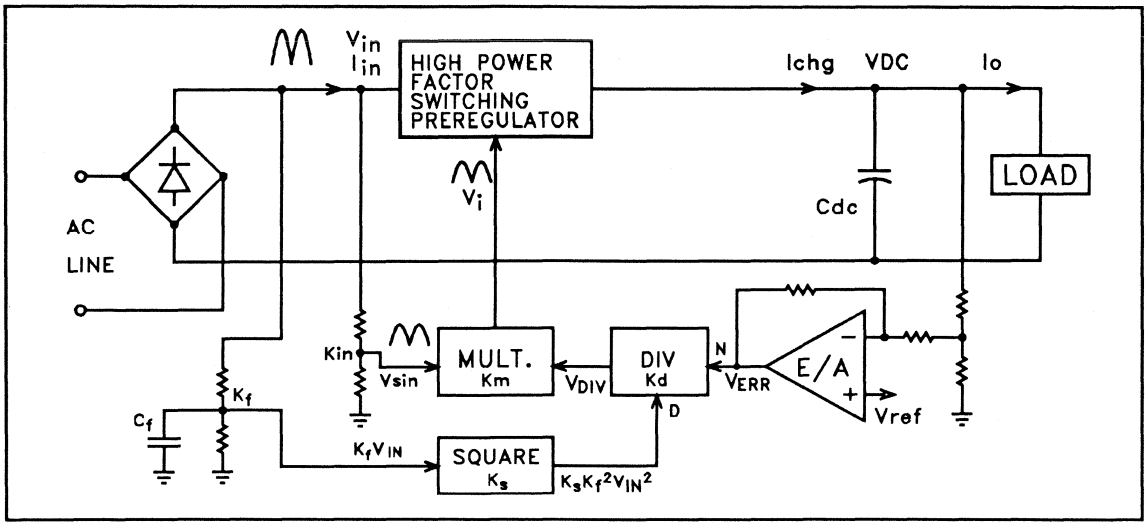


Fig. 6 - High Power Factor Preregulator with Input Voltage Feed-Forward

Capacitor C_f averages the V_{in} waveform and reduces the ripple to an acceptable level. If the time constant $C_fR_{divider}$ is too small, the power factor will be too low. If the time constant is too large, there will be too much feedforward delay, resulting in excessive overshoot and undershoot of the dc bus voltage when the line voltage changes rapidly by a large amount. This is a difficult problem to analyze mathematically, but computer simulation (which is an effective aid for high power factor circuit design) shows that a time constant of one cycle (16 msec at 60 Hz) results in only 4 V overshoot with an instantaneous line change from 180 to 270V, yet is able to achieve a power factor better than .96.

Current Mode Control Problems

Current mode control in its usual implementation is actually "peak inductor current control". When the ripple current is small, the peak inductor current is nearly equal to the average current, which is the actual control objective.

In high power factor preregulator applications, it is desired to control input current. The boost configuration is ideal for current mode control because boost inductor current *is* input current. But buck or flyback circuits are *not* ideal for input current mode control because their inductors are located elsewhere.

(In conventional switching voltage regulator applications, current mode control of *output* current is desired. The buck regulator topology is ideal in this case because the inductor is in the output. But continuous boost and flyback topologies are not well suited because their inductors are not in the output.)

Current mode works by turning off the transistor switch at the point where a voltage derived from the inductor current up-ramp intercepts a relatively constant current programming voltage level. Thus, peak inductor current is controlled. The error between peak and average current is minimized if the ripple current is small but this means the current ramp is shallow and this makes current mode control very noise sensitive.

When current mode control is used in any continuous mode application, slope compensation must be used to ensure stability when duty ratios exceed 0.5. With the boost topology in a high power factor preregulator, slope compensation is needed when the instantaneous line voltage is less than half the output dc bus volts, which occurs for a substantial portion of each line cycle. It is very difficult to achieve slope compensation with the boost preregulator. The inductor current downslope (which determines the amount of slope compensation required) varies with V_{in}, and V_{in} varies tremendously from zero to its large peak value during every line cycle.

Average Current Mode Control

Middlebrook shows that with conventional current mode control, the current loop bandwidth is 1/6 - 1/3 of the switching frequency, f_s. For f_s of 100 kHz, the current loop crossover frequency, f_{ci} > 15 kHz. In conventional voltage regulator applications, this high bandwidth current loop causes the inductor to "disappear" from the small signal model and permits exceptionally high gain-bandwidth in the outer voltage control loop.

But in the high power factor preregulator, the outer loop crossover frequency, f_{co} is limited to less than 20 – 30 Hz, by loop stability or waveform distortion considerations. This means current loop bandwidth f_{ci} does not really need to be more than 1 kHz.

Taking advantage of the wide frequency separation between f_s and f_{co}, the crossover frequency of the current control loop, f_{ci}, is purposely reduced so that the switching frequency ripple and switching noise is reduced to a negligible level. The duty ratio is controlled by comparing the averaged input current error against a sawtooth waveform.

Fig. 7 shows the inner "average current mode control" loop. The input current signal is compared to the 120 Hz current programming voltage V_i (from the multiplier in the outer loop). 100 kHz variations are averaged out through a current error amplifier. The amplified average current error is compared to sawtooth ramp V_s. The comparator output determines the duty ratio of the boost transistor switch which thereby controls the current.

Design approach: The current programming voltage V_i is limited by the multiplier's output voltage swing. This in turn limits the peak input current. The peak voltage across R_{sense} is set by resistor ratio R_1/R_2. For example, suppose a max rms I_{in} of 5 A is desired. If R_{sense} = 0.2 Ω, its dissipation is 5 W, and its voltage is 1 V rms, or 1.414 Vpk. If V_i is limited to 3.0 V, an R_1/R_2 ratio of 1.5/3 = 1/2 establishes a peak input current of 7.5 A, with rms of 5.3 Amps.

To achieve current loop stability, the error amplifier gain, $k_e = R_z/R_i$, is flat from below crossover frequency f_{ci} to above the switching frequency, f_s. This is because a -1 slope (from the inductor) already exists at f_{ci}.

The E/A gain at f_s should be such that the 100 kHz ripple and noise at the E/A output is only one tenth the 3 V sawtooth amplitude, hence negligible. Assuming that inductor L = 700 μH and max Δi_{in} = 1 A have been previously determined, then for example:

$$k_e = \frac{R_z}{R_i} = \frac{V_s/10}{\Delta i_{in} R_{sense}} = \frac{3V/10}{1A \cdot 0.2\Omega} = 1.5 \quad (11)$$

Since the loop gain rolls off with a single pole between f_{ci} and f_s, the resulting crossover frequency is:

$$f_{ci} = \frac{V_o\, k_e R_{sense}}{2\pi L\ \ V_s} = \frac{380 \cdot 1.5 \cdot 0.2}{2\pi \cdot 700 \cdot 3} = 8.6 \text{ kHz} \quad (12)$$

Zero R_zC_z below $f_{ci}/3$ boosts low frequency gain to "average" the current feedback signal, leaving 45° phase margin at f_{ci}.

Some insights: The "average current control" loop operates in the same manner as old fashioned "voltage mode control", except that it: (a) controls current and (b) functions as the inner loop of a two-loop system. Note that the chopped input current in flyback or buck topologies can be averaged and controlled in the same manner. Average current mode control can be applied to any topology even when the inductor current is not equal to the input current. This makes the specific power circuit topology irrelevant to the outer control loop.

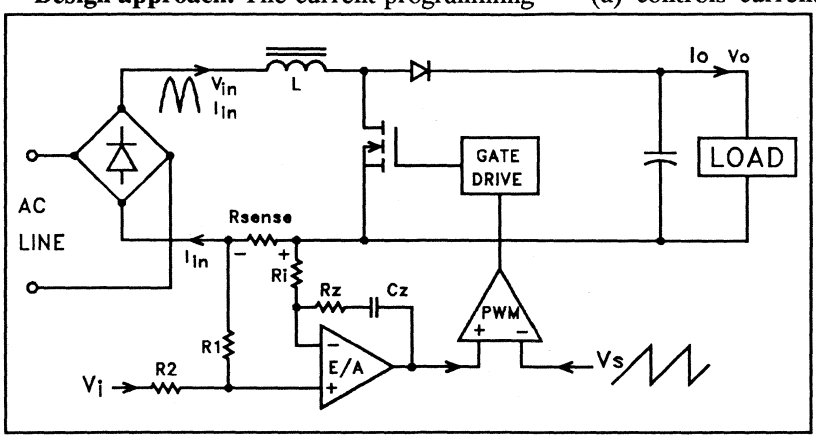


Fig. 7 - Average Current Mode Control Loop

In summary, the advantages of "average current mode control" are:

- ♦ No slope compensation required
- ♦ Good noise immunity
- ♦ No peak-avg error - inner loop actually controls "average input current" - even with flyback topology where inductor is not in input.

The one disadvantage is a somewhat reduced current loop bandwidth. This is not a problem in switching preregulator applications, considering the outer loop crossover frequency must be very low compared to the switching frequency.

(The same "average current mode control" technique can be used for multiple loop control in conventional switching voltage regulators using any power circuit topology, but at the cost of reduced current loop bandwidth.)

Sample and Hold

In a conventional switching power supply, the 0 dB loop gain crossover frequency, f_c, must be below 1/4 or 1/5 of the switching frequency, f_s. Otherwise, subharmonic oscillation occurs. This is definitely *not* a problem with a high power factor preregulator—f_c is *decades* below f_s.

In a high power factor preregulator there is a significant ripple component on the dc bus at the 120 Hz line frequency 2nd harmonic. Without sample and hold, the 120 Hz ripple passes through the control loop. This distorts the input current waveform (see Fig. 5). The amount of distortion depends on the 120 Hz loop gain. Also, if the 120 Hz loop gain is more than 1/4 - 1/5, the amplified ripple becomes so large that clipping occurs, impairing performance. Since the loop gain characteristic has a single pole rolloff (-20 dB/decade) in this region, crossover frequency f_c must be less than 1/4 - 1/5 the 120 Hz ripple frequency, or 25-30 Hz.

Additional 120 Hz ripple comes from the voltage feed-forward circuit, depending on the time constant of the averaging network. With an f_c of 20 Hz (120Hz/6) and a feed-forward time constant of 8 ms (1/2 line period), a P.F. of .95 - .98, (23% - 14% harmonic distortion) is achievable (see Table I).

If 3% input current distortion is required, f_c must be less than 120Hz/20, or 6 Hz, and the feed-forward time constant must be raised to 40 ms to reduce the harmonic levels from these sources. This *destroys* preregulator dynamics, forcing the addition of sensing/power/current limiting circuitry to override the slow loop.

As shown in Fig. 8, a sample and hold circuit placed at the control input to the multiplier is an excellent solution to this problem. The S/H samples the divider output at the very beginning of each half cycle and holds it for the entire half cycle. Thus the 120 Hz ripple from the error amplifier *and* from the feed-forward squaring circuit are eliminated. The input current programming waveform , V_i, becomes a perfect replica of V_{IN}, without distortion.

The crossover frequency is no longer limited by waveform distortion considerations, but a new limitation appears. The sampling frequency, f_{SH} (120 Hz), becomes the "switching frequency" in the small signal model of the outer loop. Also, a sampling delay is introduced in the control loop. The result is that f_c must be less than $f_{SH}/4$ to $f_{SH}/6$ or loop instability in the form of subharmonic oscillation will occur.

Also, when the sample is taken at the beginning of each half sine, the feed-forward voltage very closely approximates the average value of the input sine wave, regardless of the ripple amplitude. This means that high ripple from the feed-forward averaging network can be tolerated, and the time constant can be even shorter than 8 ms.

On the other hand, the sampling delay slows down the feed-forward response as well as the main loop. Computer simulation shows that *without* S/H and a PF of .96, slightly better dynamic response can be achieved than *with* S/H and a PF approaching 1.0.

The recommendation is: If a Power factor of .95 - .98 is acceptable, don't bother with the sample and hold. On the other hand, to achieve 3% distortion (P.F. = .999), the sample/hold technique is very useful.

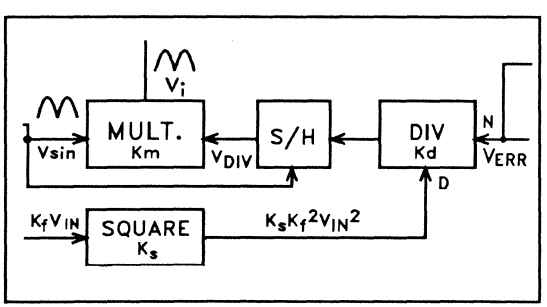


Fig. 8 - Control Circuit with Sample and Hold

Small Signal Model

The simplified small signal model of the outer voltage control loop shown in Fig. 9 is accurate at frequencies below the 120 Hz rectified line. Because the loop gain crossover frequency f_c is considerably less than 120 Hz, and decades less than the preregulator switching frequency, factors such as the rolloff of the inner current loop, the ESR zero of the bulk capacitor and the right half-plane zero of the boost topology are so much higher in frequency than f_c they are completely irrelevant to the performance of the outer loop.

The switching preregulator has the small signal output characteristic of a controlled power source, modeled as a current source shunted by a resistor. This source resistance, r, is always equal to dc load resistance R_L, so r changes when R_L changes. The control-to-output gain has a single pole, associated with the bulk filter capacitor. With a resistive load, the parallel combination of r with ac load resistance r_L ($=R_L$) results in a pole frequency $\omega_p = 2/R_L C_{DC}$. This pole frequency will usually be less than 1 or 2 Hz.

However, a load consising entirely of high efficiency switching converters is not a resistive load—it is close to being a constant power load. (Power demand is fixed and independent of the dc bus voltage as long as it is within the input range capability of the downstream converters.) A constant power load has a negative ac resistance equal to its dc load resistance, i.e., $r_L = -R_L$. The parallel combination r_s ($=R_L$) and r_L ($=-R_L$) approaches *infinity*, so the capacitor pole approaches *zero*. The resistances cancel and the model becomes simply a current source driving capacitor C_{DC}, with a slope of −1 from nearly zero frequency to well above the crossover frequency.

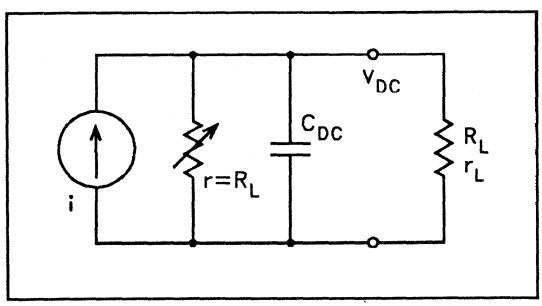


Fig. 9 - Outer Loop Small Signal Model

So r_L could be any value between $+R_L$ and $-R_L$, with the C_{DC} pole somewhere between 0 and 2 Hz. Fortunately, it really doesn't matter, and the gain in the region of interest can be expressed as:

$$v_{DC} = \frac{i_{chg}}{j\omega C_{DC}} = \frac{p_{chg}}{j\omega C_{DC} V_{DC}} \qquad (13)$$

(Note that a constant power source driving a constant power load is open-loop unstable at low frequency. The preregulator must never be tested with a negative resistance load while the voltage control loop is open—it will run away.)

The control-to-output gain also includes the modulator and ac waveshaping multiplier, as well as the feedforward divider and sample/hold, if used—everything from the error amplifier output to the dc bus preregulator output. The gain characteristic of these elements is flat with frequency, although the S/H introduces a delay of less than 1/2 line cycle, ultimately reducing the allowable crossover frequency.

Combining Eq. (13) with the small-signal version of (9) gives the control-to-output gain *without* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 V_{in}^2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (14)$$

Combining Eq. (13) with the small-signal version of (10) gives the control-to-output gain *with* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 k_2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (15)$$

Dimensionally, k_1 is V^{-1}, and k_2 is V^2, which resolves the dimensions of the above equations.

Because the control-to-output characteristic has a near-ideal single pole roll-off, the error amplifier gain should be flat for excellent loop stability. The gain required can be determined without a Bode plot. Simply calculate the arithmetic control-to-output gain at the desired crossover frequency using Eq. (14) at max. V_{in}, or (15) if feed-forward is used. The reciprocal of this number is the error amplifier gain required for a loop gain of 1, which is by definition the crossover frequency. The single 90° phase shift from C_{DC} assures loop stability.

A pole-zero pair could be incorporated in the error amplifier network to improve dc regulation of the dc bus voltage, but this is not recommended. There is no real advantage to

doing this because the low frequency boost cannot follow rapid line or load changes. The dc bus will have the same voltage excursions (although temporary) that would occur without this boost. In either case, the downstream converters will have to operate over the same voltage range. The only way to tighten this range is to (a) employ input voltage feedforward, and (b) increase the bulk capacitor size, which reduces the loop gain, allowing a corresponding error amplifier gain increase.

Bulk Capacitor Selection and System Performance

In any off-line supply, the input filter capacitor makes up a significant portion of the cost and the volume. Factors entering into the selection of the capacitor and the microFarads required are:

(a) ac line voltage range
(b) Power demand
(b) Holdup time (# of half cycles)
(c) Ripple voltage on dc bus
(d) Regulation of dc bus voltage
(e) Dynamics -- overshoot, undershoot
(f) ac current ratings
(g) ESR

Requirements (a) to (e) collectively determine the total dc bus voltage range the system is expected to operate under, with a variety of line and load conditions.

Conventional low power factor systems: With a full wave rectifier off the 220 V line, or voltage doubler off the 115 V line, the usual dc bus voltage range has a 2 to 1 ratio, from 200 to almost 400 V. Half of this is due to line variation, the other half due to 120 Hz ripple and holdup requirements, if any. Regulation is not possible, but this eliminates the dynamics problems often encountered with regulated systems.

The peak current charging the capacitor at the peak of each line cycle is perhaps 8 times the dc current, I_{DC}. through the dc bus. This is why the input power factor is so bad, but it also causes the rms capacitor current to be extremely high for the power input involved. With present day electrolytics, capacitors usually should be selected on the basis of their rms current rating. When this is done, the capacitance value is usually greater than the minimal size that otherwise might be used, and should provide a holdup time of one full cycle, 16 msec.

So rms current and holdup time usually dominate capacitor selection. For example with a full wave bridge rectifier, 150 μF is required with 100 W load for 20 msec holdup time to 200V from min 180V rms line. For a voltage doubler, 200 μF is needed for only 16 msec holdup time (two 400 μF in series).

High power factor systems: The $\sin^2$ charging current waveform has a peak-to-peak value only twice the dc current (Fig. 2), so the rms capacitor current is only $.707 \cdot I_{DC}$. Capacitor selection is now based primarily on holdup time, and reliability is much better because rms current is well below the rating.

With an optimized high power factor preregulator with a nominal dc bus voltage of 375 V and 100 W load, only 100 μF is required for 20 msec holdup to a minimum dc bus voltage of 320 V. Ripple is only 7 $V_{p\text{-}p}$. With voltage feedforward, the preregulator handles line voltage changes from 90 to 270 V with negligible change in dc bus voltage. Instantaneous 2:1 changes in line voltage result in overshoot and undershoot less than 5 V on the dc bus.

When the load changes instantaneously from 100 W down to 20 W, bus voltage rises from 375 to 387 V with no overshoot.

P.F. is 0.97. Loop gain at 120 Hz is -18 dB, and the crossover frequency is 15 Hz.

The above results were obtained by computer simulation, which is an excellent way to experiment with high power factor systems.

The reason that ripple is so low and holdup much better with a smaller capacitor than the low power system is very simple. The capacitor always operates with a bus voltage close to 375 V, even at low line voltage, because of the "bonus" output regulation of the high power factor preregulator. Thus the smaller capacitor consistently stores more energy than in the conventional system at low line. At higher voltage, the ΔV with a given energy withdrawn is smaller than at lower voltage.

Current Limiting with the Boost Topology

Unlike buck and flyback circuits, the boost topology cannot limit severe overcurrent because there is no series switch between input and output, only a shunt switch. High current occuring with fault load conditions and the start-up inrush current surge charging the bulk capacitor can not be limited or controlled without additional circuitry including a series switch.

Load Overcurrent Limiting: The boost topology can control and limit current only as long as the dc bus voltage, V_{DC}, is greater than v_{in}. If an overcurrent condition exceeds the preregulator power limit established by the control circuit, V_{DC} will eventually be dragged down below the peak value of the AC line voltage. When this occurs, the boost topology loses control. Current will rise rapidly and without limit through the series inductor and rectifier. Ultimately, the inductor will saturate and components will fail. The shunt switch is held *off* by the control circuit, since the current is above the desired level. It can't help to turn the switch ON -- the inductor current will rise even more rapidly and switch failure will occur.

Arguably, the downstream converters will have current limiting capability, eliminating concern about load faults. But a downstream converter or the bulk capacitor might fail. In some systems, the bulk capacitor voltage is bused to other boards or system modules, and there is a good possibility of a short circuit across this high voltage bus.

If it is considered necessary to limit the current to a safe value in the event of a downstream fault, some means external to the boost converter must be provided. This might be an additional series switching transistor or a fuse -- can it act rapidly enough??

Startup Inrush Current Limiting: Before start-up, V_o is zero. When V_{in} is switched on at the input of the boost converter, the bulk capacitor will attempt to charge resonantly to twice V_{in}. If V_{in} happens to be at the peak high-line 220 V condition (370 V) when the supply is turned on, the bulk capacitor will try to resonantly charge to 740 V. The peak resonant charging current through the inductor will be many times greater than normal full load current. To prevent saturation, the inductor must be much larger and more expensive. The boost shunt switch can do nothing to prevent this. The switch should not be turned on at all during start-up, or it will make the situation worse.

The current and voltage overshoot in the start-up scenario described above is intolerable. A fuse is no solution -- the fuse would blow each time to supply is turned on.

There are several methods that may be used to solve the start-up problem:

1. **"Start-up" bypass:** A additional rectifier bypassing the the boost inductor and rectifier diverts the start-up inrush current away from the boost inductor, as shown in Fig. 10. The bulk capacitor charges through D_{bypass} to the peak AC line voltage without resonant overshoot and without excessive inductor current. Under normal operating conditions, V_{DC} is higher than peak V_{in} , and D_{bypass} is reverse biased. If load overcurrent pulls down V_{DC}, D_{bypass} conducts, but this is probably preferable to having the boost inductor carry the overload.

Inrush current is high with this technique, limited only by line impedance, the same as a simple capacitor input filter. A resistor in series with D_{bypass} could theoretically limit the inrush, but a resistance large enough to have a significant effect passes most of the start-up inrush back to the inductor.

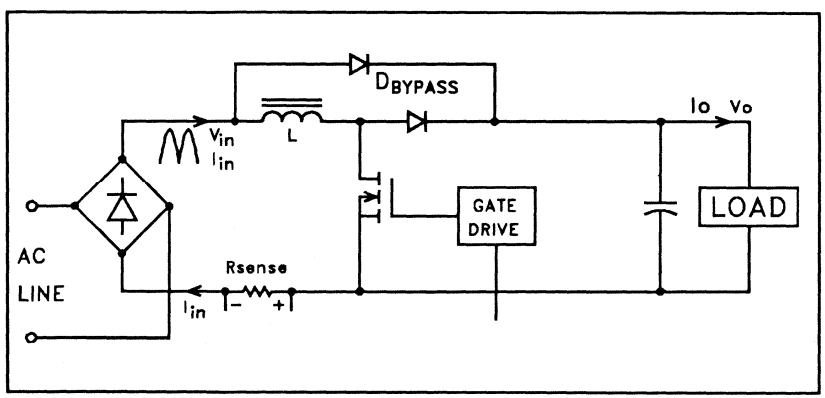


Fig. 10 - Rectifier Bypass of Start-Up Inrush Surge

2. **External inrush limiting circuit:** A thermistor in series with the preregulator input will limit the inrush current, but it has losses and is used only in low power systems. Also, the thermistor cannot respond fast enough to provide protection after a line dropout of a few cycles.

A more efficient approach uses a series input resistor shunted by a Triac or SCR which turns on toward the end of the surge, after the voltage across the inrush limiting resistor diminishes. A control circuit is necessary. This method can function on a cycle-by-cycle basis for protection after a dropout. It is frequently used at higher power levels, but its cost can be excessive for low power applications. It does not protect against load overcurrent.[2]

3. **"Buck or Boost" Topology:** Adding an additional series transistor and free-wheeling rectifier ahead of the boost inductor as shown in Fig. 11 provides a circuit which can limit load overcurrent as well as start-up inrush surge. It operates in *either* boost mode or buck mode. The series (buck) switch functions for current limiting only and has its own control circuit. Under normal conditions the buck transistor is continuously *on* and the circuit functions strictly as a boost converter. During load overcurrent or start-up surge conditions when V_{DC} is below v_{IN}, the shunt (boost) switch is kept continuously *off* by its independent control circuit and the buck switch is pulse width modulated by its overcurrent controller to limit the current to the desired level. Both controllers share the same current sense resistor.

In the buck regulator mode, input current is chopped, generating noise at the input, but this happens only under overcurrent conditions.

(This two-transistor topology can also be used, with a different control circuit, in the buck-boost (flyback) mode. This is achieved by pulse width modulating both switches in a complementary manner, with the buck switch *on* while the boost switch is *off*, and vice-versa. This is a two-transistor flyback configuration. It functions whether V_{DC} is greater or less than v_{IN} so it can be used in a high power factor preregulator supplying a 300 V bus from 220 V line, for example.)

Miscellaneous Considerations

The following considerations are pertinent in designing high power factor circuits:

Power Factor vs. harmonic content: Figure 5 shows the rectified input current waveform with 0.96 Power Factor. This rectified current waveform distortion is caused by the 120 Hz ripple on the dc bus and the 120 Hz feedforward ripple which are both passed through the control circuit and distort the current programming waveform. As shown in Figure 5, the rectified current waveform distortion is mainly phase-shifted 120 Hz.

However, this 120 Hz *rectified* waveform distortion translates into a 90° leading 60 Hz component and a third harmonic component in the *unrectified* line current on the input side of the bridge rectifier. These two components have the same amplitude. With a Power Factor of 0.96, the 90° leading component is 20% and the 3rd harmonic distortion component is also 20% of the in-phase fundamental.

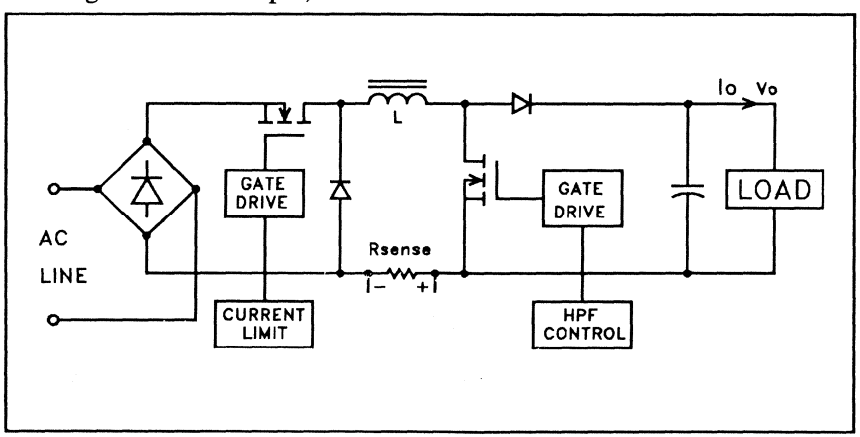


Fig. 11 - "Buck or Boost" Current Limiting Configuration

The relationship between the total rms line current with its various components and the Power Factor is:

$$I_{rms} = (I_{f0}^2 + I_{f90}^2 + I_{H3}^2)^{1/2}$$

$$\text{P.F.} = I_{f0}/I_{rms}$$

where I_{rms} = total rms current
I_{f0} = in-phase fundamental
I_{f90} = 90° phase-shifted fund.
I_{3H} = third harmonic

Table I shows Power Factor vs. I_{3H} and I_{f90} as a percentage of I_{f0}.

Table I - *Power Factor vs. Phase Shifted and Third Harmonic Components*

P.F.	$\%I_{f90}/I_{f0}$	$\%I_{3H}/I_{f0}$
0.87	40	40
0.92	30	30
0.95	23	23
0.98	14	14
0.997	5	5
0.999	3	3

Limiting and clamping: All of the control circuit elements—error amplifier, multiplier, divider, squaring circuit—have inherent limits on their output voltage swings. This results in waveform clipping and input current or power limiting, depending on where in the control circuit this occurs. Careful planning is required to use these inherent bounds properly to limit peak current and power while avoiding unintended limiting at operating extremes. Referring to Fig. 6:

The multiplier output clips peak V_i, thus limits peak I_{in}. R_{sense} and the divider at the current error amplifier input should be set up so that peak I_{in} is adequate for full load power at minimum V_{in}.

Divider k_{in} should be set so that with min. V_{in} and max. V_{DIV} (or max. V_{ERR} with no feed-forward), peak V_i is just below the multiplier output range limit.

Feed-forward divider k_f should be set in conjunction with the squaring circuit gain, k_s, so that the divider output is near its range boundaries at extremes of V_{in} and V_{ERR}.

With feed-forward, the error amplifier output limit can be used to limit maximum power input, regardless of Vin.

(Remember that with the boost topology, if an overload is severe enough to pull the output V_{DC} below v_{in}, the boost transistor remains off and current limiting no longer works, unless separate means are provided.)

Control circuit dc offsets: As the control signals propagate through the various control circuit stages, the original dc levels are frequently lost.

The intended zero point of the V_i current programming waveform is lost at the multiplier output. It must be brought into correspondence with the zero current level of the I_{in} waveform as seen across R_{sense}, or the I_{in} rectified sine wave will have its bottom clipped or elevated, resulting in distortion and reduced P.F.

DC offset through the feed-forward squaring and dividing circuits will hurt feed-forward linearity, reintroducing some loop gain and bandwidth variation with V_{in}, and perhaps interfering with input power limiting as set up at the error amplifier output.

The reference voltage at the error amplifier non-inverting input should be at the mid-range of the E/A output swing capability to minimize dc bus voltage offset error. Avoid using a capacitor in series with the E/A feedback to eliminate this offset—it will cause overshoot.

While these offsets can cause great difficulty in achieving very low harmonic distortion, they should be quite managable for P.F. up to 0.98. Watch out for temperature variations of these offsets.

Summary Comparison

High power factor preregulators provide many advantages and eliminate many of the problems compared with a simple capacitor input filter. In some systems, the reduced bulk capacitor cost and savings in the downstream converters because of the much narrower dc bus voltage range will pay for the increased cost of the preregulator.

Table II summarizes the comparison of a high power factor preregulator which can operate from 90 to 270 Volt rms line without range switching, vs. a conventional 90 to 135 V doubler and a 180 to 270 V full wave bridge.

Some aspects of the closed loop involving multipliers, dividers, and sample/hold elements do not fit into existing small signal models. Computer simulation is an ideal tool to evaluate and optimize high power factor circuits as part of the design process.

References

[1] R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," *Proceedings of Powercon 8,* pp. H4.1–H4.6, April 1981.

[2] R. Adair, "Incorporate Active Inrush Current Limiting to Improve Reliability and Efficiency of Power Supplies," *Unitrode Application Note U-83.*

[3] Power Electronics Group, California Institute of Technology, "Input-Current Shaped Ac-to-Dc Converters," *Final Report Prepared for NASA*, May, 1986.

[4] B. L. Wilkinson, J. Mandelcorn, "Unity Power Factor Supply," *U. S. Patent #4,677,366*, June, 1987

Table II - *Summary Comparisons*

100 WATT LOAD ON DC BUS

	115 V Doubler	220 V Bridge	High P. F. Preregulator
Line Voltage Range (Volts rms)	90 - 135 V	180 - 270	90 - 270
Bulk Filter Capacitance (μF)	2 x 400 μF	150	100
Holdup Time, milliseconds to min. V_{DC}:	16 ms 200 V	20 200	20 320
Normal dc Bus Voltage Range, V	228 - 381 V	226 - 381	360 - 390
Maximum Bus Ripple Voltage, p-p	18 V p-p	28	7
Power Factor	0.6	0.65	0.96

How to Place Leakage and Wiring Inductances in the High Frequency Circuit Model

by Lloyd Dixon

TOPIC 7

How to Put Leakage and Wiring Inductances in the High Frequency Circuit Model

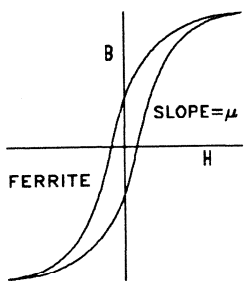
Lloyd H. Dixon, Jr.

OBJECTIVES

1. DEFINE THE ELECTRICAL CIRCUIT EQUIVALENTS OF MAGNETIC DEVICE STRUCTURES TO ENABLE IMPROVED ANALYSIS OF CIRCUIT PERFORMANCE.
2. DEFINE THE MAGNITUDE AND CIRCUIT LOCATION OF RELEVANT PARASITIC MAGNETIC ELEMENTS TO ENABLE PREDICTION OF PERFORMANCE EFFECTS.
3. MANIPULATE PARASITIC ELEMENTS TO OBTAIN IMPROVED OR ENHANCED CIRCUIT PERFORMANCE.
4. ENCOURAGE THE CIRCUIT DESIGNER TO BE MORE INVOLVED WITH MAGNETIC DEVICE DESIGN.

1A

MAGNETIC FUNDAMENTALS



INT'L STD UNITS (S.I.)
RATIONALIZED MKS

UNIT VOLUME PARAMETERS:
- B Flux Density
- H Field Intens. A-T/m
- μ Permeability B/H

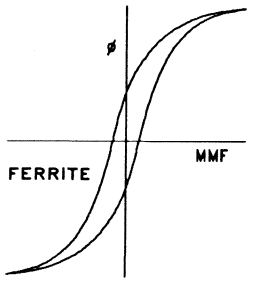
ENERGY DENSITY:
$W/m^3 = \int HdB \rightarrow BH/2$

CAN'T FORCE INST. CHANGE

AIR vs. FERRITE

1B

MAGNETIC FUNDAMENTALS



$\phi = BA$ Flux Webers

$MMF = H\ell$ Potential A-T

Slope:

$P = \phi / MMF$ Permeance

AMPERE'S LAW:

$NI = \int H d\ell \dashrightarrow H\ell$

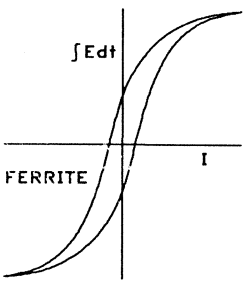
FARADAY'S LAW:

$d\phi/dt = -E/N$; $\phi = 1/N \int E dt$

PERMEANCE IS INDUCTANCE OF 1 TURN

1B1

MAGNETIC FUNDAMENTALS



$\int E dt = \phi \cdot N$ (Faraday's Law)

$I = H\ell/N$ (Ampere's Law)

SLOPE = $L = \int E dt / I$

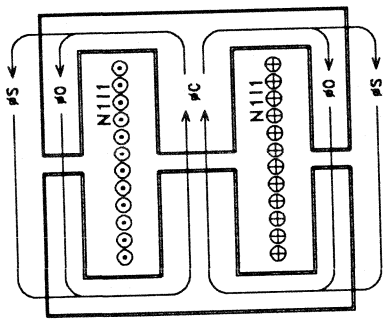
1B2

CONVERSION FACTORS, CGS to SI

		SI	CGS	CGS to SI
FLUX DENSITY	B	Tesla	Gauss	10^{-4}
FIELD INTENSITY	H	A-T/m	Oersted	$1000/4\pi$
PERMEABILITY (space)	μ_o	$4\pi \cdot 10^{-7}$	1	$4\pi \cdot 10^{-7}$
PERMEABILITY (Rel)				1
AREA (Core,Window)	A	m	cm	10^{-4}
LENGTH (Core, Gap)	ℓ	m	cm	10^{-2}
TOTAL FLUX = $\int BdA$	ϕ	Weber	Maxwell	10^{-8}
TOTAL FIELD = $\int Hd\ell$	F, MMF	A-T	Gilbert	$10/4\pi$
RELUCTANCE = MMF/ϕ	R			$10^9/4\pi$
PERMEANCE=1/R=L/N^2	P			$4\pi \cdot 10^{-9}$
INDUCTANCE = $P \cdot N^2$	L	Henry	(Henry)	1
ENERGY	W	Joule	Erg	10^{-7}

1C

INDUCTOR – MAGNETIC STRUCTURE

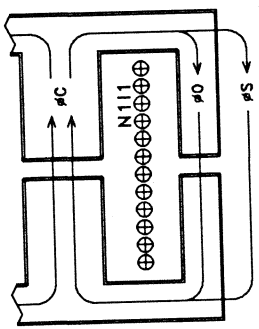


PROBLEMS:
DISTRIBUTED MMF
DISTRIBUTED FLUX
FRINGING FIELD
STRAY FLUX

SIMPLIFY:
COMBINE OUTER LEGS
Symmetry
No Fract. Turns

2

INDUCTOR – MAGNETIC STRUCTURE

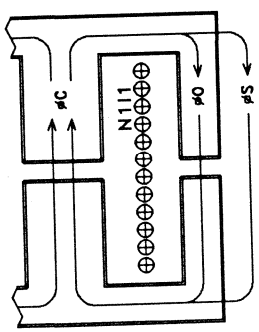


DISTRIBUTED MMF
CIRCULATION

SIMPLIFY:
CONCENTRATE WINDING
IGNORE FRINGING FIELDS
MIN # OF FLUX DIV. POINTS
DEFINE DISCRETE REGIONS

2A

INDUCTOR – MAGNETIC STRUCTURE



ASSUME TYPICAL VALUES:
$A_e = 1 cm^2$; $\ell_e = 10 cm$
$A_w = 2 cm^2$ (ETD34)

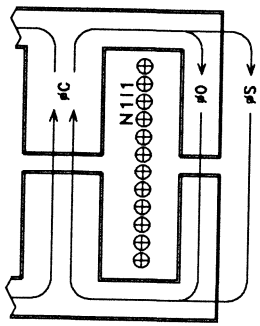
MAX $H\ell = NIm = JmAw = 400 \cdot 2 = 800$

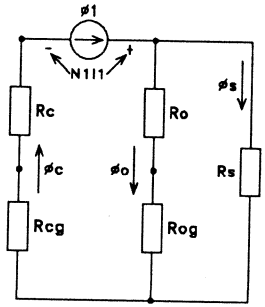
MAX ENERGY – FULL UTILIZ:
$W_m = H\ell \cdot BmA_e/2$
$= 800 \cdot .25 \cdot .0001/2 = 5mJ$

GAP LENGTH – FULL UTILIZ:
$\ell_g = NI/H = NI\mu/B$
$= 800 \cdot 4\pi \cdot 10^{-7}/.25 = .4cm$

2A1

SIMPLIFIED RELUCTANCE MODEL

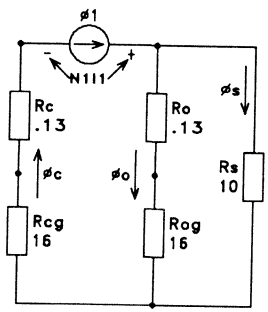




"DISCRETIZED" – SOURCE, Rc, Ro

2B

SIMPLIFIED RELUCTANCE MODEL



RELUCTANCE = MMF/ø

$R = H\ell/BA = \ell/\mu A$

APPORTION ℓe TO Rc, Ro

APPTN ℓg TO Rcg, Rog

$\mu=\mu o\mu r$, $\mu o=4\pi\cdot10^{-7}$

μr=1 (air), =3000 (ferrite)

$Ro=(\ell e/2)/(\mu o\mu rAe)$

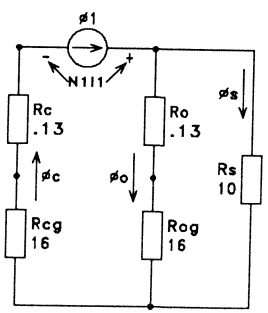
$=.05/(\mu o\mu r\cdot.0001)$

$Ro=.133\cdot10^{8}$ (omit 10^{8})

Rs IS AN ESTIMATE

2B1

SIMPLIFIED RELUCTANCE MODEL



WITH ALL LEGS GAPPED:

Rc<<Rcg; Ro<<Rog

STRAY FLUX, L>PREDICTED

WITH OUTERLEG GAP ONLY:

Rcg=0; Rc,Ro<<Rog,Rs

GREATER STRAY FLUX

WITH CENTERLEG GAP ONLY:

Rog=0

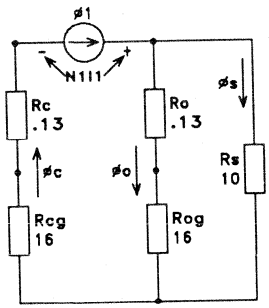
Ro<<Rcg and Rs

MINIMAL STRAY FLUX

Rcg TOTALLY DOMINANT

2B2

SIMPLIFIED RELUCTANCE MODEL



CALCULATING:
I1 FROM AMPERE'S LAW
V1 FROM FARADAY'S LAW
IS THIS THE EQUIVALENT ELECTRICAL CIRCUIT?

PROBLEM:
I1 IS A POTENTIAL
V1 IS A CURRENT

FOUR PROBLEMS

2B3

THE EQUIVALENT ELECTRICAL CIRCUIT

IS A DUAL OF THE MAGNETIC CIRCUIT

(ELECTRICAL DUALS ARE NOT EQUIVALENT: CUK vs FLYBACK)

MAGNETIC – ELECTRICAL DUALITY:

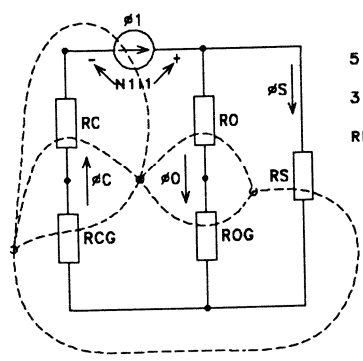
NODES	MESHES (LOOPS)
MMF	AMP-TURNS
dø/dt	VOLTS/TURN
RELUCTANCE	PERMEANCE
SHORT	OPEN
SERIES ADDN.	PAR. ADDN.

ORIENTATION: ROTATE IN SAME DIRECTION

CIRCUITS MUST BE PLANAR

2C

THE MAGNETIC/ELECTRICAL DUAL



5 NODES ---> 5 LOOPS

3 LOOPS ---> 3 NODES

RELUCTANCE-->PERMEANCE

MMF--->NI

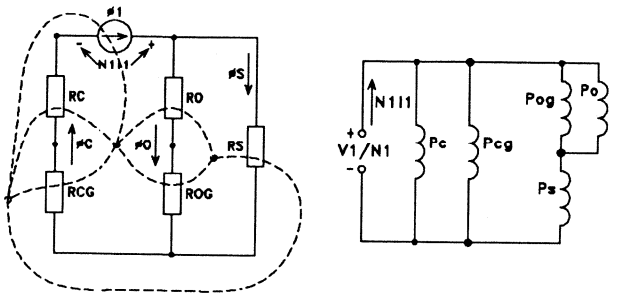
dø/dt-->V/N

ORIENTATION

PLANAR

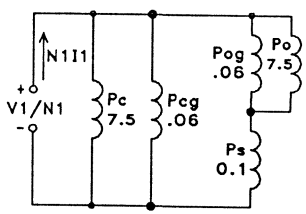
2C1

THE MAGNETIC/ELECTRICAL DUAL



2C2

THE EQUIVALENT ELECTRICAL CIRCUIT



PERMEANCE = 1/RELUCTANCE

UNITS: Henrys/Turn

$P = 1/R = \mu A/\ell = L/N^2$

$Po = 1/Ro = 7.5\mu H/N^2$

$V1/N1 = d\phi 1/dt$

$N1I1 = H\ell$

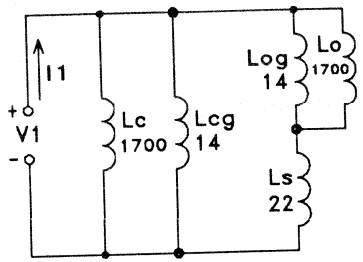
COMBINE INTO ONE

NOTE RELATIVE SIGNIFICANCE

2D

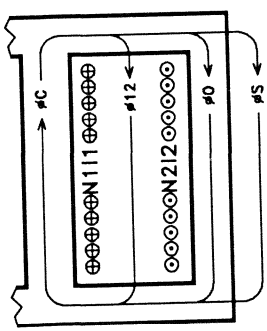
THE EQUIVALENT ELECTRICAL CIRCUIT

WITH N = 15 TURNS



2D2

SIMPLE TRANSFORMER



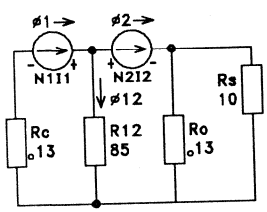
ASSUME V1 ACROSS N1
NO LOAD – I2=0
MMF IS TINY – NO GAP
I1=MAGNETIZING I_m
ϕ12 IS NEGLIGIBLE

WITH FULL LOAD I2
LARGE MMFs – CANCEL
EXCEPT BETWEEN COILS
ϕ12 IS LARGE
LEAKAGE L ENERGY
N1I1 = N2I2 + N1I_m

3

TRANSFORMER RELUCTANCE MODEL

ETD34 CORE. Rc, Ro, Rs FROM PREVIOUS EXAMPLE
WINDOW DIM.: BREADTH bw=2.5cm, HEIGHT hw=.8cm
MEAN TURN LENGTH, MLT=6cm

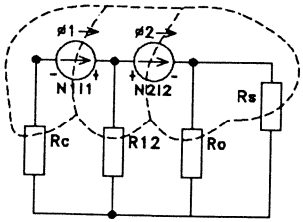


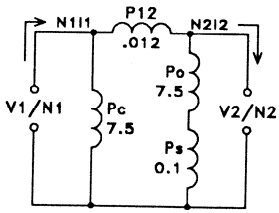
CALCULATE R12 = $\ell/\mu A$
ASSUME WDG CTR = .4cm
A = .4·.6 = 2.4 cm
= .0024 m
ℓ = 2.5cm = .025m
R12 = $85 \cdot 10^6$

ALL R VALUES $\cdot 10^6$

3A

THE TRANSFORMER ELECTRICAL DUAL



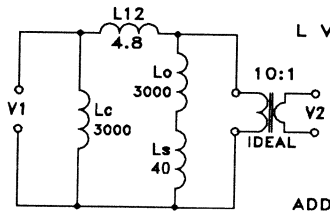


4 LOOPS, 4 NODES IN BOTH

3B

TRANSFORMER EQUIVALENT CIRCUIT

WITH Np = 20 TURNS, Ns = 2 TURNS



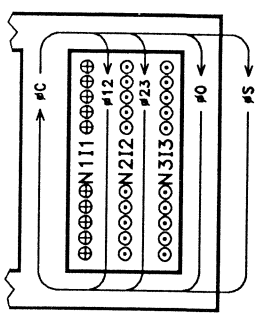
L VALUES REFERRED TO PRI.

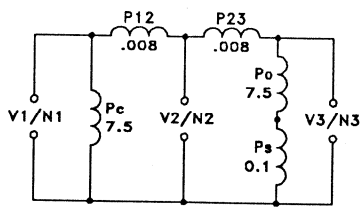
ADDED IDEAL TRANSFORMER
ALLOWS DIFFERENT Np/Ns
PROVIDES GALV. ISOLATION

3C

THREE–WINDING TRANSFORMER

Refer to Topic P2





PERMEANCE IN $\mu H/turn^2$

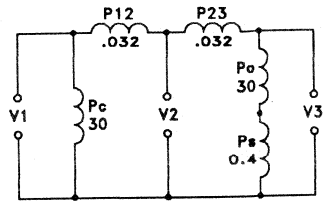
4

THREE–WINDING TRANSFORMER

ASSUME Np=20, Ns=2

L VALUES IN μH

REF TO 2 TURN SEC.



EXPLORE:

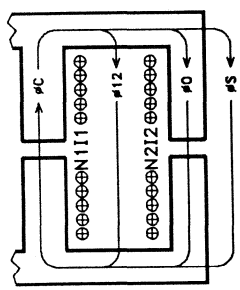
1 PRI (N1), 2 SEC (N2,N3)	T1=10:1
1 PRI (N1), 1 SEC (N2 OR N3)	T1=10:1
2 PAR PRI (N1,N2), 1 SEC (N3)	T1,T2=10:1 P
2 PAR PRI (N1,N3), 1 SEC (N2)	T1,T3=10:1 P
2 SER PRI (N1,N3), 1 SEC (N2)	T1,T3=5:1 S

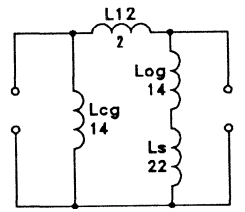
4A

COUPLED INDUCTOR

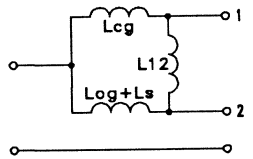
N1, N2 = 15 TURNS

L IN μH



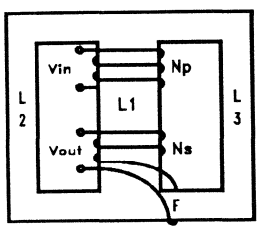


Ref.
Topics
M7. P3



5

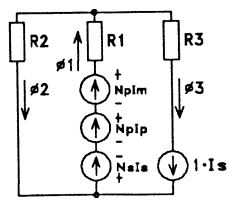
FRACTIONAL TURNS

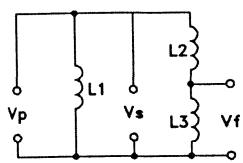


EFFECTIVE LEAKAGE L

HOW TO STIFFEN UP

Ref. Topic M8





6

REFERENCES

1. CHERRY, E.C., "The Duality Between Electric and Magnetic Circuits and the Formation of Transformer Equivalent Circuits," Proc. Phys. Soc. (Britain), 62B, pp 101–111, Feb. 1949

2. Severns and Bloom, "Modern DC–to–DC Switchmode Power Converter Circuits," Van Nostrand Reinhold Co., Inc., New York, 1985.

3. Dauhajre and Middlebrook, "Modelling and Estimation of Leakage Phenomena in Magnetic Circuits," IEEE Power Electronics Specialists Conference, 1986 Record, pp. 213–226.

9

Eddy Current Losses in Transformer Windings and Circuit Wiring

by Lloyd Dixon

TOPIC 8

Eddy Current Losses in Transformer Windings and Circuit Wiring

Lloyd H. Dixon, Jr.

Introduction

As switching power supply operating frequencies increase, eddy current losses and parasitic inductances can greatly impair circuit performance. These high frequency effects are caused by the magnetic field resulting from current flow in transformer windings and circuit wiring.

This paper is intended to provide insight into these phenomena so that improved high frequency performance can be achieved. Among other things, it explains (1) why eddy current losses increase so dramatically with more winding layers, (2) why parallelling thin strips doesn't work, (3) how passive conductors (Faraday shields and C.T. windings) have high losses, and (4) why increasing conductor surface area will actually worsen losses and parasitic inductance if the configuration is not correct.

Basic Principles

The following principles are used in the development of this topic and are presented here as a review of basic magnetics.

1. Ampere's Law: The total magneto-motive force along *any* closed path is equal to the total current enclosed by that path:

$$F = \oint H d\ell = I_t = NI \quad \text{Amps} \qquad (1)$$

where F is the total magneto-motive force (in Amperes) along a path of length ℓ (m), H is field intensity (A/m), and I_t is the total current through all turns enclosed by the path.

2. Conservation of energy: At any moment of time, the current within the conductors and the magnetic field are distributed so as to minimize the energy taken from the source.

3. Energy content of the field: The magnetic field *is* energy. The energy density at any point in the field is:

$$w = \int H dB \quad \text{Joules/m}^3$$

where B is the flux density (Tesla). In switching power supplies, almost all magnetic energy is stored in air gaps, insulation between conductors, and within the conductors, where relative permeability μ_r is essentially 1.0 and constant. The energy density then becomes:

$$w = \tfrac{1}{2}BH = \tfrac{1}{2}\mu_0 H^2 \quad \text{J/m}^3$$

where μ_0 is the absolute permeability of free space ($=4\pi \cdot 10^{-7}$ in S.I. units). Total energy W (Joules) is obtained by integrating the energy density over the entire volume, v, of the field:

$$W = \tfrac{1}{2}\mu_0 \int H^2 dv \quad \text{Joules}$$

Within typical transformers and inductors, the magnetic energy is almost always confined to regions where the field intensity H is relatively constant and quite predictable. This often occurs in circuit wiring, as well. In these cases:

$$W = \tfrac{1}{2}\mu_0 H^2 A \cdot \ell \quad \text{Joules} \qquad (2)$$

and from (1), $H\ell = NI$. Substituting for H:

$$W = \tfrac{1}{2}\mu_0 N^2 I^2 A/\ell \quad \text{Joules} \qquad (3)$$

where A is the cross-section area (m^2) of the region normal to the flux, and ℓ is the length of the region in meters (and the effective length of the field).

4. Circuit inductance: Inductance is a measure of an electrical circuit's ability to store magnetic energy. Equating the energy stored in the field from (3) with the same energy in circuit terms:

$$W = \tfrac{1}{2}LI^2 = \tfrac{1}{2}\mu_0 N^2 I^2 A/\ell$$

$$L = \mu_0 N^2 A/\ell \qquad (4)$$

Skin Effect

Figure 1 shows the magnetic field (flux lines) in and around a conductor carrying dc or low frequency current I. The field is radially symmetrical, as shown, only if the return current with its associated field is at a great distance.

At low frequency, the energy in the magnetic field is trivial compared to the energy loss in the resistance of the wire. Hence the current

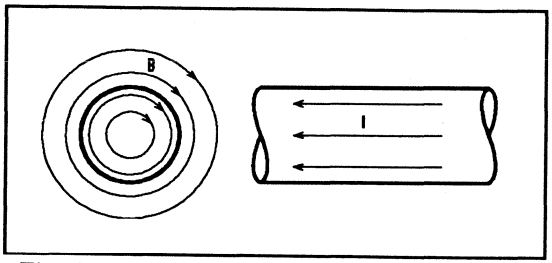


Fig. 1 - Isolated Conductor at Low Frequency

distributes itself uniformly throughout the wire so as to minimize the resistance loss and the total energy expended.

Around any closed path outside the wire (and inside the return current), magneto-motive force F is constant and equal to total current I. But field intensity H varies inversely with the radial distance, because constant F is applied across an increasing ℓ ($=2\pi r$).

Within the conductor, F at any radius must equal the enclosed current at that radius, therefore F is proportional to r^2.

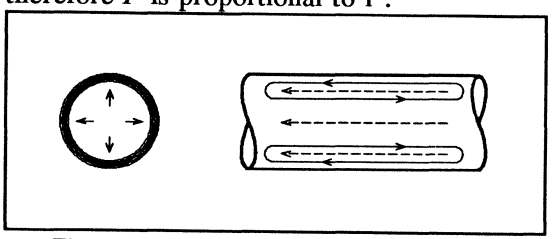


Fig. 2 - Eddy Current at High Frequency

At high frequency: Figure 2 is a superposition model that explains what happens when the frequency rises. The dash lines represent the uniform low frequency current distribution, as seen in Fig. 1. When this current changes rapidly, as it will at high frequency, the flux within the wire must also change rapidly. The changing flux induces a voltage loop, or eddy, as shown by the solid lines near the wire surface. Since this induced voltage is within a conductor, it causes an eddy current coincident with the voltage. Note how this eddy current reinforces the main current flow at the surface, but opposes it toward the center of the wire.

The result is that as frequency rises, current density increases at the conductor surface and decreases toward zero at the center. as shown in Fig. 3. The current tails off exponentially within the conductor. The portion of the conductor that is actually carrying current is reduced, so the resistance at high frequency (and resulting losses) can be many times greater than at low frequency.

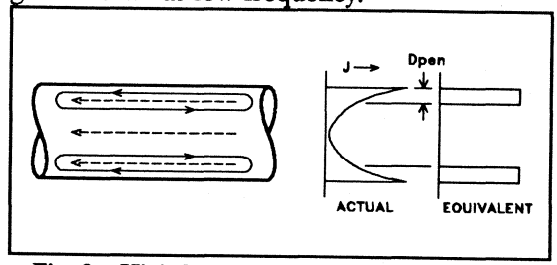


Fig. 3 - High Frequency Current Distribution

Penetration depth: Penetration or skin depth, D_{PEN}, is defined as the distance from the surface to where the current density is 1/e times the surface current density (e is the natural log base)[1]:

$$D_{PEN} = [\ \rho/(\pi\mu f)\ ]^{1/2} \quad m \qquad (5)$$

where ρ is resistivity. For copper at 100°C, $\rho = 2.3 \cdot 10^{-6}\ \Omega$-cm, $\mu = \mu_0 = 4\pi \cdot 10^{-7}$, and:

$$D_{PEN} = 7.5/(f)^{1/2} \quad cm \qquad (6)$$

From (6), D_{PEN} = .024 cm at 100 kHz, or .0075 cm at 1 MHz.

Eqs. (5) and (6) are accurate for a flat conductor surface, or when the radius of curvature is much greater than the penetration depth.

Although the current density tails off exponentially from the surface, the high frequency resistance (and loss) is the same as if the current density were constant from the surface to the penetration depth, then went abruptly to zero as shown on the right hand side of Fig. 3. This equivalent rectangular distribution is easier to apply.

Equivalent circuit model: Another way of looking at the high frequency effects in transformer windings and circuit wiring is through the use of an equivalent electrical circuit model. This approach is probably easier for a circuit designer to relate to.

Figure 4 is the equivalent circuit of the isolated conductor of Figs. 1 to 3. With current I flowing through the wire, L_x accounts for the energy $\frac{1}{2}L_xI^2$ stored in the external magnetic field. L_x is the inductance of the wire at high frequencies.

Point A represents the outer surface of the conductor, while B is at the center. R_i is the

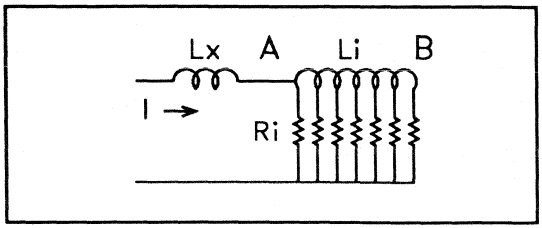


Fig. 4 - Conductor Equivalent Circuit

resistance, distributed through the wire from surface to center. Think of the wire as divided into many concentric cylinders of equal cross section area. The R_i elements shown in the drawing would correspond to the equal resistance of each of the cylinders. Likewise, the internal inductance L_i accounts for the magnetic energy distributed through the cylindrical sections. The energy stored in each section depends on the cumulative current flowing through the elements to the right of that section in the equivalent circuit.

Note that external inductance L_x of the wire (or the leakage inductance of a winding) limits the maximum di/dt through the wire, depending on the source compliance voltage, no matter haw fast the switch turns on.

The time domain: If a rapidly rising current is applied to the wire, the voltage across the wire is quite large, mostly across L_x. Internal inductance L_i blocks the current from the wire interior, forcing it to flow at the surface through the left-most resistance element, even after the current has reached its final value and the voltage across L_x collapses. Although the energy demand of L_x is satisfied, the voltage across the wire is still quite large because current has not penetrated significantly into the wire and must flow through the high resistance of the limited cross-section area at the surface. Additional source energy is then mostly dissipated in the resistance of this surface layer.

The voltage across this R_i element at the surface is impressed across the adjacent L_i elements toward the center of the wire, causing the current in L_i near the surface to rise. Current cannot penetrate without a field being generated within the conductor, and this requires energy. As time goes on, conduction propagates from the surface toward the center (at B in the equivalent circuit), storing energy in L_i. More of the resistive elements conduct, lowering the total resistance and reducing the energy going into losses. Finally, conduction is uniform throughout the wire, no further energy goes into the magnetic fields external or internal to the wire, and a small amount of energy continues to be dissipated in R_i over time.

Note that the concept of skin depth has no meaning in the time domain.

The frequency domain: Referring again to Fig. 4 with a sine wave current applied to the terminals, it is apparent that at low frequencies, the reactance of internal inductance L_i is negligible compared to R_i. Current flow is uniform throughout the wire and resistance is minimum. But at high frequency, current flow will be greatest at the surface (A), tailing off exponentially toward the center (B).

Penetration depth (skin depth) is clearly relevant in the frequency domain. At any frequency, the penetration depth from Eq. (5) or (6) reveals the percentage of the wire area that is effectively conducting, and thus the ratio of dc resistance to ac resistance at that frequency.

Although the current waveforms encountered in most switching power supplies are not sinusoidal, most papers dealing with the design of high frequency transformer windings use a sinusoidal approach based on work done by Dowell in 1966.[2] Some authors use Fourier analysis to extend the sinusoidal method to non-sinusoidal waveforms.

Proximity Effect

Up to this point a single isolated conductor has been considered. Its magnetic field extends radially in all directions, and conduction occurs across the entire surface.

When another conductor is brought into close proximity to the first, their fields add vectorially. Field intensity is no longer uniform around the conductor surfaces, so high frequency current flow will not be uniform.

For example, if the round wire of Fig. 1 is close to another wire carrying an equal current in the opposite direction (the return current path?), the fields will be additive between the two wires and oppose and cancel on the outsides. As a result, high frequency current flow is concentrated on the wire surfaces facing each other, where the field intensity is greatest, with

little or no current on the outside surfaces where the field is low. This pattern arranges itself so as to minimize the energy utilized, hence inductance is minimized. As the wires are brought closer together, cancellation is more complete. The concentrated field volume decreases, so the inductance is reduced.

Circuit wiring: The field and current distribution with round wires is not easy to compute. A simpler and more practical example is given in Figure 5. The two flat parallel strips shown are actually the best way to implement high frequency wiring, minimizing the wiring inductance and eddy current losses. These strips could be two wide traces on opposite sides of a printed circuit board. (Don't use point-to-point wiring. It is much more important to collapse the loop and keep the outgoing and return conductors as intimate as possible, even if the wiring distances are greater.)

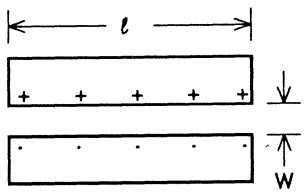


Fig. 5 - Circuit Wiring - Flat Parallel Strip

The + signs indicate current flow *into* the upper strip, the · indicates current *out* of the lower strip. Between the strips, the magnetic field is high and uniform, so the current is spread out uniformly on the inner surfaces. On the outside of the strips the field is very low, so the current is almost zero. This results in the minimum possible energy storage (and wiring inductance) for this configuration. If the breadth of the strip, ℓ, is much greater than the separation, w, the energy is almost entirely contained between the two strips. Then ℓ and w are the length and width of the field, and can be used to calculate the inductance. Converting Eq. (4) to cm and with N = 1 turn, the inductance per centimeter length of the 2-conductor strip is:

$$L = 12.5\, w/\ell \quad \text{nH/cm} \qquad (7)$$

If the strips have a breadth of 1 cm and are separated by 0.1 cm, the combined inductance of the pair is only 1.25 nH for each centimeter length, divided equally between each of the two conductors. If one conductor is much wider than the other, such as a strip vs. a ground plane, most of the inductance calculated in (6) is in series with the narrower conductor. This is good for keeping down noise in the ground returns.

Note that current penetration is from one side only -- the side where the field is. This means that a strip thicker than the penetration depth is not fully utilized. The equivalent circuit model of Fig. 4 still applies, with A at the surface adjacent to the field. But B becomes the *opposite* side of the strip, not the center, since there is no penetration from the side with no field.

Bad practice: Figures 6 and 7 show what *not* to do for circuit wiring (unless you want high inductance and eddy current losses). Although these strips have large surface areas, proximity effects in these configurations result in very little surface actually utilized. Remember that the field is concentrated directly between the two conductors so as to minimize the stored energy.

In Fig. 6 this results in current flow only at the *edges* facing each other. Also, because the concentrated field region is short, the energy density is very high, and the inductance is several times greater than in Fig. 5.

The Fig. 7 configuration is not *quite* as bad as Fig. 6 because the current does spread out somewhat in one of the two conductors, but it is still many times worse than the proper configuration in Fig. 5. The message is: large

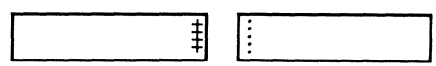


Fig. 6 - Bad Wiring Practice - Side by Side

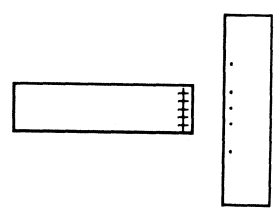


Fig. 7 - Bad Wiring Practice - Right Angled

surface area doesn't improve high frequency performance if the configuration is wrong.

Inductor Windings: Figure 8 is a simple inductor. The winding consists of 4 turns in a single layer. Assuming a current of 1 Ampere through the winding, the total magneto-motive force $F = NI$ along any path linking the 4 turns is 4 Ampere-turns. The field is quite linear across the length of the window because of the addition of the fields from the individual wires in this linear array. The winding could have been a flat strip carrying 4 Amps with the same result.

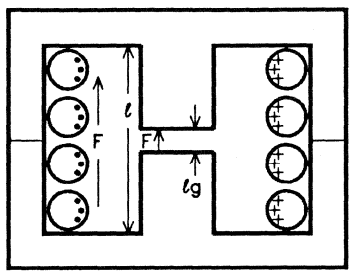


Fig. 8 - Inductor Winding

Without the ferrite core, the field outside of the winding would have been weak because of cancellation, but with the high permeability core, the external field is completely shorted out. This means the entire field, $F = NI$ is contained across the window inside the winding. Field intensity, H equals NI/ℓ. In the center, the entire field is compressed across the small air gap. Field intensity ($H_g = NI/\ell_g$) is therefore much greater within the gap, so the energy stored in the gap (using Eq. 2 or 3) is much greater than the energy in the much larger window.

At high frequency, current flow is concentrated on the inner surface of the coil, adjacent to the magnetic field. The field outside the coil is negligible, so no current flows on the outer surface.

Transformer Windings: Figure 9 shows a transformer with a four turn single layer primary and a 1 turn single layer copper strip secondary. In any transformer, the sum of the Ampere-turns in all windings must equal zero (except for a small magnetizing current which

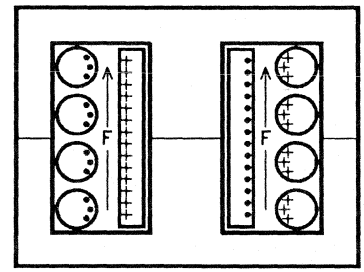


Fig. 9 - Transformer Windings

is neglected). So if the secondary load current is 4 A through 1 turn, the primary current through 4 turns must be 1 Amp. The fields tend to cancel not only outside both windings, but in the center of the two windings as well. Whatever field might remain is shorted out by the high permeability core which has no gap. Thus the field generated by the current in the windings, $F = 4$ A, exists only *between* the windings. So at high frequency, current flow is on the outside of the inner winding and on the inside of the outer winding, adjacent to the field.

Multiple Layer Windings

Figure 10 shows a transformer with multi-layer windings and its associated *low frequency* mmf (F) and energy density diagrams. One half of the core and windings are depicted. At low frequency, current (not shown) is uniformly distributed through all conductors, because they are much thinner than the penetration depth.

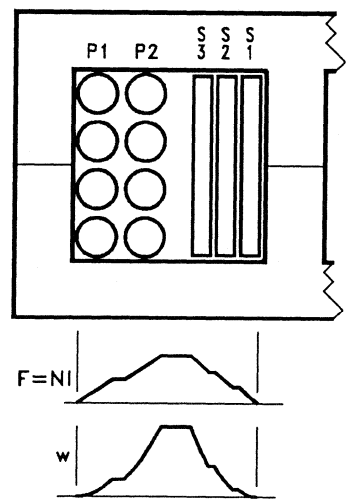


Fig. 10 - Multiple Layer Winding

The primary winding has 8 turns arranged in two 4-turn layers, while the secondary has 3 turns of copper strip in 3 layers. With 2 Amp load current, the secondary has 3T · 2A = 6 A-T. The primary must also have 6 A-T, so primary current is 0.75 A.

As shown in the mmf diagram below the core in Fig. 10, there is no field outside of the primary or inside the secondary, but starting at the outside of the primary and moving toward the center, the field rises to its maximum value between the two windings. With uniform current distribution at low frequency, note how the field builds uniformly within each conductor according to Faraday's law, staying constant between the conductors. The energy density in the field goes up with the square of the field strength, as shown below the mmf diagram. The area under the energy density curve is the total leakage inductance energy stored in and between the windings.

So multiple layers cause the field to build. At high frequencies, it will be shown that the eddy current losses go up exponentially as the number of layers is increased. The number of layers should be kept to a minimum by using a core with a long narrow window to accommodate all the turns in fewer layers (this also causes a dramatic reduction in leakage inductance). The window shape illustrated in Fig. 10 is far from optimum.

Interleaved Windings: Another way to reduce the effective number of layers is to break up the winding into smaller sections through interleaving, as shown in Figure 11.

With interleaving, each winding is essentially divided into two or more sections, as shown on each side of the dotted line in Fig. 11. The primary now has two sections a and b, each with 1 layer of 4 turns. The secondary is also divided down the middle into two sections of 1 ½ layers, 1 turn per layer. (This is why half layers are included in eddy current loss curves.) Note that the 2 amperes through the 1 ½ turns of secondary section (a) cancels the 0.75 A, 4 turns of primary section (a), and the field goes through zero in the middle of the center secondary turn at the dotted line. *F* builds up to only half the peak value compared to Fig. 10, and reverses direction between alternate winding sections. It will be shown that the reduced field causes a great reduction in eddy current losses.

Because of the reduced field, the total energy under the energy density curve in Fig. 11 is only 1/4 the total energy in Fig. 10. Thus, interleaving reduces the leakage inductance by a factor of 4!

Multiple layers at high frequency: Figure 12 is an enlarged section of Fig. 10 but at a high frequency where the penetration depth is 20% of the secondary winding strip thickness. The field strength and current density are the same as at low frequency in the spaces between the conductors. But *within* the conductors, current density, magnetic field and energy density all fall off rapidly moving in from the surface. (Dash lines show low frequency distributions.

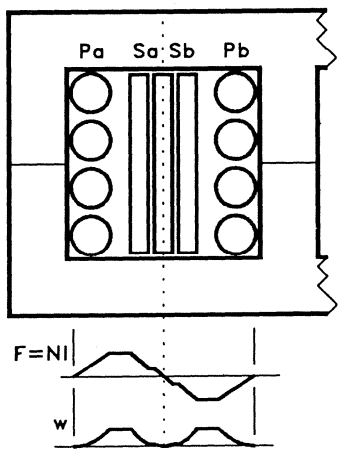


Fig. 11 - Interleaved Windings

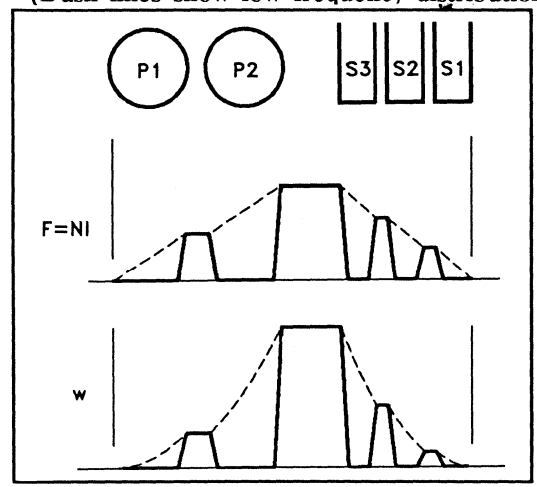


Fig. 12 - Multiple Layers at High Frequency

The heavier lines showing the high frequency distributions are approximations based on the current distribution ending abruptly at the penetration depth. Actually, the slopes are steeper at the surfaces, and tail off within the wire.)

Notice that the total energy under the energy density curve is about half the amount at low frequency. This means the leakage inductance has decreased at high frequency, but only because the energy within the conductors is practically eliminated. This is not a very practical way to reduce leakage inductance -- the penalty is a huge increase in eddy current losses.

With the penetration depth 20% of the strip thickness, the ac resistance might be expected to be 5 times the dc resistance. But with three layers building up the field, the ac resistance is actually 32 times greater!

Why multiple layers cause high losses:

Figure 13 is an even more enlarged view of the 3 secondary layers of Fig. 12, together with their high frequency mmf diagram. Assume a current of 1 Ampere through the 3 layer winding. There is only one turn (strip) per layer.

To the right of layer S1, the mmf is 0. At the left of S1, F=1 A-T. The 1 Amp current in S1 is crowded into the 20% penetration depth adjacent to the field. Field F also cannot penetrate more than 20% into S1. This 1 A-T field exists only between S1 and S2. F cannot penetrate S2, either. It must terminate on the right side of S2, but it cannot just magically disappear.

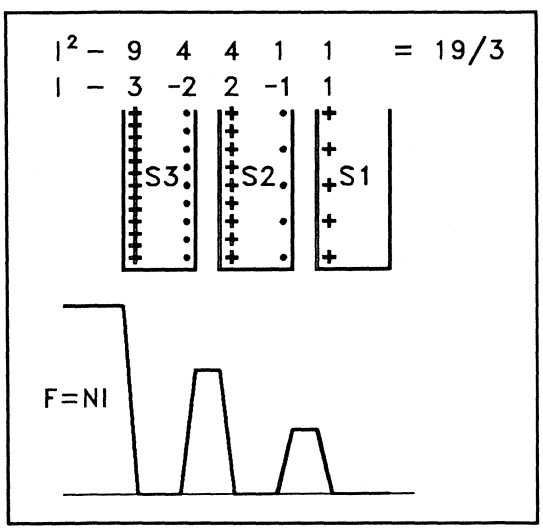


Fig. 13 - Surface Currents

According to Faraday's law, for the mmf to be zero in the center of S2, the enclosed current must be zero. This requires a current of 1 Amp on the right surface of S2 *in the opposite direction to normal current flow* to cancel the 1 Amp in S1. Then, to achieve the 2 A-T field to the left of S2 requires a surface current of 2 Amps! (The net current in S2 is still 1 Amp.)

The 2 A-T field must be terminated at the right side of S3 with 2 A reverse current flow. Then 3 Amps must flow on the S3 left surface to support the 3 A-T field and to conform to the net 1 Amp through the winding.

If the current in each layer were just the 1 Amp, limited in penetration to 20% of the conductor thickness, the ac to dc resistance ratio, F_R, would be 5:1. But the surface currents in successive layers become much larger, as discussed above. The tabulation above the conductors in Fig. 13 gives the current at each surface and the current squared, which indicates the relative power loss at each surface. The two surfaces of S2 together dissipate 1+4 = 5 times as much as S1, while dissipation in S3 is 4+9=13 times S1!

The average resistance of the 3 layers is (9+4+4+1+1)/3 = 19/3 = 6.333 times the resistance of layer S1. Since the ac resistance of S1 is already 5 times the dc resistance (because of the 20% penetration depth), the ratio of average ac resistance to the dc resistance, F_R, is 31.67 : 1. Hardly negligible.

Referring to S3 with 3A and -2A at its surfaces, if conductor thickness is decreased or if frequency is decreased to improve penetration, the penetration "tails" of these opposing currents will reach across and partially cancel. When D_{PEN} is much larger than the conductor thickness, cancellation is complete, conductor current is 1 Amp uniformly distributed, and F_R = 1.

Although each layer was a 1 turn strip carrying 1 Amp in this illustration, each layer could have been 10 turns carrying 0.1 Amps with the same results.

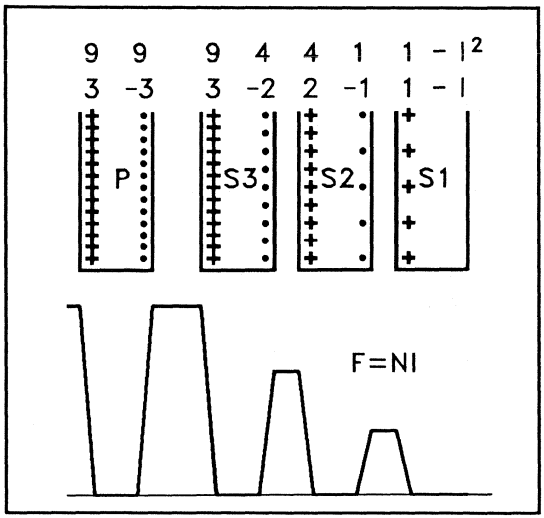


Fig. 14 - Passive Winding Losses

Passive layers: A passive layer is any conductor layer that is not actively "working" by carrying net useful current. Faraday shields and the non-conducting side of center-tapped windings are examples of passive layers.
Figure 14 shows what happens if a Faraday shield is inserted in the 3 A-T field between the secondary winding of Fig. 13 and the primary (off to the left). If the Faraday shield thickness is much greater than D_{PEN}, 3 Amps must flow on each surface because the field cannot penetrate. At each surface, I^2 is 9 Amps squared, and both surfaces together dissipate 18 times as much as S1, or almost as much as all three secondary turns combined.

Faraday shields are always located where the field is highest. Their thickness should be less than 1/3 of D_{PEN} keep the loss to an acceptable level.

For another example, consider a center-tapped secondary with sides A and B each side of the center-tap. If A is physically between B and the primary, A is a passive conductor in the high field region when B is conducting, but B is outside the field when A conducts. The *additional* passive dissipation in A will probable exceed the active dissipation in either A or B. This is one reason that single-ended transformers overtake or even surpass push-pull and half-bridge versions at frequencies above a few hundred kHz.

Paralleled windings: When ac resistance of a strip secondary winding is too high because the required strip thickness is too great, it is tempting to simply subdivide it into several thinner strips, insulated from each other. This doesn't work -- the parallel combination will have the same losses as an equivalent solid strip. This is because the individual thin strips occupy different positions in the field, causing eddy currents to circulate between the outer and innermost strips where they are connected in parallel at their ends, similar to what happens in a single solid strip.

Conductors can be successfully paralleled only when they experience the same field, averaged along their length:

1. Wires in the same layer can be paralleled, as long as they progress together from one layer to the next.
2. Litz wire -- fine wires woven or twisted in such a manner that they successively occupy the same positions in the field.
3. Portions of a winding at comparable field levels in different interleaved sections can be paralleled. For example the two four-turn primary sections in Fig. 11 could be paralleled. The field must remain apportioned equally between in the two sections or much more energy would be required. If the secondary in Fig. 11 were a single solid turn, it could be divided into two thinner paralleled turns.

Calculating ac resistance: It has been shown that it is not difficult to calculate F_R when the conductor thickness is much greater than the penetration depth. It is also easy when the conductor thickness is much less than D_{PEN} -- $F_R = 1$. But the condition of greatest interest to the transformer designer is when the conductor thickness is in the same range as D_{PEN}, and here the calculations are quite difficult.

Dowell solved the problem for sinusoidal waveforms in his 1966 paper.[2] The curves in Figure 15 are derived from Dowell's work. The vertical scale is F_R, the ratio of Rac/Rdc. The horizontal scale, Q, is the ratio of the effective conductor height, or layer thickness, to the penetration depth, D_{PEN}. For strip or foil windings, the layer thickness is the strip thickness. For round wires touching each other in the layer, the effective layer thickness is 0.83 times

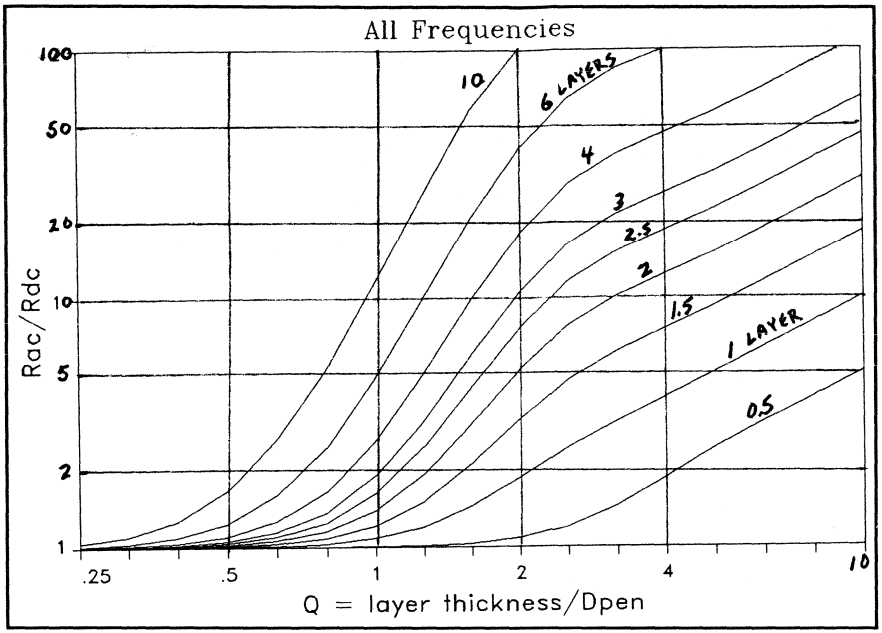


Fig. 15 - Eddy Current Losses - R_{AC}/R_{DC}

the wire diameter. For round wires spaced apart in a layer, the effective layer thickness is $.83 \cdot d \cdot (d/s)^{1/2}$, where d is wire diameter and s is the center-to-center spacing of the wires.

Referring to the calculation of F_R = 31.67 on page 7, enter Fig. 15 with Q=5 and 3 layers. The resulting F_R value agrees.

At the extreme right of Fig. 15 is the region where the conductor thickness is much greater then D_{PEN} and F_R is very large. The curves are parallel and have a +1 slope. On the extreme left, conductor thickness is much less than D_{PEN} and F_R approaches 1.0. In the center of the graph, the curves plunge downward as Q gets smaller. An F_R of 1.5 is a good goal to achieve. With a much higher value, losses hurt too much. To go much below 1.5 is past the point of diminishing returns, requires much finer conductor sizes. Achieving F_R of 1.5 requires a Q value ranging from 1.6 with 1 layer, to 0.4 with 10 layers.

Starting with a conductor thickness much greater than D_{PEN} and subdividing into smaller conductors usually makes F_R worse before it gets better. For example, assume a single layer winding of 10 close spaced turns, and a Q of 4. F_R from the Fig. 15 is 3.8 -- not good enough. If four parallel wires of half the diameter are substituted for the original wire (taking care to handle this properly), there will be 40 wires, 20 per layer, 2 layers deep. Q is now 2. Entering Fig. 15 at Q=2 and 2 layers, F_R is 5.2 -- it went up! The reason for this is the wire size is still too large for effective penetration and cancellation of the eddy currents, and the number of layers has been doubled with the extra eddy current surfaces this generates.

Subdividing again into 16 parallel wires of 1/4 the original diameter there are 160 total wires, 40 per layer, 4 layers deep. Q is 1 and F_R is down to 2.8.

A third subdivision to 64 parallel wires with 1/8 the original diameter results in 640 total wires, 80 per layer, 8 layers. Q is 0.5 and F_R finally reaches 1.5.

Non-sinusoidal waveforms: Venkatramen[3] and Carsten[4] have applied Dowell's sine wave solution to various non-sinusoidal waveforms more relevant to switching power supplies. This is done by taking the Fourier components of the current waveform, then using Dowell's approach to calculate the loss for each harmonic and adding the losses. They have also redefined the way the data is presented in an attempt to make it more useful.

Their curves show that as the pulse width narrows, the effective ac resistance goes up because the higher frequency harmonics are more important. But the worst losses are not at narrow pulse widths. In most switching supplies, the *peak* pulse current is constant (at full load). The high frequency harmonics and losses are much the same regardless of pulse width, but the total rms, the dc and low frequency components get much worse as the pulse width widens. Worst case for total copper

losses is probably near a duty ratio of 0.5.

In applications where current pulse widths in the vicinity of 0.5 duty ratio are the worst case conditions for copper losses, a shortcut method to achieve satisfactory results is to design the winding for an F_R of 1.5 at the fundamental of the current waveform, then allow an extra 30-50% for additional losses due to the high frequency components.

References

[1] D. G. Fink et al, *Electronics Engineer's Handbook,* McGraw-Hill, 1975

[2] P. L. Dowell, "Effects of Eddy Currents in Transformer Windings," *Proceedings IEE (UK),* Vol. 113, No. 8, August, 1966, pp. 1387-1394.

[3] P. S. Venkatramen, "Winding Eddy Current Losses in Switch Mode Power Transformers Due to Rectangular Wave Currents," *Proceedings of Powercon 11,* 1984, Sec. A1.

[4] B. Carsten, "High Frequency Conductor Losses in Switchmode Magnetics," *High Frequency Power Converter Conference,* 1986, pp. 155-176

Appendix I -- Litz Wire

In switching power supply transformers, if the conductor thickness is similar to or greater than penetration (skin) depth at the operating frequency, ac current flows in only a portion of each conductor, resulting in high ac losses. This effect is magnified exponentially the more layers there are in the winding. To bring the ac losses back down to an acceptable level, the conductor thickness must be reduced.

Thin strip with a width equal to the winding width is often used, especially for low voltage, high current windings with few turns and large conductor area. Each turn is a layer and each turn must be insulated from the others. Strips cannot be subdivided into several paralleled thinner strips unless the individual strips are in different winding sections, otherwise unequal induced voltages will cause large eddy currents to circulate from one strip to another and losses will be high.

When strip or foil is not appropriate for a winding, the conductor can be divided into multiple strands of fine wire which are then connected in parallel at the terminations of the winding.

All wires in the group must be individually insulated and must encompass the identical flux to avoid eddy currents circulating from one wire to another through their terminating interconnections. If only a few wires in parallel are to be used, they can be laid together side-by-side (as though they were tied together as a flat strip). Each wire must have *exactly* the same number of turns as the other wires within *each layer*, to avoid cross-circulating eddy currents. This is not practical when large numbers of fine wires must be used.

Another solution is to interweave or twist the wires together in such a manner that each wire moves within the group to successively occupy each level within the field. But when this is done properly, voids are introduced, resulting in poor utilization of the available winding area compared with closely packed (untwisted) conductors.

Low power, high frequency Litz wire is usually woven from very fine wires, but the woven structure results in a large percentage of voids and poor copper utilization. Litz wire for power applications is usually made with a few wires twisted together in a strand and a few of these strands twisted into bigger strands, etc. The amount of twist required is moderate -- not enough to significantly increase the strand diameter or the length of the individual wires.

Consider a bundle of seven wires twisted into a strand, with one wire in the center. The packing structure is hexagonal -- as efficient as possible, with an outer surface which is almost circular. The amount of copper in this strand is .778 of a single solid wire with the same max. diameter as the strand. The outer six wires rotationally occupy each of the outside positions, but the center wire is fixed in its location. ac losses are actually improved by eliminating the seventh, inner wire. (In practice, it should be replaced by a non-conductive filler to maintain the shape of the strand.) This reduces the winding area utilization factor to .667 of the equivalent solid wire.

Even solid wire does not achieve 100% utilization of the winding area. The bottoms of the wires in each layer ride diagonally across the tops of the wires in the layer below, so they cannot pack down into the valleys between the wires below, except in a limited and unpredictable way. This means that round wire occupies the area of a square with sides equal to wire diameter, hence the utilization is pi/4, or .785. If a six-wire strand described above is substituted for the solid wire, overall utilization is further reduced to .785•.667 = .524.

Table I shows the utilization factor of 3 to 6-wire strands. Although the utilization factors are quite similar, it will be shown that they do not perform equally well in achieving a multistrand cable with a large number of wires.

TABLE I
Utilization Factor of Single Strands

Number of Wires:	3	4	5	6
Utilization Factor:	.65	.686	.685	.667

It is not unusual to require *hundreds* of fine wires in parallel to achieve the required dc and ac resistances at 100 kHz or higher. This requires that strands be twisted into larger strands, and these twisted with each other, progressing to a cable containing the total number of fine wires needed to carry the desired high frequency current. The effective diameter of each strand is the circle of rotation of the outer extremities of the wires. Each level of twisting further reduces the utilization factor. As shown in Table II, much better utilization is achieved when more wires/strands are twisted together at one time, because fewer levels of twisting are required to achieve a similar number of wires.

For example, with 4 strands/twist, 4 wires twisted comprise a Level 1 strand, four Level 1 strands are twisted to obtain a Level 2 strand having 16 wires. Four Level 2 strands are then twisted resulting in a Level 3 strand with 64 wires, etc. Add levels until the desired number of wires is reached.

The utilization factors of Table II are further reduced by pi/4 (.785) because round cable made according to Table II occupies a square portion of the winding space.

Instead of making up one cable containing all of the wires needed, it is often advantageous not to twist the final level. This may provide greater flexibility in fitting the winding to the available breadth and height, and improves the utilization factor by eliminating one level of twisting.

For example, assume 256 wires of a given diameter are required. This could be achieved in one Level 4 cable using 4 strands/twist and 4 twist levels. The utilization is .22 compared with solid wire the same diameter as the cable, and .22•.785 = .17 of the winding space is copper. However if 4 Level 3 cables are used in parallel, the utilization is .32 compared to solid wire, and .32•.785 = .25 of the occupied winding area. Remember that *each of the paralleled cables must have the same number of turns in each layer.*

Insulation on the wires further reduces the utilization, especially with fine wires whose insulation is an increasing percentage of the wire area. With more and more turns of finer wire, the total area of the winding must increase if the desired copper area is maintained. When the maximum available window area is reached, improvement may still be obtained by going to more turns of finer wire, even though the dc resistance will increase, if the reduction in ac resistance is sufficient. Otherwise, the only solutions are: (a) Let the transformer run hotter, or (b) use a larger size core which will provide a bigger window (and fewer turns are usually required).

TABLE II

Utilization Factor vs. Twist Levels

# Strands/Twist:	3		4		5		6	
	Wires	Util.	Wires	Util.	Wires	Util.	Wires	Util.
Level 1	3	.65	4	.69	5	.69	6	.67
Level 2	9	.42	16	.47	25	.47	36	.44
Level 3	27	.28	64	.32	125	.32	216	.30
Level 4	81	.18	256	.22	625	.22	1296	.20
Level 5	243	.12	1024	.15				

Notes

Notes

Design Reference Addenda

Design Reference Addenda

Design Review: A 300W, 300KHz Current-Mode Half-bridge Power Supply with Multiple Outputs using Coupled Inductors

Table of Contents

Introduction

This paper gives a practical example of the design of an off-line switching power supply. The half-bridge topology is used with current mode control. Until recently this was considered an unstable combination, but a simple compensation circuit is now available and is described in this paper. This power supply has two outputs and uses a coupled inductor. Using a coupled inductor with a current mode controlled buck type topology is especially helpful, as will be explained later.

Specifications

Topology: Half Bridge

Mode: Current Mode

Output: 5V ± 1%, 10 to 50A, ripple v = 100mV pp max
15V ± 5%, 1A to 4A, ripple v = 200mv pp max

Frequency: 300KHz (600KHz oscillator)

Efficiency: 75%

Input: 110/220VAC

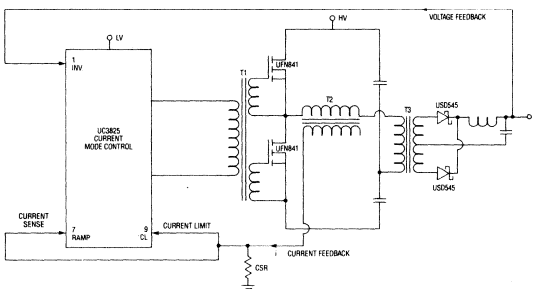


Figure 1. Simplified Schematic Showing Voltage Feedback and Current Mode Pat

Topology — Half Bridge with Current Mode Control

Advantages of Half Bridge:

1. Voltage rating of switching devices is one-half that required by Flyback or Forward converter.
2. Output filter inductor helps capacitor (compared to flyback)
3. More efficient use of transformer core and copper.
4. Leakage inductance energy is returned to the input capacitor instead of being dissipated in resistive snubbers.

Advantages of Current Mode:

1. Removes one pole of half bridge's 2 poles.
   a. Easier to compensate.
   b. Better large signal performance from error amplifier.
2. Gives input voltage feed forward. (Good output regulation for input line changes.)

The Stability Problem of the Half Bridge Topology Using Current Mode Control (Refer to Figure 3)

Assume that Q2 closes with a longer pulse width than Q1. Current mode control keeps the peak current equal, so the amount of charge transferred from C2 is more when Q2 is closed. As a result the voltage at node 2 will decrease. The next time Q2 closes the voltage across the primary will be less so the current ramp will have a slower slope. The peak current will be kept the same, so the pulse width will be wider. This means that the node 2 voltage decreases even further, and eventually reaches zero. It is this stability problem that has prevented the widespread use of the half-bridge topology with current mode control. Fortunately there is a simple solution to this problem, using an auxiliary transformer winding made of small diameter wire with the same number of turns as the primary winding, and two small high voltage diodes. The credit belongs to an unknown engineer who attended one of our seminars in 1984.

Operation of the Correction Circuit

Assume that node 2 is low by 1 volt, at 49.5V. When Q1 closes, the primary voltage is V_{CC} – V node 2 = 100V – 49.5V = 50.5V. The auxiliary winding also has 50.5V across it, by transformer action, with the polarity as shown. Diode D1 will hold node 3 at approx. 0 volts. The other end of the aux. winding, node 2, will try to go to +50 volts. However, as node 2 voltage approaches 50 volts (from its original value of 49V) the voltage across the primary will also approach 50 volts.

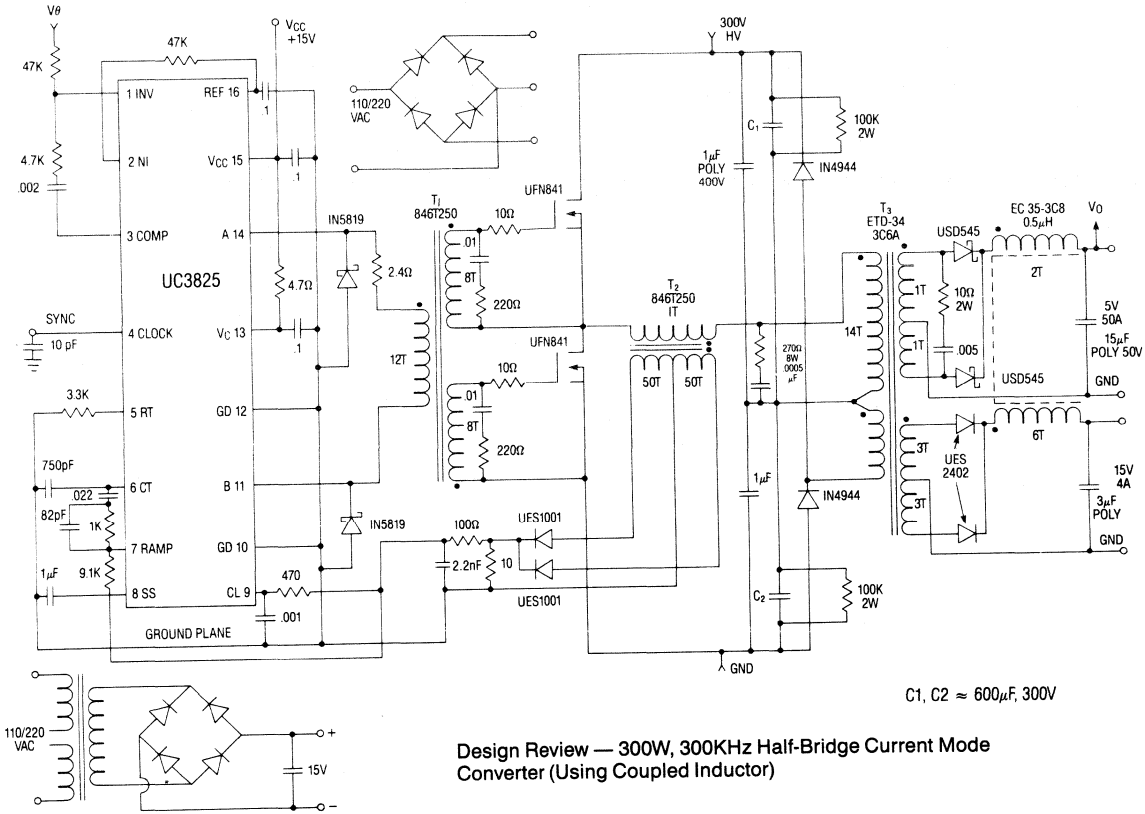
If Q2 closes when node 2 is low, no corrective action takes place. Corrective action takes place when the other half of the cycle occurs, ie, when Q1 closes again. If node 2 is high, corrective action occurs when Q2 is closed.

PWM Controller

The PWM controller used is the UC3825, a high speed 1MHz chip with voltage or current mode capability, dual high current 1.5A totem pole outputs, 50ns propagation for shutdown during fault conditions, and other desirable features. It is somewhat similar to the UC3525A and UC3526A, with the addition of much faster speed and current mode capability.

Control and Gate Drive Circuits (See Figure 2)

The MOSFET gate drive circuit consists of the dual totem pole outputs of the UC3825 driving a small toroidal transformer with two secondaries having opposite polarity outputs. There are several advantages to this type of drive; first, no coupling capacitors are needed because of the balanced drive, and second, during off time both ends of the primary are grounded, preventing transients from turning on the MOSFETs.



Design Review — 300W, 300KHz Half-Bridge Current Mode Converter (Using Coupled Inductor)

Figure 2.

T1 uses a Ferroxcube toroid, the 846T250-3C8, which has an A_L = 1650 mH/1000T. For 12 turns, $L_P = A_L \times N^2$ = $(12/1000)^2 \times 1650$ mh = 230μH. Magnetizing current = i_M = di = edt/L = 15V × 1.5μs/230μH = 100 ma. This current passes through the A and B outputs of the UC3825, and creates power dissipation which needs to be minimized while keeping a low value of leakage inductance. The leakage inductance needs to be low in order to get fast risetimes and low delay time.

The ability of the core to handle the required energy without saturating is important. The circuit energy is

$1/2\ L_M I_M^2 = 1/2 \times 230\mu H\ (100ma)^2 = 1.2\mu J.$
The core can store

$$W = \frac{B^2 Ae\ le \times 10^{-8}}{2u_e} = \frac{2500^2 \times .259 \times 5.42 \times 10^{-8}}{2 \times 2700} = 16\mu J$$

(For explanation of magnetic terms refer to Section M in back of this manual). Mylar tape can be used to insulate between the primary and secondary windings.

The UC3825 outputs A and B see an inductive load, eg, the leakage inductance of the transformer. The energy stored in this inductance can drive the outputs negative during turn-off, which can impair the functioning of the chip. Schottky diodes from ground to each output will assure proper operation.

The inductance at the transformer secondaries in conjunction with the MOSFET gate capacitance will cause ringing at the gate, which could turn the MOSFET on during off-time. Resistive damping (with a small series dc blocking capacitor to reduce power dissipation) is used at each gate.

When discussing PWM controllers and gate drive circuits, especially at higher frequencies, remember that the design must start with a good ground plane, located as close to the PWM chip terminals as possible, and all components should have leads as short as possible. Supply voltages and reference voltages should be by-passed at the PWM chip terminals, and the single point ground concept should be used, especially for PWM chip signal ground, chip output ground and gate drive ground.

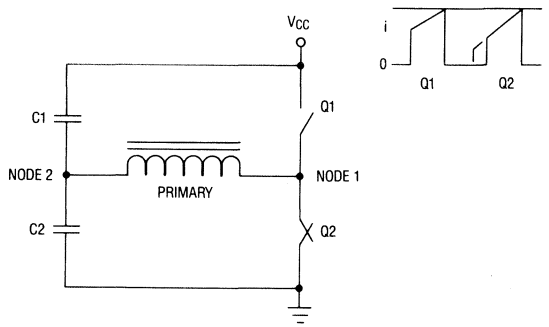


Figure 3.

Power Stage

This part of the design selects the power MOSFETs and calculates the amount of heat sinking needed.

$$I_{pri} = \frac{P_O}{V_{in} \times \text{Eff.} \times \text{D.F.}} = \frac{300W}{100V \times 0.75 \times 0.9} = 4.45A,$$

(where D.F. is the Duty Factor)

I_{pri} is time shared by the two MOSFETs

I_{pri} = 4.45A plus 10% safety margin = 4.9A

$V_{PRI\,(max)}$ = 385V

From the TO-220 MOSFET selection guide in the catalog, the UFN841 is rated at 450V, and 5.0A continuous at 100°C case. Since each of the MOSFETs will carry the 4.9A for less than half of a cycle, the current rating is OK.

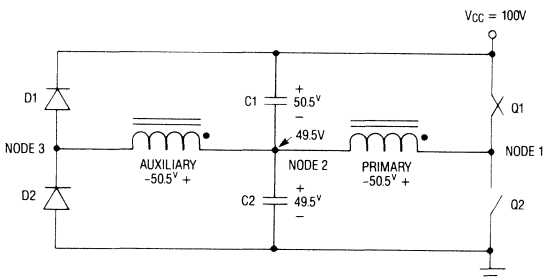


Figure 4.

The junction temperature rise due to dissipation in $R_{DS\,(ON)}$ during ON time should be decided (55°C) and the amount of heat sinking needed should be decided, 55°C. The fact that the $R_{DS\,(ON)}$ increases with temperature has to be factored into the calculations. From the data sheet curve that factor is 1.5 at 80°C.

$P_D = I^2 R_{DS\,(ON)} \times \text{D.F.} = 4.9^2 \times (0.80 \times 1.5) \times 0.45 =$ 12.9W average

where $R_{DS\,(ON)}$ is at T_j of 80°C (55°C rise)

$$R\Theta_{JA} = \frac{\triangle T_j}{P_D} = \frac{55°C}{12.9W} = 4.3°C/W$$

Two heatsinks 2″ x 2.3″ piggybacked will have a thermal resistance of 3°C/W. The TO-220 will add 1°C/W for a total of 4°C/W, just under the value required.

Power Transformer Design

First the approximate value of flux is determined. It is expected that at 300KHz it will be core loss limited. The allowable temperature rise of the transformer is decided, 40°C. The core and copper loss are made equal as a first approximation. It is planned to use the Ferroxcube ETD series of cores.

Temperature rise due to core loss = $\frac{40°C}{2}$ = 20°C

RΘ of ETD-34 (smallest ETD) = 19°C/W

$$P = \frac{20°}{19°C/W} = 1.05W$$

$$\frac{P}{Vol} = \frac{1.05W}{7.64cm^2} = 140\ mw/cm^2$$

For 3C6A core loss curve at 140mw/cm²

B_{max} (at 300KHz) = 600GAUSS

$\triangle B = 2B_{max} = 2 \times 600G = 1200G$ pk to pk
= 0.12 Tesla

Now the core size can be selected, using the area product method. (Refer to Section M5 for a similar method.)

$$\text{Area product } AP = A_w A_e = \frac{11.1\ Pin\ 1.143}{K \triangle B\ F}\ cm^4$$

$$= \frac{11.1 \times 300W / 0.75^{1.143}}{(1 \times 0.3 \times 0.41) \times 0.12T \times 300KHz} = 1.03cm^4$$

For ETD-34, $AP = A_e A_W = 0.971cm^2 \times 1.22cm^2$
$= 1.18cm^4$

Minimum number of primary turns to support the primary voltage at the frequency selected.

$$N_{pri} = \frac{V_{pri\,(min)} \times 10^4}{2F \triangle B\ Ae} =$$

$$\frac{100V \times 10^4}{2 \times 300K \times 0.12T \times 0.971cm^2} = 14.2 \text{ turns minimum}$$

Turns ratio: Primary to 5 volt secondary

$$N = \frac{N_p}{N_s} = \frac{k\,[V_{in\,(min)} - V_{(on)}]\ \text{D.F.}}{V_O + V_F}$$

where k is allowance for inaccuracies, IR drops and delays.

$$= \frac{0.9\,(100-3.2)\,0.9}{5 + 0.55} = 14.1$$

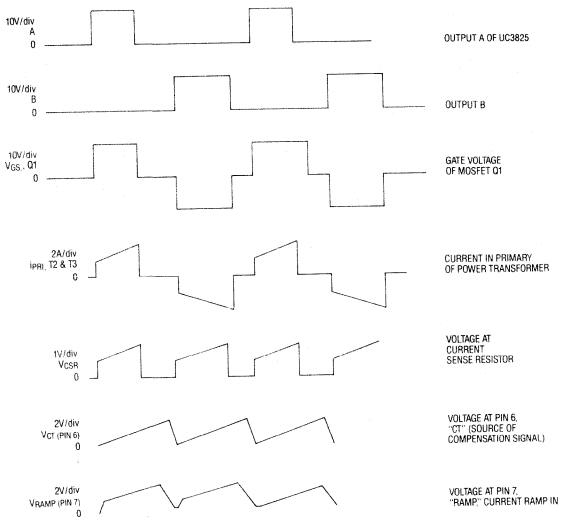


Figure 5.

Since 5V and 15V are required, the secondary turns ratio needed is approximately 3 to 1 (Approx. because of rectifier drops). The primary will have 14 turns, and the 5V secondary will have 1 turn (C.T.), in order to minimize copper volume and loss and window area needed. The 15V secondary will have 3 turns (C.T.) and an output of 15.5 volts.

Primary (See Sections M5 and M2)

$$I_p\,(max) = I_{in}\,(max)/K_t = \frac{P_{in}\,(max)}{V_{in}\,(min) \times K_t} = \frac{300/.75}{100 \times 1} = 4.0A$$

$$J\ max = 450\,(AP)^{-0.125} = 450 \times 1.18^{-0.125}\ 450 \times 0.98 = 440A/cm^2$$

$A_{xp} = I_p(max) / J\ max = 4.0/440 = .009\ cm^2 = \#17AWG$

Depth of penetration at 300KHz = .013 cm, diameter of #17 is 0.115 cm

Use 20 × #32 in parallel. (Twisted.) See Section M2 for eddy current loss curves. Wind in two banks, one bank on each side of the secondary windings. This is termed interleaving. It reduces leakage inductance by a factor of 3.

5V Secondary

$I_S(max) = I_O(max) / 1.414 = 50A / 1.414 = 35A$

$Ax\,(sec) = I_S(max) / J\ max = 35 / 440 = 0.079cm^2$

Use copper strap 10 mils × 0.8″ = .008 sq in = $0.052cm^2$

Area OK since strap is better than wires.

Check eddy current loss factor; Dpen = 7.5/f (1/2) = 7.5 (300K) 1/2 = .013cm = 5 mils. Strap is 10 mils thick. Primary is interleaved around secondary so depth is 5 mils in from each side for a total of 10 mils.

15V Secondary

$I_S(max) = I_\Theta(max) / 1.414 = 4A / 1.414 = 2.82A$

$Ax = I_S(max) / J\ max = 2.82 / 440 = .0064cm^2$

Use copper foil 3 mils thick × 0.3 inches wide.

Losses and Temperature Rise of Transformer

$P_w = 2\ I_P^2 N_P 1_t R = 2 \times 4^2 \times 14 \times 6.0 \times .00028 =$ 0.66 watts (pri & sec)

For 3C6A, loss = 1.05W

$Pt = Pw + 0.66 + 1.05 = 1.71W$

For ETD-34, $R\Theta = 19°C/W$

$\triangle T = P_T \times R\Theta = 1.71W \times 19°C/W = 32.5°C$ rise (less than 40°C is OK)

Current Sense and Slope Compensation

Known circuit values:

Power transformer turns ratio = 14
Current sense transformer turns ratio = 50
Maximum primary current = 4.0A
Voltage threshold at current limit pin of UC3825, 1.0V
T_{ON} of UC3825 at 600KHz = 1/600K – 0.1μs deadtime = 1.57μs

For current sense circuit:

$$I_{SEC} = \frac{I_{pri}}{N} = \frac{4.0A}{50} = 0.080A$$

Using margin of 20%

$$R_{CSR} = \frac{V_{th}}{1.2\ I_{sec}} = \frac{1.0V}{0.08 \times 1.2} = 10\ ohms$$

Slope compensation, from current slope of 5V output inductor, to ramp input (Pin 7) of UC3825, and from C_T (Pin 6)

$di/dt\ (sec) = V_{sec}/L = 5.7V/0.5\mu H = 11.4A/\mu s$

$$di/dt\ (pri) = \frac{11.4A/\mu s}{14} = 0.81A/\mu s$$

$$V_{slope}\ at\ CSR = \frac{di/dt\ (pri)}{50} \times R_{CRS}\ \frac{0.81 \times 10}{50} = 0.16V/\mu s$$

V_{osc} slope at pin 6 = 1.8V/1.57μs = 1.15V/μs

$$R_{comp} = \frac{R_{in} \times V_{osc.\ slope}}{V_{slope} \times k} = \frac{R_{in} \times 1.15}{0.16 \times .75} = R_{in} \times 9.6$$

where k = ratio of slope compensation introduced, to inductor slope, value usually between 0.5 and 1.0.

Current Sense Transformer

The transformer should not saturate. Circuit energy is 1/2 Li²

For the 846T250 core, primary inductance of 1 turn, L_{pri} = $A_L\ N_P{}^2/N^2 = 1650mh \times 1^2/1000^2 = 1.65\mu H$,
$W = 1/2\ L\ i^2 = 1/2 \times 1.65\mu H \times 13.2\mu J$

Maximum core energy storage:

$$W = \frac{B^2 A_e l_e \times 10^{-8}\,(cm)}{2u_e} = \frac{2500^2 \times .259 \times 5.42 \times 10^{-8}}{2 \times 2700} = 16\mu J$$

Coupled Filter Inductor Design

If both inductor coils are wound on a common core, then several benefits are obtained, eg, good dynamic cross-regulation, current limiting to prevent core saturation, and low cost and smaller size. Two design constraints need to be observed. First, use the same turns ratio for the inductor windings as the secondary windings of the transformer. Second, use a winding arrangement that gives approximately 2% or more leakage inductance. (These two points will minimize circulating ripple currents and make matching rectifier V_f's unnecessary.

Coupled inductors are especially useful when current mode control is being used. Separate inductor-capacitor filters for each output each have a tendency to series resonate at their own frequencies, since current mode makes the output look like a high impedance. This adds large gain and phase shifts at these different frequencies, all usually within the loop closing frequency, and thus causing unaccustomed problems. Coupled inductors minimize this effect.

Other factors should be considered when using coupled inductors, such as ripple current, leakage inductance and wiring inductance. Refer to Section M7 for a more complete discussion.

Closing the Loop

The oscillator frequency is 600KHz. Theory suggest that we close the loop at 0db at a frequency no higher than f_{odb} = fsw/2πD = 600KHz/2π0.9 = 106KHz, where D = maximum duty factor.

For current mode operation of a buck type converter the inductor does not appear in the forward signal path. Instead there is a pole consisting of the output filter capacitor and the effective output load resistance. This resistance changes as the load current changes: $R_O = V_O / I_O$.

The output filter capacitor and its ESR constitute a zero in the forward path. For electrolytic capacitors, whose capacitance is usually much larger than necessary in order to get a low enough ESR to meet the ripple voltage spec, the frequency of this zero is fairly low, and in many cases, it is used to get enough phase margin to close the loop. In the design discussed here, polypropylene film capacitors are used; their zero is above a megahertz and thus does not enter into loop closure.

The approach taken here is to reduce the gain of the error amplifier with a slope of −20db/decade through 0db to a negative gain equal to the (positive) gain of the control to output response at 106KHz. The error amplifier is then flattened out at the lowest output pole frequency by adding a zero in the EA compensation network. Refer to Figure 6.

In designing the network around the error amplifier, we wish to use low values of resistance for low noise pickup, but not so low as to load down the output of the EA. For this case 4.7K is used in the feedback path, in series with 0.002uf, and 47K in series with the input. This gives a negative gain of 10x = −20db, and a zero at 17KHz. A 47K resistor is also put in series with the non-inverting input to help negate input current offset.

Control to Output Response

The main output is 5V at 50A max., 5A min.
R_O = 5V/50A = 0.1Ω, R_O = 5V/5A = 1Ω

The output filter capacitor is 15μF.

$f_p = 1/2\pi R_O C = 1/2\pi 0.1 \times 15\mu$ = 110 KHz at 50A, 11KHz at 5A

k = Max I_L/max V_C = 50A/1.0V = 50A/V

$V_O / V_C = KR_O = 50 \times 0.1 = 5$ (14db) at 50A
$= 50 \times 1 = 50$ (34db) at 5A

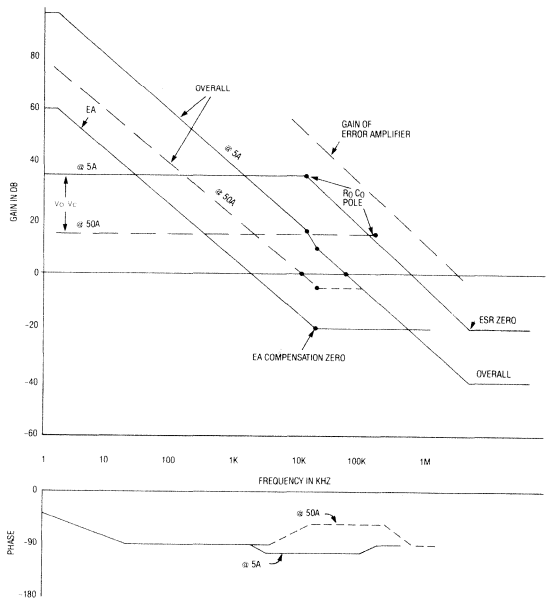


Figure 6.

Bibliography

Current mode control, SEM 400 Topic 1, and Application Note U-97

MOSFET Gate Drive, Addenda, Section D2 or Application Note U-98

Transformers, Addenda, Section M5

Inductors, Addenda, Section M6

Coupled Inductors, Addenda, Section M7

Feedback Loop, Addenda, Section C1

Snubbing, Application Note U-85

Eddy Current Losses, Addenda, Section M-2

150 WATT FLYBACK REGULATOR

R. PATEL, D. REILLY, AND R. ADAIR

This paper describes the design of a low cost 150 Watt flyback switching regulated power supply. Output voltage regulation is achieved through the UC3842, a low cost current mode control IC, and the UC3901 isolated feedback generator. The complete schematic is shown in Figure 1.

The adverse effect of flyback transformer leakage inductance on power transfer to the output is discussed in detail.

SPECIFICATIONS:

Switching frequency, f_S:	100 kHz	
Efficiency, η:	80% minimum	
Output Voltages, V_{out}:	+5 V ±1%,	7.5 - 15 A
	+12 V ±3%,	1.5 - 3.0 A
	+24 V ±10%,	.75 - 1.5 A

TOPOLOGY SELECTION:

Current mode control used in this supply provides inherent good line regulation and optimum dynamic response. The two-transistor discontinuous mode flyback circuit shown in Figure 2 is a low cost approach with multiple output capability. Advantages and disadvantages of this topology are:

Discontinuous Mode Flyback - Advantages:

1. Because there are no filter inductors in series with each output (as in buck regulator circuits), all output voltages will track each other within ±5-10% without post-regulation. This minimizes the headroom required and its associated losses in the +12 V linear post-regulator. Dynamic cross-regulation is also very good with this topology.

2. Only one rectifier is required in each output instead of the two required in buck regulator circuits, reducing overall component and assembly costs.

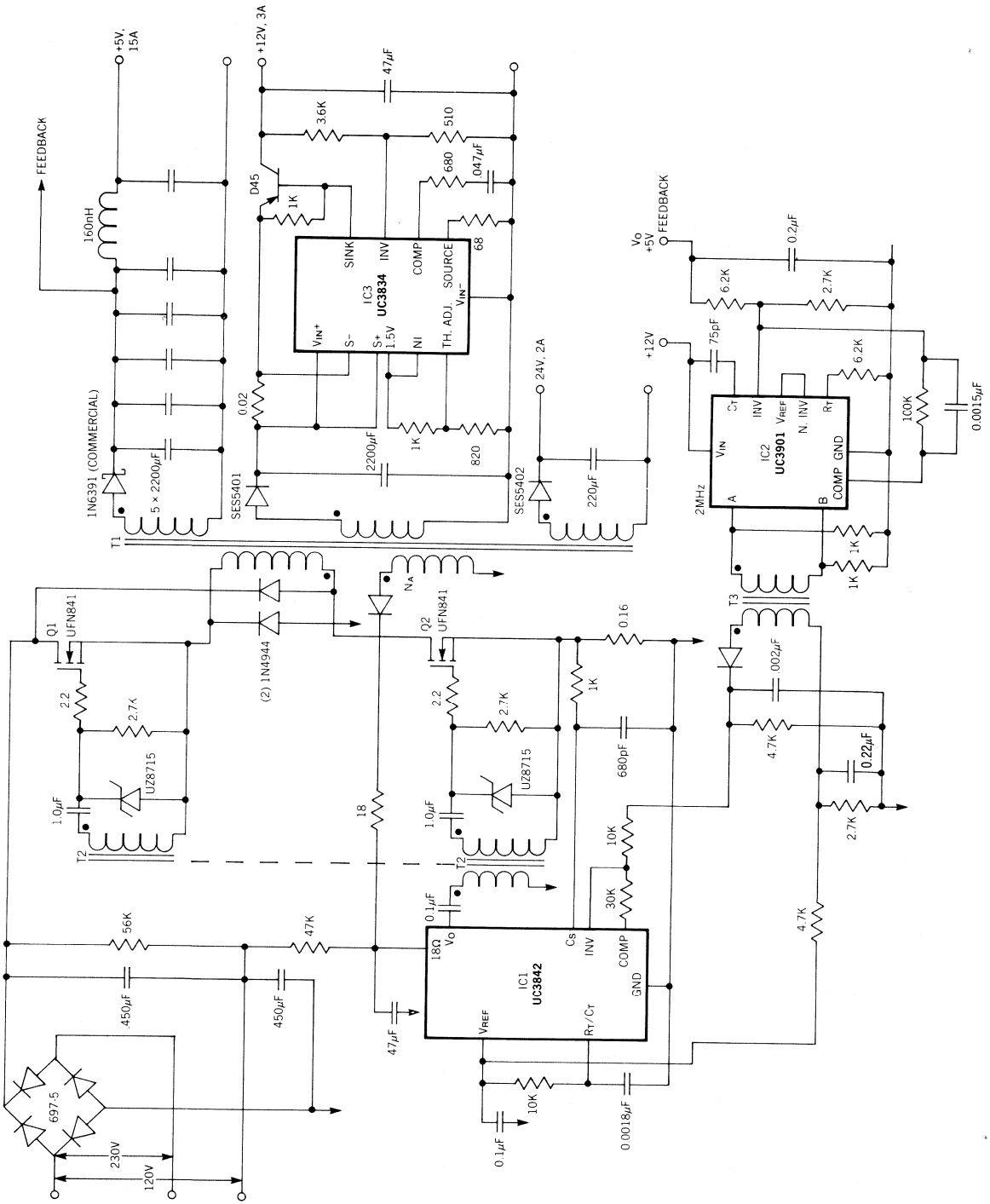
3. Rectifier reverse recovery time is not critical because forward current is zero well before reverse voltage is applied.

4. The flyback transformer used in the discontinuous mode is much smaller because the inductive energy stored is only 1/5 to 1/10 of the energy required in comparable continuous mode circuits.

5. Turn-on circuits are simplified because load current in the power switch is zero during turn-on. There is no concern for turn-on losses or turn-on snubber circuits.

6. Closing the feedback loop is simplified because of the single pole roll-off characteristic of the power circuit.

Figure 1. 150 Watt Flyback Supply -- Complete Schematic



7. Transient response is excellent. The circuit can be designed to correct for large step changes in line or load in little more than one cycle of the switching frequency

8. Conducted EMI is reduced because transistor turn-on occurs with zero collector current. The triangular waveforms of the discontinuous mode contain only the odd harmonics which are attenuated much more rapidly than the even harmonics present in the rectangular waveforms of continuous mode flyback circuits or buck regulators.

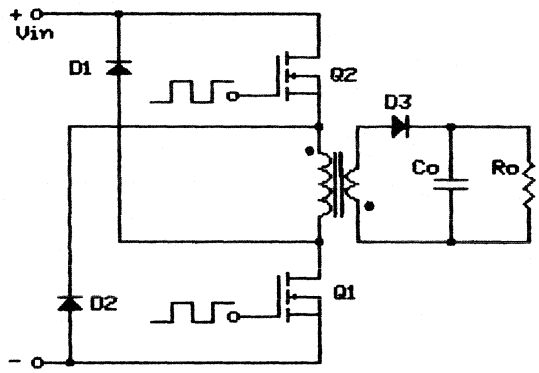


Fig. 2 - Two Transistor Flyback

Discontinuous Mode Flyback - Disadvantages:

1. Switching transistor and rectifier peak currents are nearly two times greater than in the comparable continuous mode circuit. However, the average currents are the same and transistor and diode dissipation is only slightly greater than in the continuous mode.

2. Output filter capacitor ESR and ESL requirements are quite stringent because of the high peak currents encountered in the discontinuous mode. Capacitance values must be nearly twice the comparable continuous mode requirements, and 10-20 times larger than a buck regulator with the same output capability. Nevertheless, transient response is much better because the flyback transformer inductance is so small.

Two-Transistor vs. Single Transistor - Advantages:

1. Voltage rating requirements of MOSFET power switches Q1 and Q2 are half that of a single transistor. This results in much better switching dynamics and much less than half the chip area for the same saturation voltage drop.

2. Cross-coupled diodes D1 and D2 provide a simple non-dissipative way to clamp the voltage backswing caused by T1 leakage inductance. The clamp energy is returned to the bulk input filter capacitor, thus the efficiency is not significantly impaired. Single transistor circuits require an additional transformer winding closely coupled to the primary to obtain non-dissipative clamping, or else the dump the energy (which usually amounts to 15-20% of the output power) into a dissipative snubber circuit.

3. Conducted and radiated EMI is significantly reduced because switching voltages at each end of the transformer move simultaneously in equal and opposite directions. Thus the current spikes that result from charging the stray capacitance to ground (from the wiring, switching transistors and within the transformer) tend to cancel, especially if the capacitance to ground from each end of the transformer is deliberately balanced.

Two-Transistor vs. Single Transistor - Disadvantages:

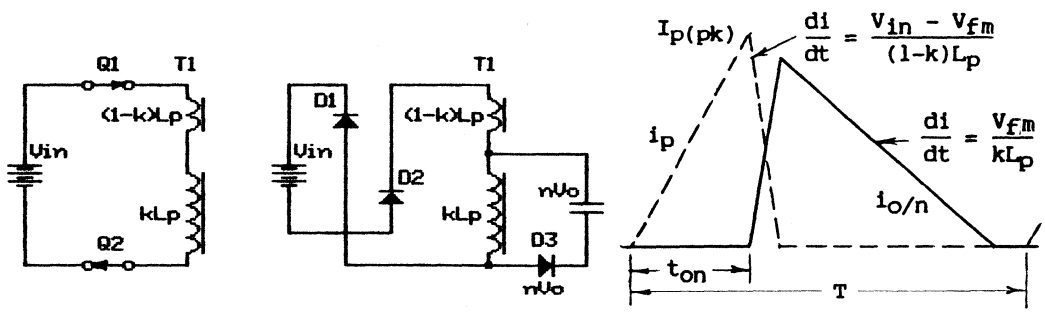
1. Two transistors are required rather than one, but for a 150 watt application, devices are available in the TO-220 package. Because of the lower voltage and smaller size, lower cost can be realized.

2. Requires more complex drive circuit for the upper of the two transistors.

ENERGY TRANSFER IN THE FLYBACK CONVERTER -- LEAKAGE INDUCTANCE EFFECTS

In a flyback converter operated in the discontinuous mode, the energy stored in the flyback transformer (actually an inductor) must be zero at the beginning and end of each switching period. During the "on" time, energy taken from the input is stored in the transformer. When the switching transistors turn off, this stored energy is all delivered somewhere -- mostly to the output. However, the transformer leakage inductance causes much of the stored energy to be dumped into the primary side snubber or clamp, diverting it from the output. The leakage inductance dumps not only its own energy, but also causes much of the energy stored in the mutual inductance to be diverted into the clamp circuit. The amount of energy diverted is typically 15-25% of the total energy stored. In the two-transistor circuit, this diverted energy is returned to the input so the efficiency is not hurt, but peak primary current is greater and the total stored energy in the flyback transformer must be increased.

The amount of energy returned depends upon the transformer turns ratio as well as its leakage inductance. To explain the power transfer process, the simplified equivalent converter circuits during "on" and "off" times are shown in Fig. 3.



3A - "On" time 3B - "Off" time 3C - Current Waveforms

When switches Q1 and Q2 are closed as shown in Figure 3A, energy from the input filter capacitor is transferred to the transformer primary mutual inductance, kL_p, and the leakage inductance, $(1-k)L_p$, where k is the coupling coefficient between primary and secondary. The total energy stored equals $1/2\ LI_p^2$. Energy cannot be transferred to the secondary side at this

time because the output rectifiers are reverse biased.

During the "off" time (see Figure 3B), the current established in the inductor forces the transformer voltage to reverse, or "flyback", until the output rectifier D3 conducts and hopefully transfers the energy stored in the mutual inductance to the output. The current flowing in the leakage inductance causes its voltage to reverse an *additional* amount so that clamp diodes D1 and D2 conduct. This transfers the leakage inductance energy back to the bulk input filter capacitor. Unfortunately, the leakage inductance also causes some of the *mutual* inductance energy to be returned to the input through D1 and D2. This is because whatever current flows in the leakage inductance forces the same current flow on the primary side through the mutual inductance. Thus the leakage inductance delays current transfer to the secondary (see Fig. 3C) and diverts a substantial portion of the mutual inductance energy back to the input. This diversion of energy raises peak primary currents and requires a larger flyback transformer which must store more energy for the same output power. Energy diversion is reduced by making the leakage inductance smaller and by providing a large additional flyback voltage across the leakage inductance so as to reset its current to zero as rapidly as possible.

As shown in Figure 3B and 3C, during the "off" time the output voltage, V_O, and forward rectifier drop, V_f, are reflected across the mutal inductance on the primary side by the transformer turns ratio, $n = N_P/N_S$. The flyback voltage across the mutual inductance is:

(1) $$V_{fm} = n(V_O+V_f).$$

The voltage across the entire primary side inductance L_P is clamped by diodes D1 and D2 to the supply voltage V_{in}. The flyback voltage, $V_{f\ell}$, which resets leakage inductance $(1-k)L_P$ is therefore:

(2) $$V_{f\ell} = V_{in} - V_{fm} = V_{in} - n(V_O+V_f)$$

Referring to Fig. 3C, the time required for the current through the primary side leakage inductance to reach zero is proportional to $V_{f\ell}$. This determines how fast the current can transfer to the secondary side and therefore the amount of mutual inductance energy that will be transferred to the output rather than being diverted into the clamp (see Fig. 3C). Equation 3 shows the total flyback transformer energy, W_L, required to make up for losses and for energy diverted back to the input:

(3) $$\frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{\eta(k-V_{fm}/V_{in})}$$

Higher efficiency, η, and better transformer coupling, k, improve the energy transfer and reduce the stored energy required in the transformer. The leakage inductance in a flyback transformer with high voltage insulation is typically 5% of the primary inductance, corresponding to a k of 0.95. A smaller turns ratio decreases V_{fm} which increases reset voltage $V_{f\ell}$ across the leakage inductance, reducing the energy diverted back to the input.

However, the smaller V_{fm} decreases duty ratio D and increases peak primary current, $I_{p(pk)}$, at a given power output:

$$D = \frac{1}{1+kV_{in}/V_{fm}} \quad ; \quad D_{max} \text{ (at mode boundary) occurs at min } V_{in} \tag{4}$$

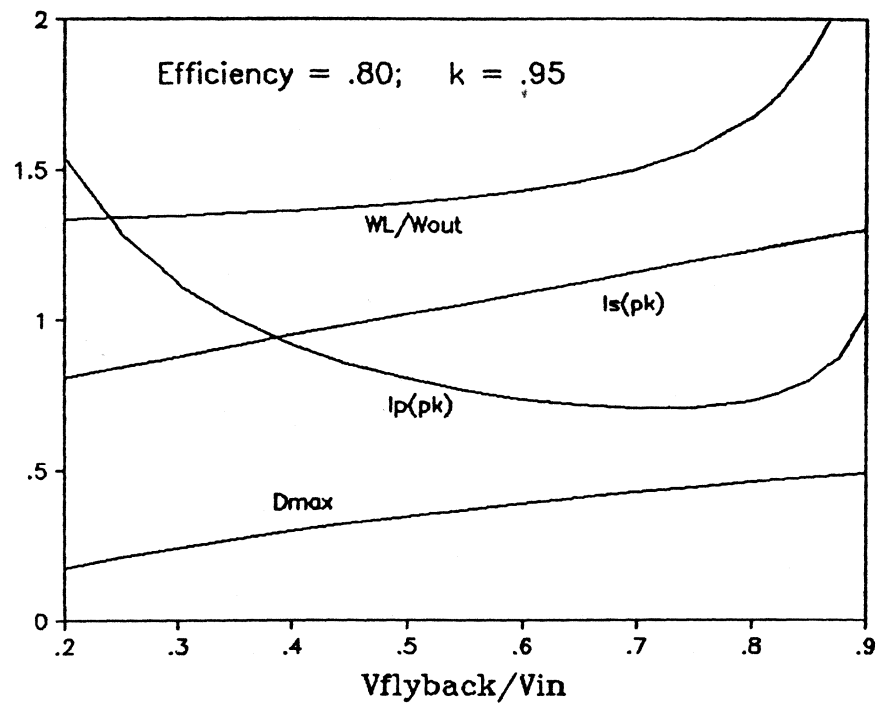
$$I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D} \tag{5}$$

On the other hand, smaller V_{fm} *reduces* peak currents on the secondary side, $I_{s(pk)}$:

$$I_{s(pk)} = \frac{2\ I_{out}}{(1-D)} \tag{6}$$

Figure 4 shows the values calculated from Equations 3 - 6: W_L/W_{out}, D_{max}, $I_{p(pk)}$, and $I_{s(pk)}$, plotted against the ratio V_{fm}/V_{in}. Note that $i_{p(pk)}$ and $I_{s(pk)}$ are calculated at minimum V_{in} and maximum P_{out} values and are plotted on a *relative* basis. These curves suggest that a good design compromise is to use a transformer turns ratio such that $n(V_{out}+V_f) = V_{fm}$ is approximately 1/2 of the worst case minimum V_{in} at low line voltage. The energy transfer process will be more efficient at line voltages above the minimum because V_{fm} remains constant but reset voltage $V_{f\ell}$ across the leakage inductance becomes larger.

Figure 4. Peak Current and Energy Requirements vs. Clamp Ratio.



DESIGNING THE INPUT RECTIFIER AND FILTER

Refer to Design Reference Section I1, "Line Input AC to DC Conversion and Input Filter Capacitor Selection". The input circuit may be connected as a voltage doubler from the 120 V line or as a full-wave bridge from the 230 V line. In either case the input bulk filter capacitors must store enough energy to provide 200 Vdc minimum to the switching converter during the milliseconds that the instantanteous AC line voltage is below 200 V.

Section I1, Table I shows that for a 100 Watt input supply in the worst case doubler configuration, two 160 µF capacitors maintain the required 200 V at mimimum RMS line voltage. The full load input power required for 150 Watt output is 150/η, or 187.5 Watts. This requires 160x187.5/100, or 300 µF for each voltage doubler capacitor. Considering tolerances and temperature coefficients of aluminum electrolytic capacitors, 450µF is used. Peak repetitive charging current from Table I is 3.28x187.5/100 = 6.15 A. RMS charging current is 1.126x187.5/100 = 2.11 A.

DESIGN OF THE POWER INVERTER

Table A below shows the winding turns definition that comes reasonably close to achieving the desired output voltages and the desired 100 V primary side flyback voltage (approximately 1/2 of the 200 V minimum V_{in}):

TABLE A:	Winding	Turns	Vfm	$V_{out}+V_f$	V_f	V_{out}
	Primary	36	100.8			
	5 V, 15A	2		5.6	0.6	5.0
	12 V, 3A	5		14.0	1.0	13.0
	24 V,1.5A	9		25.2	1.0	24.2
	16 V Aux.	6		16.8	.8	16.0

The 16 V Auxiliary output provides power for the control and gate drive circuits. It is not closely coupled to the other secondaries because it is on the primary side of the isolation boundary, so its load regulation is an acceptable 20%. The 12 volt secondary provides 13 V, allowing 1 Volt of headroom for the linear post-regulator which achieves 3% regulation.

During the flyback time all windings will have 2.8 Volts per turn. The turns ratios between secondaries are critical because they determine the output voltage ratios. Each winding must have an integral number of turns, making it impossible to use fewer secondary turns than Table A without hurting the output voltage ratios. The number of primary turns is not as critical because flyback voltage V_{fm} is not rigidly defined. Obviously the number of turns could be any integral number times the values given above.

The total maximum energy storage, W_L, required in the primary inductance of the flyback transformer at full load output and minimum V_{in} is:

$$(3R) \quad \frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{\eta(k-V_{fm}/V_{in})} = \frac{1-100/200}{0.8(.95-100/200)} = 1.3889$$

$$W_L = 1.3889 \times P_{out}/f_s = 1.3889 \times 150/100{,}000 = 2083\ \mu J$$

From Equation 4, the maximum duty ratio and t_{on} at min. V_{in} are calculated:

$$(4R) \qquad D_{max} = \frac{1}{1+kV_{in}/V_{fm}} = \frac{1}{1+.95x200/100} = .3448$$

$$\max t_{on} = DT = D/f_s = .3448/100{,}000 = 3.448\ \mu sec$$

The maximum peak primary current is, from Equation 5:

$$(5R) \qquad I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D} = \frac{2x2083x0.1}{200x0.3448} = 6.04\ A$$

The primary current limit need not exceed 6.04 A because it represents a combination of worst case conditions that are not likely to coexist. For example, with minimum V_{in} slightly larger than 200 V (because the bulk filter capacitors are larger than required), less energy is returned to the source, so that less inductor energy and less $I_{p(pk)}$ is required for full load output.

The total primary inductance required is:

$$(7) \qquad L_p = 2\ W_L/I_{p(pk)}^2 = 2x2083/6.04^2 = 114.2\ \mu H$$

Transformer Design: Design Reference Section M6, "Filter Inductor and Flyback Transformer Design for Switching Power Supplies", defines the approach and the equations used. An EC41 core is chosen based on operating frequency, maximum flux density and hot spot temperature rise limitations.

At 100 kHz operating frequency, the maximum flux density, B_{max}, is limited by core losses, not magnetic saturation. The EC41 core has an effective thermal resistance of 16.5°C/W to the centerpost hot spot. An acceptable hot spot temperature rise of 33°C allows 2 Watts total dissipation -- 1 Watt winding and 1 Watt core losses. Since the EC41 core volume is 11 cm^3, 1 Watt total core loss equals .091 W/cm^3. This occurs with a flux density swing of 0.155 Tesla (1550 Gauss) at 100 kHz, from the core loss data in Design Reference Section M3. Flux remnance is nearly zero at the beginning of each switching period because of the air gap used to store energy in the flyback transformer. Therefore the 0.155 Tesla flux density swing results in B_{max} of 0.155 T for normal conditions at full load. Under the temporary conditions requiring maximum stored energy at V_{in} = 200 V, B_{max} is allowed to reach 0.17 Tesla.

The *minimum* number of primary turns, N_p, needed to store the worst case energy requirement at minimum V_{in} without exceeding 0.17 T flux density is:

$$(8) \qquad N_{p(min)} = \frac{L_p\ I_{max}}{B_{max}\ A_e} = \frac{114x10^{-6}x6.04}{0.17x1.25x10^{-4}} = 32.4\ ; \quad N_p = 36\ turns$$

Referring back to Table I, N_p must be 36 turns or an integer multiple such as 72 or 108. The 32.4 turns defined in Eq. 8 is the *minimum* N_p, so 36 turns is the obvious choice. This will require a slightly larger gap to obtain the desired inductance. The flux swing and core losses will be less than would be obtained with $N_{p(min)}$, but winding losses will be greater.

The actual flux swing can be recalculated from Eq. 8, plugging in 36 turns and solving for B_{max} = 0.153 Tesla. In this case, N_P is not much more than $N_{P(min)}$ and there will be little increase in total transformer dissipation and temperature rise. If N_P had to be much larger than $N_{P(min)}$, winding losses would be much higher and might force the use of a larger core size.

The core center-post is ground to the desired gap length calculated by the classic inductance formula, using the actual N_P of 36 turns:

(9) $\ell_g = \mu_0 N^2 A_e / L_p = 4\pi x10^{-7} x36^2 x1.25x10^{-4} / 114x10^{-6} = .00178\ m = .178\ cm$

The required gap can also be obtained without grinding the center-post by spacing the core halves apart by one-half the total gap. This puts half the gap in the center-post and half in the outer legs of the core (provided the combined area of the outer legs is the same as the center-post area). Using this method, considerable magnetic field is propagated outside the core, and EMI problems may be worsened.

Designing the Windings: AC eddy current losses (skin effect and proximity effect) will be very significant in the 100 kHz flyback transformer unless the windings are designed specifically to minimize these effects. The skin or penetration depth, Δ = .024 cm at 100 kHz, so even a single layer of AWG 24 starts to incur AC losses. Another major concern is to minimize the leakage inductance between primary and secondaries, in spite of the high voltage isolation requirements which force them to be physically separated. Good coupling between secondaries is easier to achieve because they may be co-mingled or even wound multifilar.

First, the 36 turn primary winding is split into two 18 turn portions. The secondaries are in a single closely coupled group. One primary portion is wound around the center post inside of the grouped secondaries, the other primary portion is wound on top of the secondaries. This interleaving results in a dramatic reduction of the magnetic field (energy) between the windings. Leakage inductance between primary and secondary, $L_P(1-k)$, is reduced by a factor of 3, and there is a similar beneficial effect in reducing eddy current losses in both primary and secondaries.

Second, windings are made up of many paralleled wires with diameters less than 2 times the penetration depth, Δ, so that AC current is not excluded from the central portions of the conductors. Thin copper strip may also be used for the same purpose in low voltage, high current windings.

The total cross-section area of all windings is limited by the core window area, A_W = 2.15 cm^2 for the EC41 core. Much of the window area is wasted, taken up by insulation around wires, voids between round wires, insulation between winding portions, and necessary creepage distance at the ends of the windings. Window utilization factor, k_U = 0.4 is the fraction of the window area that is actual conductor. All windings in the flyback transformer are single ended, so that winding losses are minimized by apportioning equal winding cross-section areas to the primary and to the group of secondaries, hence primary area factor, k_P = 0.5. The maximum primary conductor area available is:

(10) $A_P = A_W \cdot k_U \cdot k_P = 2.15x0.4x0.5 = 0.43\ cm^2$

The average length of each turn around the core is ℓ_t = 6 cm (otherwise known as MLT -- mean length per turn). The total length of the entire 36 turn primary is then 6x26 = 216 cm. The RMS primary current, I_p, is:

(11) $$I_p = I_{p(pk)} \cdot (D_{max}/3)^{1/2} = 6.04x(.345/3)^{1/2} = 2.05 \text{ A}$$

Total power dissipation allowed in all windings is 1 Watt, so the primary may dissipate 0.5 watts. The maximum resistance of the primary winding is therefore:

(12) $$R_p = P_p/I_p^2 = 0.5/2.05^2 = 0.119 \text{ Ohms}$$

$$R_p/cm = 0.119/216 = .000551 \text{ Ohms/cm}$$

AWG 21 copper wire comes close to this with .000561 Ohms/cm at 100°C. But a single layer (after interleaving) of AWG 21 at 100 kHz has an AC resistance factor, $F_R = R_{ac}/R_{dc}$ of 2.45, which more than doubles the loss.

An acceptable F_R value of 1.4 is obtained by using 7 AWG 29 wires paralleled in place of a single AWG 21 wire. The 7 wires are twisted together into a 7-strand cable, or Litz wire, with 6 outer strands packed in a hexagonal pattern about the 7th central strand. The DC resistance of the paralleled strands is .000512 Ohms/cm, less than a single AWG 21 conductor. The 36 turn primary is wound with 18 turns of the seven strand cable inside the secondaries and 18 turns top of (outside) the secondaries. The breadth of the winding window in the EC41 core is 2.78 cm. The 18 turns of 7-strand cable will occupy the central 1.75 cm of the window, leaving plenty of creepage distance.

Peak and rms secondary currents are proportional to the DC output currents as follows. The results of these calculations are given in Table B below:

(6R) $$I_{s(pk)} = 2 \cdot I_{out}/(1-D_{max}) = 3.05 \cdot I_{out}$$

(13) $$I_s = I_{s(pk)} \cdot ((1-D_{max})/3)^{1/2} = .467 \cdot I_{s(pk)}$$

The conductor area for each winding is proportioned to operate at the same rms current density as the primary. The results are shown in Table B.

TABLE B WINDING DATA

Winding	$I_{s(pk)}$	Irms	Area(cm^2)	Configuration
Primary		2.05	.0041	18+18 turns, 7xAWG29
5V, 15A	45.75	21.36	.0429	2 turns, .025x1.75 cm strip
12V, 3A	9.15	4.27	.0086	5 turns, 2 - 7xAWG29 paralleled
24V,1.5A	4.58	2.14	.0043	9 turns, 7xAWG29
16V Aux	.21	.05	.0001	6 turns, AWG 29

Three layers of 1 mil mylar tape (.016 cm - 6.6 mil incl. adhesive) are used to meet VDE 3750 V isolation requirements, applied between the two primary halves and the secondary bundle.

Copper strip is used for the two turn 5 Volt secondary. The thickness of the strip is comparable to the skin depth, Δ, so that F_R is only slightly

greater than 1.0.

Note that the same 7-strand AWG29 cable is used for the primary and the 12 and 24 Volt secondaries. The 12 and 24 Volt windings are mingled in a single layer as follows: Four lengths of cable -- A, B, C, and D are wound simultaneously side by side for 5 turns. This results in a single smooth layer 20 cable diameters wide across the winding breadth, in the sequence A,B,C,D,A,B,C,D,A....etc. A and C are paralleled for the 5 turn 12 Volt output. One turn is taken off D, leaving a total of 19 cable diameters across the winding. The 5 turns of B are put in series with the 4 turns left in D for the 9 turn 24 Volt output.

The 16 Volt auxiliary windings are put on last, spread over the outer half primary. The auxiliary winding must be separated from the other secondaries because of the line isolation requirements.

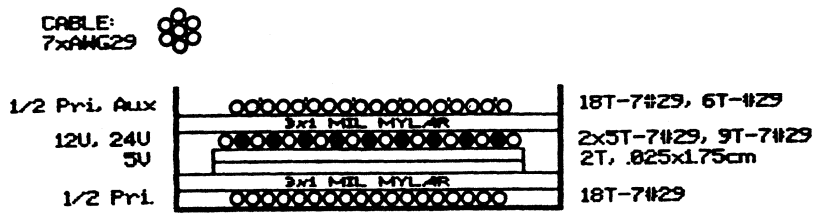


Figure 5. Transformer Winding Layout

Output Filter Capacitors: Aluminum electolytic capacitors have the lowest cost and are therefore most widely used in commercial/industrial supplies. Filter capacitor selection is dominated entirely by the ESR (Equivalent Series Resistance) necessary to obtain acceptable peak-peak ripple voltage.

$$ESR_{max} = V_{ripple}/I_{s(pk)}$$

Table C shows the parameters and results of the capacitor selection process:

TABLE C -- OUTPUT FILTER CAPACITORS

Output	Vripple	Is(pk)	ESRmax	Capacitor Selection
5V, 15A	0.3	45.75	.0066	(5) 2200 µF, 16 V, Panasonic HF
12V, 3A	0.3	9.15	.033	(1) 2200 µF, 16 V, "
24V,1.5A	0.5	4.58	.11	(1) 220 µF, 50 V, "
16V Aux	0.3	.21	1.42	(1) 47 µF, 25 V, "

The 5 Volt output ripple voltage is further reduced to below 0.1 V by the additional L-C filter section (actually L-R because of ESR). The 160 nH inductor is 0.1 Ω at 100 kHz, and the additional 2200 µF capacitor has an ESR of .03 Ω, for a ripple reduction factor of 3.3.

CONTROL AND GATE DRIVE CIRCUITS:

The auxiliary supply provides an average current of 50 mA to power the UC3842 control IC and power MOSFET gate drive circuits. The auxiliary supply is maintained from the 7 turn auxiliary winding on T1 through an 18 Ω resistor which limits the peak charging current and prevents the supply from charging to the high peak voltage of the leakage inductance spike.

During initial startup of the supply, the UC3842 undervoltage lockout disables the control and drive circuits so that the total current drawn is less than 1 mA. This enables the 47K resistor from the input bulk filter to initially charge the auxiliary supply capacitor to 16 volts, where the circuit comes alive and starts the converter. It takes 200 - 300 switching periods for the output voltages and the T1 auxiliary winding voltage to rise to normal levels and recharge the aux supply capacitor, so the capacitor must be large enough to supply 50 mA for 300x10μs without dropping below 11 Volts (where the UC3842 turns off).

The totem pole output of the UC3842 drives the gates of the two MOSFETs through transformer T2, consisting of three 20 turn windings of AWG 30 wire on a 1/2 inch O.D. ferrite toriodal core, 204XT250, 3E2A material. The three wires are wound together (trifilar). High voltage insulation between primary and secondaries is not needed, as all windings are on the same side of the isolation boundary.

Primary current in T1 is sensed by a 0.16 Ω resistor. This current sense voltage is applied through a spike filter to the current sense terminal of the UC1840, where it is compared against the amplified output error voltage. The comparator input voltage is clamped to 1 V, which effectively limits the peak primary current to 1/0.16 = 6.25 A and indirectly limits the duty ratio. The error amplifier output (pin 1 - Compensation) must swing from 1 to 4.5 Volts in order to swing the comparator input from 0 to 1 Volt for full range control of the current. This is because there are two forward diode offsets and a 3 to 1 divider between the error amplifier output and the comparator input within the IC.

The 30K feedback resistor and 10K input resistor together establish an error amplifier gain of 3. Combining this with the 3/1 divider at output of the error amplifier results in an overall gain of 1 from the input of the 10K resistor to the current control comparator. The inverting input of the error amplifier normally sits at 2.5 V. This makes it necessary to provide +1.8 V bias to the input demodulator so that the input will swing from 1.8 to 3.0 V in order to swing the output full range from 4.5 to 1 V.

A UC3901 isolated feedback generator compares the 5 volt output against an internal reference, amplifies the resulting error and uses it to amplitude modulate a 2 mHz carrier. This signal is easily coupled through a tiny isolation transformer T3 back to the primary side where it is demodulated and the error voltage recovered and applied to the UC3842 error amplifier input. Transformer T3 has two 15 turn, AWG 30 windings on the same 1/2" O.D. epoxy coated ferrite toriodal core (204XT250, 3E2A material) used for T2. These windings must be wound individually on opposite sides of the core to provide 3750 Volt isolation. Although the coupling is hurt because the windings are not distributed uniformly around the entire core, leakage inductance in this application is not critical.

CLOSING THE FEEDBACK LOOP:

The 5 Volt output has the most critical regulation requirement. and is used as the basis for closed loop control. The 12 Volt output uses a simple linear post-regulation technique to achieve better than 3% regulation. The 24 Volt output achieves better than 10% line and load regulation by simply tracking the 5 Volt output without additional post-regulation.

The feedback loop design approach is taken from Design Reference Section C1 - "Closing the Feedback Loop". The Bode plot of Figure 6 shows the overall loop gain and phase, along with its two major components -- the control to output gain and the feedback circuit gain.

The overall loop gain Bode plot shows the 0 dB crossover frequency to be 8.4 kHz. The solid lines show the gain and phase with maximum filter capacitor ESR. Minimum ESR, shown in the dash lines, is assumed to be 1/5 of the maximum. The worst case phase shift of 135 degrees which occurs with minimum ESR provides an adaquate phase margin of 45 degrees. The gain of 333 (50 dB) below 60 Hz is sufficient that a .015 Volt error on the 5 Volt output swings the output over its full range, which is much better than the 1% regulation required.

The control to output portion of the loop gain includes the current control comparater and pulse width modulator in the UC3842, the power switching circuit, flyback transformer and filter. The formulae from which the plots were calculated are from Design Reference Section C1, Appendix C, pages 5 and 6. These equations give no consideration to the power transformer turns ratio, so the control to output gain must be multiplied by n = 36/2. (These equations apply to current mode control, and the current is stepped up.)

Before beginning the calculations, the primary inductance, filter capacitance and load resistance values are all referred into the 5 Volt output according to their respective turns ratios squared:

$$C' = 2200x6 + 2200x(5/2)^2 + 220x(9/2)^2 = 31400\ \mu F$$

$$ESR' = .03x2200/31400 = .002\ \Omega\ max,\ .002/5 = .0004\ \Omega\ min$$

$$R_O' = V_O^2/P_O = 5^2/150 = .1667\ \Omega\ min;\ = 5^2/75 = .333\ \Omega\ max$$

$$L' = L_p/n^2 = 114.2/(36/2)^2 = 0.352\ \mu H$$

$$k = I_{p(pk)}/maxV_C = 6/1 = 6 \quad (6A\ controlled\ by\ 1V\ comparator\ swing)$$

Below 60 Hz, the control to output gain at full load is 14 dB:

$$(14)\quad v_O/v_C = nK(R_O'L'f/2)^{1/2} = 18x6x(.1667x.352x0.1/2)^{1/2} = 5.85$$

Considering losses, actual gain will be slightly less -- assume gain of 5, or 14 dB. The gain rolls off above 60 Hz with a single pole characteristic (-20 dB/decade with -90° phase shift). This pole frequency is determined by output filter capacitance and load resistance:

$$(15)\quad f_p = 2/(2\pi RoC) = 2/(2\pi x.1667x.0314) = 60.8\ Hz$$

At 2400 Hz, a zero is encountered attributable to the maximum ESR of the filter capacitor. This zero cancels the pole, flattening out the gain and bringing the phase lag gradually back to zero.

(16) $f_Z = 1/(2\pi x ESR x C) = 1/(2\pi x.002x.0314) = 2413$ Hz (ESR max)
$= 1/(2\pi x.0004x.0314) = 12670$ Hz (ESR min)

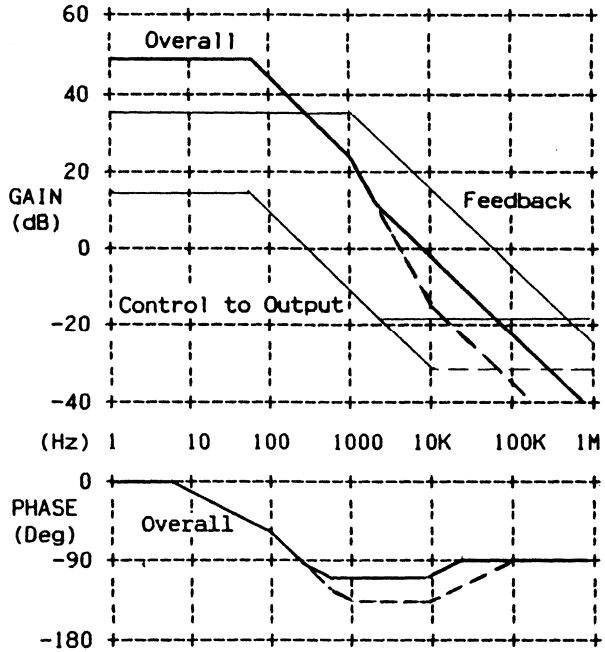


Figure 6. Loop Gain Bode Plot

Stability considerations dictate that the overall loop gain must cross 0 dB below 1/4 or 1/5 of the switching frequency. In designing the gain of the feedback circuits, it is necessary to add a pole to compensate (cancel) the ESR zero, otherwise the ESR zero would cause the overall loop gain to flatten out and not cross 0 dB as required. If the compensating pole is put exactly at the ESR zero frequency, the overall loop gain will have a single pole -20 dB/decade slope with -90' phase shift from 60 Hz to well above 100 kHz. The phase margin would be 90', which is much more than necessary. The overall low frequency loop gain can be increased by putting the compensating pole *below* the ESR zero frequency. This results in a 2 pole slope between the compensating pole and the ESR zero, increasing phase shift and reducing phase margin. A pole frequency of 1 kHz is used in this design, which reduces the phase margin to 45' with the worst case ***minimum*** ESR.

The control to output gain at 20 kHz is -18 dB. To set the crossover frequency at 20 kHz ($f_S/5$) requires +18 dB feedback circuit gain. However, this causes another problem: With feedback circuit gain of +18 db at 20 kHz, decreasing 20 dB/decade as it must to compensate the ESR zero, the feedback gain is 4 dB at the 100 kHz switching frequency. There is nearly 0.3 V of switching frequency ripple at the 5 Volt output where it is sampled

for feedback control. The 0.3 Volts ripple will be amplified 4 dB to 0.48 Volts by the feedback circuit and applied to the current sense comparator in the UC3842 along with the amplified output error voltage. The sawtooth waveform representing primary current at the other input of the comparator is a *maximum* 1 Volt amplitude at full load, and 0.5 Volts at 1/4 load. The 0.48 Volts of 100 kHz ripple will cause erratic behavior of the modulator at moderate load levels. Solving this problem requires lower feedback circuit gain at 100 kHz, which lowers the gain at all frequencies and reduces the crossover frequency. In this application, 0.2 Volts ripple amplitude at the current sense comparator input is acceptable, which dictates a feedback circuit gain of 2/3, or .667 (-3.5 dB) at 100 kHz. Thus the gain is 7.5 dB (2.37) less than originally attempted, and the crossover frequency is 2.37 less, or 8.4 kHz. With a gain of .667 at 100 kHz, the feedback circuit gain at the pole frequency, 1 kHz, is .667x100K/1K = 66.7 (36 dB).

As stated earlier, the gain from the demodulator at the input of the UC3842 to the input of the current sense comparator is 1 (0 dB), to well above 100 kHz. The AC gain through the coupling transformer and demodulator is also 1. The gain of the driver section of the UC3901 isolated feedback generator is fixed at 4. The 100K feedback resistor around the UC3901 error amplifier together with the 6.2K input resistor to provides a gain of 16.5, for a total gain of 16.5x4 = 66, as required. the .0015 µF across the 100K resistor establishes the 1 kHz pole frequency.

CLOSING THE FEEDBACK LOOP

by

Lloyd H. Dixon, Jr.

Switching power supplies almost always use closed-loop negative feedback systems in order to achieve design objectives for line and load regulation and dynamic response. As shown in Figure 1, the closed loop can be described in terms of these major elements:

	Reference and comparator
G1(s):	Error amplifier and compensation networks
G2(s):	Pulse width modulator and power switching circuit
$H_e(s)$:	Output power filter

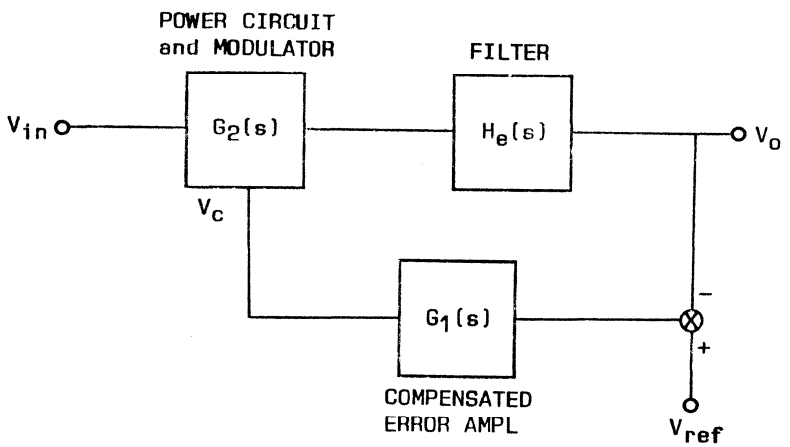


Figure 1. Control loop block diagram

Fortunately, these closed-loop control systems can be stabilized using simple analytical techniques. Unity gain crossover occurs only once in the gain vs. frequency characteristic, permitting the use of a simplified version of the Nyquist stability criterion. Bode plots provide a simple and powerful method of displaying and calculating the loop gain parameters (see Appendix B).

The switching frequency, f_c, the gain-frequency characteristics of the pulse width modulator and power switching circuit, G2(s), and the filter, $H_e(s)$, are predetermined by the application and the choice of circuit topology. The task in closing the feedback loop is to define the characteristic of the error amplifier and related compensation networks, G1(s), that will result in the optimum closed loop gain-bandwidth for good dynamic response, line and load regulation and stability.

CLOSED LOOP DESIGN PROCEDURE

(1) Define the Goal: Make a Bode plot of the desired closed-loop characteristic that will achieve the best possible gain-bandwidth for good dynamic response, line and load regulation and stability.

(2) Define the Control to Output Gain: Decide upon the control method. Make a Bode plot of G2(s), the gain characteristic of the pulse width modulator and power switch, and $H_e(s)$, the filter.

(3) Design the Compensation Network: Subtract the gain(dB) and phase plotted in (2) above from (1). The result is the G1(s) characteristic necessary to attain the closed loop objective.

DEFINE THE GOAL

Stability Criterion: Referring to Figure 2, if the gain magnitude crosses unity (0 dB) only once, the system is stable if the phase lag at the crossover frequency, f_c, is less than 180 degrees (in addition to the normal 180 degree phase shift of the negative feedback system). At other frequencies, the phase lag may exceed 180 degrees and the system will still be stable.

The 'phase margin' is the amount by which the phase lag at the crossover frequency, f_c, is less than 180 degrees. The 'gain margin' is the factor by which the gain is less than unity (0 dB) at the frequency where the phase lag is 180 degrees. If the phase lag at f_c is only slightly less than 180 degrees (small phase margin), the system will be stable, but will exhibit condsiderable overshoot and ringing. A phase margin of 45 degrees provides for good response with very little overshoot.

Nyquist's stability criterion permits the phase lag to exceed 180 degrees at frequencies below f_c where the gain is greater than 0 dB, but this is not a good practice. The system will be conditionally stable, but if the loop gain decreases it becomes unstable. That is exactly what happens when the system runs into large signal bounds, as with large step changes in load. The system will then oscillate or have severe underdamped ringing.

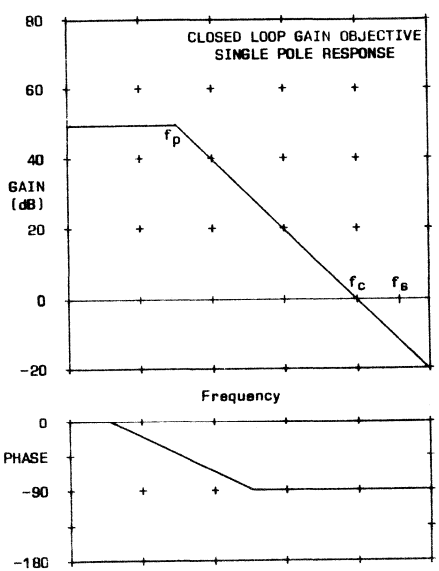


Figure 2.

Short Cut Stabilization Method: It is easy to achieve good loop stability by using a dominant low frequency pole to roll the loop gain off at a very low frequency. Unity gain cross over must occur substantially below the output filter pole frequency to avoid

the additonal phase lag it introduces. The result of this short cut stabilization method is poor dynamic response.

Closed Loop Objective: The goal in designing the stabilization network is to optimize line and load regulation and dynamic response by providing high loop gain out to high frequencies. Phase lag must not approach within 45 degrees of 180 at f_C and all lower frequencies to avoid oscillations, ringing and instability. Stability analysis must be made at circuit operating extremes.

A practical goal for the closed loop characteristic is that of a net single pole as shown in Figure 2. The resulting high gain at low frequency provides good DC regulation. Gain falls off linearly at -20 dB/decade with 90 degree phase lag until well above f_C. High f_C provides good small signal dynamic response.

Maximum Crossover Frequency: (1) Sampling theory shows it is not possible to transmit information at any frequency greater than 1/2 the sampling frequency (which is the switching frequency, $f_S/2$). (2) The system becomes unstable when f_C exceeds $f_S/(2\pi D)$ with duty cycle, D, greater than 0.5.[1] At $f_C = f_S/(2\pi D)$, system response is maximally fast. (3) At $f_C = f_S/(2\pi D)$ the error amplifier gain may be high enough to cause the amplified output ripple voltage to drive the error amplifier into saturation, necessitating a further reduction in f_C.

In the examples given in Appendix C, a crossover frequency $f_C = f_S/4$ is attempted, but not always attained because of right-half-plane zeros or insufficient error amplifier gain-bandwidth.

DEFINE THE CONTROL TO OUTPUT GAIN

The control to output gain, or transfer characteristic, is the combined gain and phase vs. frequency characteristics of the PWM and switching circuit, G2(s), plus the output filter, He(s). The PWM, switching circuit and filter are fundamental to the design of the switching power supply. These elements are usually designed well before the process of closing the loop is started.

Because the control to output gain is part of the total loop, it is necessary to make a Bode plot of the control to output gain in order to know how to design the remainder of the loop -- the error amplifier and compensation network. This task is facilitated by the equations given in Appendix C for each PWM-switching topology combination. These equations translate the previously defined physical parameters of the PWM and switching circuit into gain and phase vs. frequency for the Bode plots.

Control method: The mode of operation of the pulse width modulator has a great effect upon the performance of the closed loop system and the design of the compensation networks. This discussion considers only PWM methods that run at fixed frequency, which all function on the basis of a comparator

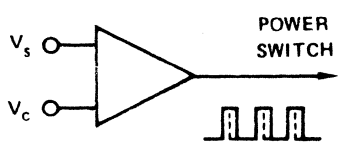


Figure 3.

as shown in Figure 3. A control voltage, V_C, is compared to a fixed frequency linear sawtooth ramp voltage, V_S. The comparator output provides rectangular fixed frequency pulses which drive the power switching transistors. The duty cycle of the power switch conduction is thereby controlled according to the relationship between V_C and V_S.

Direct Duty Cycle Control: The oldest, most commonly used method, implemented in most control IC's. The sawtooth ramp is constant amplitude, (see Figure 4), and the circuit operates exactly as above. Disadvantages are: (1) Provides no voltage feedforward to anticipate the affects of input voltage changes. Slow response to sudden input changes. Poor audio susceptibility. Poor open loop line regulation, requiring higher loop gain to achieve specifications. (2) In continuous mode regulators, provides no help in dealing with the resonant two pole filter characteristic with its sudden 180 degree phase shift. Control changes must propagate through these two filter poles to make a desired output correction, resulting in poor dynamic response.

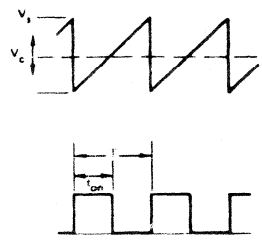


Figure 4.

Voltage Feedforward Control: Functions exactly like direct duty cycle control above with one key exception -- the sawtooth ramp is not constant amplitude, but varies in direct proportion to the input voltage (see Figure 5). The effect of this simple modification is dramatic. Because V_S varies directly with input voltage, if V_C is constant the duty cycle varies inversely with input voltage. Thus the volt-second product, $V_{in}D$, remains constant without any control change. Open loop line regulation is very good, and the problems of direct duty cycle control in (1) above are corrected. Much less closed loop gain is required, mostly to achieve good dynamic response. The UC1840 is a third generation control IC with voltage feedforward capability.

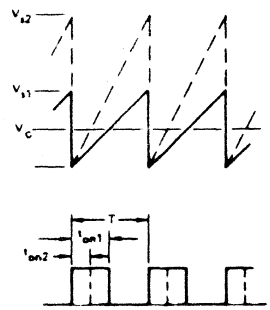


Figure 5.

Current Mode Control: This newest control method, embodied in the UC1846 IC, also controls the duty cycle by comparing the control voltage to a fixed frequency sawtooth ramp. In this case, the ramp voltage is not derived artificially from a ramp generator, but is provided directly from the power switching circuit inductor current waveform through a current sampling resistor (Figure 6). Thus the inductor current ramp is fed back to the control comparator, forming a second, inner control loop. The control voltage out of the error amplifier is derived from the output voltage compared to a voltage reference, as before, but now the control voltage programs the inductor current via the inner loop and no longer controls the duty cycle directly.

The results of this method are profound. All of the problems of the direct duty cycle control method (1) and (2) above are corrected with current mode control. In addition to having the voltage feedforward characteristic with instantaneous open loop response to input changes, current mode control eliminates the inductor filter pole, because this pole is inside the inner loop. This reduces two pole second order filter which is not easy to compensate to a single pole (the filter capacitor) first order filter, which permits simpler compensation networks.

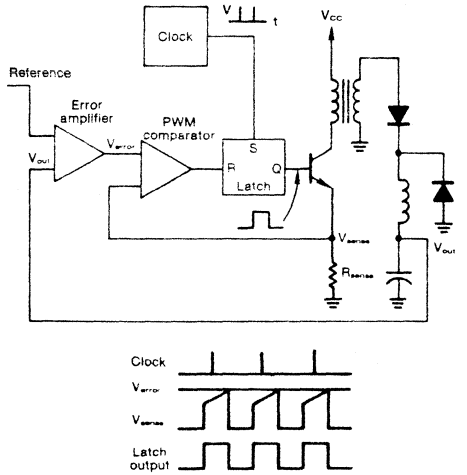


Figure 6.

Current mode control circuits used with continuous mode power switching circuits benefit from slope compensation, and it is required for stability at duty cycles greater than 50%. Ref. Appendix A. Power transformer magnetizing current superimposed upon the reflected load current acts to provide some slope compensation, but the amount is rather variable and indeterminate.

DESIGN THE COMPENSATION NETWORK

The control to output gain characteristic subtracted from the overall closed loop objective roughly defines the characteristic sought in the error amplifier with its compensation network. In general, the procedure involves:

(1) Put zeros in the compensation network near the frequencies where excess poles occur in the control to output gain so that phase shift has an adequate margin (45 degrees) up to the crossover frequency.

(2) Put poles in the compensation network near the frequencies where ESR zeros and right-half-plane zeros occur in the control to output gain. Otherwise these zeros will flatten the gain characteristic and prevent it from falling off as desired.

(3) If low frequency gain is too low to obtain desired DC regulation because of zeros added in step (1), add a pole-zero pair at low frequency to boost gain.

(4) In complex situations, a certain amount of juggling with trial solutions is inevitable.

Compensation Circuits: Two circuits that will handle most compensation requirements are given in Appendix A. These circuits are applied to the example problems in Appendix C. Try to use the power switching topology/control method combination that allows the use of the essentially flat characteristic of circuit A-1 which has no input capacitor, to avoid the poor large signal behavior that invariably results with circuits like A-2 because of abnormal voltage levels that appear on the input capacitor, C_i.

Determine Closed Loop Regulation: It is possible to calculate the DC regulation of the system using classical closed loop analysis, but this is often awkward and of questionable value, because the gain of the system often changes as a function of input and load variables.

It is simpler and more direct to calculate the DC regulation as the large signal problem that it really is: (1) Use the DC equation of the topology/control method combination (Eq. 1a in the examples) to calculate the DC control voltage, V_C, required to maintain the output voltage at the desired level under extremes of line and load conditons. The extreme V_C swing must of course be less than the sawtooth ramp amplitude or the system will not even have control over the desired range of conditions. (2) Divide the extreme V_C swing by the low frequency gain of the E/A compensation circuit. (3) The result is the output error voltage required to provide the desired V_C control swing, which can be expressed as a percentage of the nominal output voltage.

Insufficient Gain-bandwidth: If the amplifier gain-bandwidth is not enough for the desired compensation scheme, there are some alternatives other than: (1) use an IC with a better amplifier, or (2) back down on the crossover frequency.

One alternative is to use a control method that requires less loop gain because line regulation problems are eliminated with input feedforward, and the two pole filter characteristic is gone with current mode control.

Also, when the ramp slope at the comparator input can be set independently, such as in the UC1840 or UC1846, greater control to output gain-bandwidth is achieved by reducing the ramp slope and correspondingly reducing the duty cycle clamp voltage. The full output range is now controlled with a smaller control voltage range, and error amplifier gain-bandwidth requirement is reduced.

Control to output gain-bandwidth is also increased by sensing the highest available output voltage. This reduces the gain-bandwidth requirement of the error amplifier.

EXAMPLES OF CLOSING THE LOOP

Examples are worked out in Appendix C for most basic topologies operated in discontinuous as well as continuous inductor current modes, and using three control methods: direct duty cycle control, voltage feedforward and current mode control.

In the examples given, an input voltage range of 2:1 and load current range of 10:1 is assumed for consistency and to permit direct comparison. All elements of the power circuit are assumed to be transformed to the level of a 12 volt output, and actual primary side voltages, currents and transformer turns ratio, if used, are not visible. The 12 volt output is used as the basis for feedback voltage sensing.

MISCELLANEOUS POINTS

EMI Filter Resonance: When an input EMI filter is used, make sure its resonance is well damped and its resonant frequency is not near the resonant frequency of the output filter, or severe interaction will result.

Modulator Phase Lag: The vast majority of PWM control chips use a simple comparator method of determining pulse width, wherein the output pulse is terminated according to the instantaneous value of the feedback control voltage at the moment of pulse termination. This "naturally sampled" method of pulse width modulation ideally results in zero phase lag in the modulator and in the converter power switching stage.[2] In practice, however, comparator delays and storage time delays in the power switch will cause a phase lag directly proportional to the delay time, t_d, and signal frequency, f, according to the relationship:

$$\Phi_m = 360\ t_d/T = 360\ t_d\ f$$

This additional phase lag reduces the phase margin at the unity gain crossover frequency and may therefore contribute to control loop instability. For example, at a crossover frequency of 25 kHz, consistent with a switching frequency greater than 50kHz, a storage time of 1 microsecond in the power switch will cause an additional phase lag of 9 degrees, reducing phase margin by that amount.

REFERENCES

(1) J. R. Wood, "Taking Account of Output Resistance and Crossover Frequency in Closed Loop Design," POWERCON 10, pp. D4.1-D4.16, March 1983.

(2) R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," POWERCON 8, pp. H4.1-H4.6, April 1981.

APPENDIX A -- ERROR AMPLIFIER AND COMPENSATION NETWORK DESIGN

The error amplifier with its associated compensation network completes the closed loop system by comparing the output voltage to a voltage reference at the input of the error amplifier and feeding the inverse of the amplified error signal back to the control input. The compensation networks provide phase leads and lags at appropriate frequencies to cancel excess phase lags and leads of the power circuit. The goal is to obtain an overall loop gain characteristic approaching that of a single pole, rolling off -20 dB/decade with 90° phase lag with the gain crossing 0 dB at high frequency (appx. $f_S/4$).

Single Pole Topologies. The circuit of Figure A-1 provides essentially a flat gain characteristic with zero phase shift (not including normal 180° negative feedback). One or two poles are introduced at high frequency to compensate for power circuit zeros. Figure A-1 is intended for use with all power circuits which have single pole filter characteristic. This includes all topologies in the discontinuous inductor current mode (regardless of control method) and all continuous mode topologies when used with current mode control.

Pole #1, R_f and C_f, compensates for the zero of the output filter capacitor ESR in the power circuit.

Resistor R_{ref} should be equal to the net DC resistance seen by the E/A inverting input (R_d in parallel with R_i) in order to cancel input voltage offset caused by amplifier input bias current.

Resistor R_d forms a voltage divider with R_i and R_p when the regulated output voltage, V_o, is larger then V_{ref}. R_d simply provides a DC offset. It has absolutely no effect on loop gain. This is because under normal operation, the voltage on the inverting input is a DC voltage always within a millivolt or two

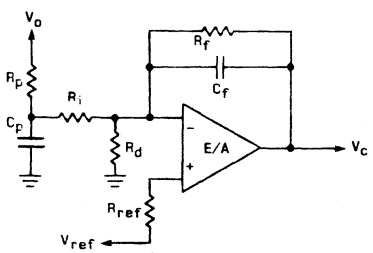
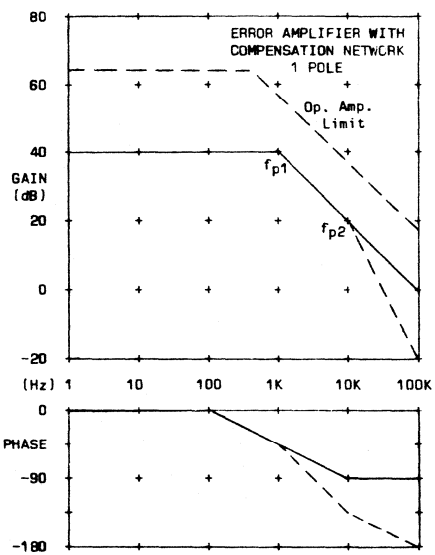


Figure A-1



$$\text{Gain (below } f_{p1}) = R_f/R_i$$

$$\omega_{p1} = \frac{1}{R_f C_f}, \qquad \omega_{p2} = \frac{1}{R_p C_p} \qquad R_p << R_i$$

$$R_d = \frac{V_{ref}(R_i + R_p)}{V_o - V_{ref}}$$

of V_{ref} applied to the non-inverting input. DC current flows through R_d, but no AC current. R_d sets the DC input voltage level, but does not effect the gain.

Two Pole Topologies. The circuit of Figure A-2 is intended for power circuits which have a two-pole filter characteristic — all continuous inductor current mode topologies when not using current mode control. Pole #2 is used in all cases to compensate the filter capacitor ESR zero.

Zero #2 is required to cancel one of the two filter poles. Unfortunately, this usually reduces the low frequency gain below the gain required to meet DC regulation requirements. Pole #1 is added to boost the low frequency gain. Zero #1 is then required to cancel Pole #1 when the filter pole frequency is reached. Zeros #1 and #2 are often placed at one-half the filter pole frequency to provide anticipatory phase shift. This is because the two pole second order resonant filter can have an extremely rapid phase shift at the pole frequency. This whole mess is avoided by using current mode control and/or discontinuous inductor current operation.

Pole #1 frequency is determined by C_f and R_f. However, in most cases R_f is omitted (open), which would predict the gain rising to infinity at $f_{p1} = 0$. In reality, the gain cannot exceed the error amplifier capability, and f_{p1} occurs where the gain curve intersects this limit at a frequency below 1 Hz.

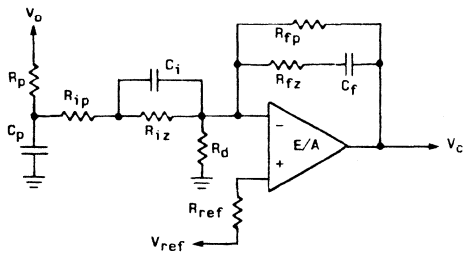
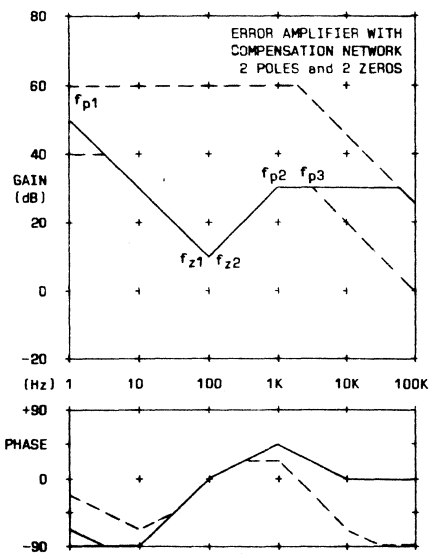


Figure A-2



Gain (at f_{z1}, f_{z2}) = $R_f/(R_{ip}+R_{iz})$

$$\omega_{z1} = \frac{1}{R_{fz}C_f}, \qquad \omega_{p3} = \frac{1}{R_pC_p} \qquad R_p << R_i$$

$$R_d = \frac{V_{ref}(R_{iz} + R_{iz} + R_p)}{V_o - V_{ref}}, \qquad \omega_{z2} = \frac{1}{R_{iz}C_i}$$

$$\omega_{p1} = \frac{1}{(R_{fp} + R_{fz})C_f}, \qquad \omega_{p2} = \frac{R_{ip} + R_{iz}}{R_{ip}R_{iz}C_i}$$

Although well-designed compensation networks similar to Figure A-2 will provide excellent regulation and small-signal dynamic performance, the input capacitor, C_i, severely impairs large signal transient performance. This is because in all the continuous inductor current mode circuits, the inductor current cannot keep up with large step changes in load current. The rate of change of inductor current depends on the excess volt-seconds available when the duty cycle is at its max. limit. It may take up to 10 or 20 switching periods for the inductor current to follow a step change from half to full load, especially at low V_{in}. During this time, the error amplifier is driven into its bounds (max V_c), and

the closed loop is temporarily 'open'. The voltage at the inverting input is no longer held equal to V_{ref}, and C_i and C_f will charge to abnormal voltage levels. When the inductor current reaches the new value and the loop is again able to resume functioning, the error voltage on C_i causes a corresponding error in V_o. Further, the time constant for recovery, C_iR_{iz}, may be milliseconds.

The circuit of Figure A-1 does not have this problem because there is no C_i and the circuit can recover almost immediately. The only capacitors are small with relatively high frequency poles with much shorter time constants. This is a good recommendation for discontinuous mode power circuits and current mode control of continuous mode circuits which can be compensated with Figure A-1.

Minimum Load Resistance. Be careful not to use too small a value of feedback resistance, R_f, and/or other loading on the output of the error amplifier. Every amplifier (whether voltage or transconductance type) has a maximum source and sink output current capability. If the load impedance is too small, the ability to swing the output over the desired range will be restricted. For example, the UC1524A is limited to 100 µA source or sink current. An output load resistance less than 25 K will limit the output voltage swing to less than the 2.5 volts necessary to swing the duty cycle over the full range.

Gain Limits. After the desired E/A compensation network has been designed and plotted, make sure the indended error amplifier can provide the gain required at low and high frequencies. The high frequency end of the error amplifier gain characteristic is a -20 dB/decade slope crossing 0 dB at the specified unity gain-bandwidth frequency. This slope terminates at lower frequencies at the specified open loop voltage gain.

Transconductance Amplifiers. Although the open loop output impedance of a transconductance type error amplifier is high, the closed loop gain is determined by the feedback impedance ratio, Z_f/Z_i, exactly the same as with a voltage mode amplifier. Both types of amplifiers have source/sink current limits which determine the minimum load impedance that can be driven without limiting the output voltage swing. The one difference between amplifier types is: the open loop voltage gain (the feedback gain limit) of the voltage type amplifier is fixed, whereas the open loop voltage gain of the transconductance amplifier is gmR_L, and varies with output load (note the feedback resistor is an output load). Curves shown on the UC1524A data sheet illustrate this point. If the required gain runs into the gain limit, it can be raised by increasing all the impedances of the compensation network.

Slope Compensation. Recommended for all continuous mode regulators with current mode control, although not necessary for stability when duty cycle is less than 50%. Ideal slope compensation is achieved by introducing a ramp whose slope is one-half the downslope of the current ramp. It can be either a negative going ramp superimposed on the current programming voltage (the output of the error amplifier), or a positive ramp added to the current ramp. For example, a 0.2 V ramp is easily added to the current ramp by a 10:1 voltage divider in series with the input of the current amplifier, taken from the 2 Volt UC1846 oscillator ramp.

TABLE A-1

	UC1524A UC1525A/27A UC1526	UC1840	UC1846
Gain-Bandwidth (MHz)	3	3	0.8
Transconductance (gm)	.002		
Open Loop Gain (30K load)	37 dB	66 dB	80 dB
Open Loop Gain (1M load)	66 dB	66 dB	>80 dB
Full Output Swing (V)	2.5	3.5	3.5
Min Load R for Full Swing	30K	15K	10K

APPENDIX B

BODE PLOTS

The Bode plot is a method of displaying complex values of circuit gain (or impedance). The gain magnitude in dB is plotted vs. log frequency. The phase angle is plotted separately against the same log frequency scale.

Bode plots are an excellent vehicle for designing switching power supply closed loop systems. They provide good visibility into the gain/phase characteristics of the various loop elements. Calculation of the overall loop is made simply by adding gain in dB and phase in degrees.

The process is further simplified by using straight line approximations of the actual curves, called asymptotes. Calculations are then made only at the frequencies where the asymptotes change direction.

Bode's theorem for simple systems, which includes most switching power supplies: The phase angle of the gain at any frequency is dependent upon the rate of change of gain magnitude vs. frequency. A single pole (simple RC lowpass filter) has a gain slope of -20 dB/decade above its corner frequency and has a corresponding -90 degree phase shift.

FIRST ORDER FILTERS (RC or LR)

Single pole or single zero first order filters all have a gain slope of 20 dB/decade above the corner frequency. The phase shift asymptotes have a slope of 45°/decade, extending 1 decade each side of the corner frequency for a total 90° phase shift (see Figure B-1).

Maximum error between exact values (curved lines) and the straight line approximations are:

Gain — 3 dB
Phase — 5.7°

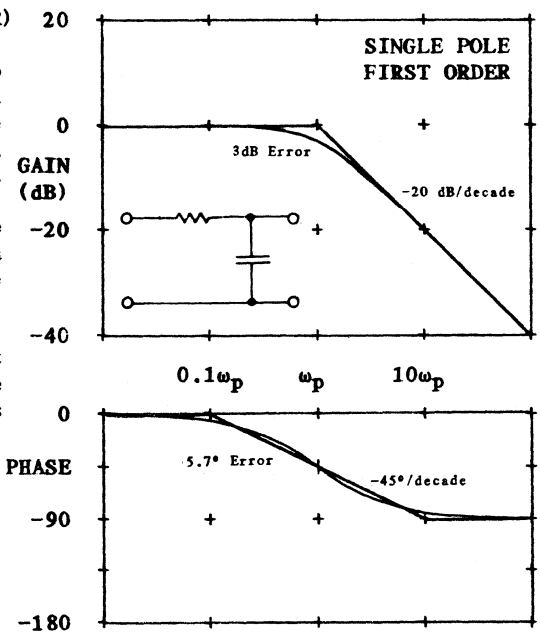


Figure B-1

Low Pass — Single Pole: Figure B-1

$$F(s) = \frac{1}{1+s/\omega_p}, \qquad \omega_p = 1/RC \text{ or } L/R, \qquad s = j\omega$$

Gain: -20 dB/decade slope. Phase: -90° total lag

Single Zero: Has the same gain and phase characteristic as the single pole shown in Figure II-1, except gain increases with frequency. Gain and phase slopes are both positive.

$$F(s) = 1+s/\omega_z, \qquad \omega_z = 1/RC \text{ or } L/R$$

Gain: +20 dB/decade slope. Phase: +90° total lead

Right-Half-Plane Zero. Refers to its location on the complex s-plane. The RHP zero has the same positive gain slope as the conventional (left-half-plane) zero, but the phase slope is negative, like a single pole. The RHP zero holds the loop gain up while adding additional phase lag, making it virtually impossible to provide compensation above its corner frequency. Fortunately, the right-half-plane zero is encountered only in boost and flyback regulators operated in continuous inductor current mode.

$$F(s) = 1-s/\omega_z$$

Gain: +20 dB/decade slope. Phase: -90° total lag

SECOND ORDER FILTERS (Resonant LC)

Low Pass — 2 Pole: Figure B-2

The second order 2 pole resonant LC filter characteristic of Figure B-2 has a -40 dB/decade slope in gain magnitude above the corner (resonant) frequency and a total phase lag of 180 degrees, the same as two single pole first order filters in cascade. Here the similarities end. The gain characteristic has a peak which varies with the Q of the resonant circuit, as shown in Figure B-3. This is of little importance unless the resonant frequency is close to the loop gain crossover frequency, when it could eliminate the gain margin and cause instability.

The phase characteristic slope is -45 degrees/decade with a Q of 0.5. At higher values of Q, Figure B-4 shows the phase slope becomes much more rapid, making compensation by means of first order zeros more difficult.

Gain: -40 dB/decade slope
Gain peak at ω_o: 20 log Q
Phase: -180° total lag
Phase asymptote intercepts: ω/K, $K\omega$, $K = 5^{\frac{1}{2Q}}$

$$F(s) = \frac{1}{1+(s/\omega_o)/Q+(s/\omega_o)^2}$$

where $\omega_o = \frac{1}{\sqrt{LC}}$, $Q = \omega_o L/R_s$, $R_s = R_c+R_L+R_d+R_r+\frac{L}{CR_o}$

Effective series resistance R_s determines Q. R_s includes: capacitor ESR: R_c, inductor: R_L, rectifier dynamic: R_d, leakage inductance effective resistance: R_i, and load resistance: R_o, transformed into its equivalent series R. $(L/C = Z_o^2)$.

Q seldom reaches more than 4 or 5. At full load, low R_o transforms into high R_s. At light loads, diode R_d limits Q.

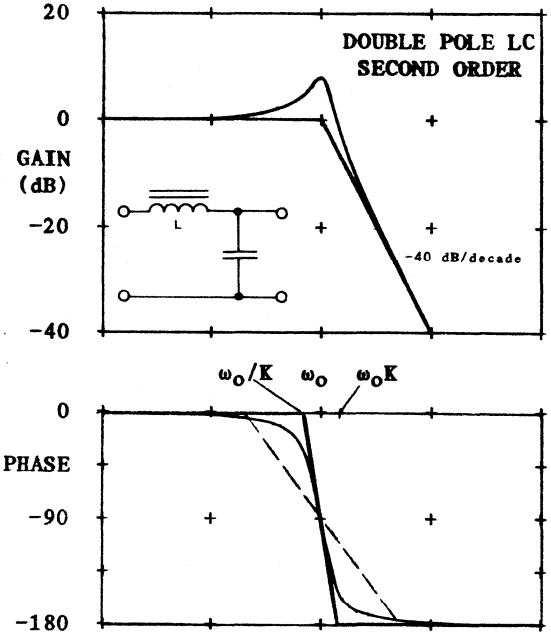


Figure B-2

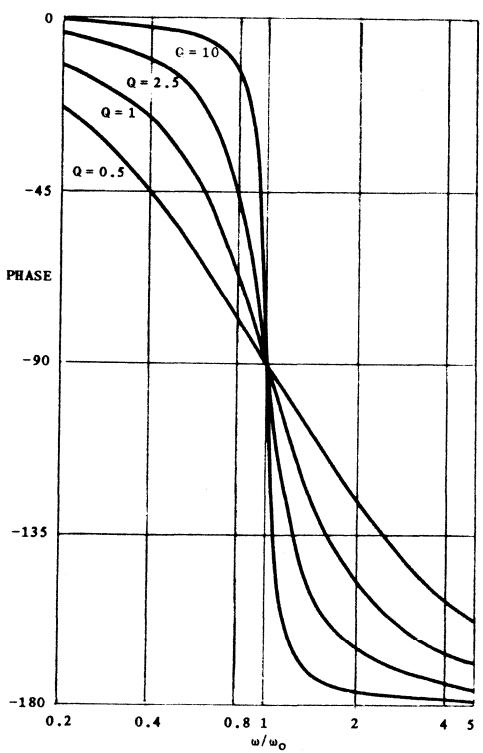


Figure B-4

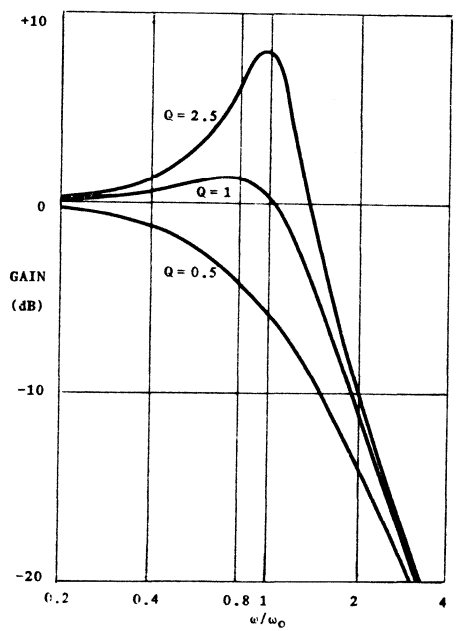


Figure B-3

APPENDIX C

FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL

Example 1: 12 Volt, 60 Watt Output

f_s = 80 kHz, T = 12.5 µsec

V_{in} = 12 to 24 V

V_o = 12 V, I_o = 0.5 to 5 A

R_o = 24 to 2.4 Ohms

I_{sc} = 6 A Short Circuit Limit

Discontinuous Current Mode Boundary Duty Cycle Limit at I_{sc}, min V_{in}:

$D_{max} = 1/(1+V_{in}/V_o) = 0.5$

Max. $t_d = (1-D)T = 6.25$ µsec

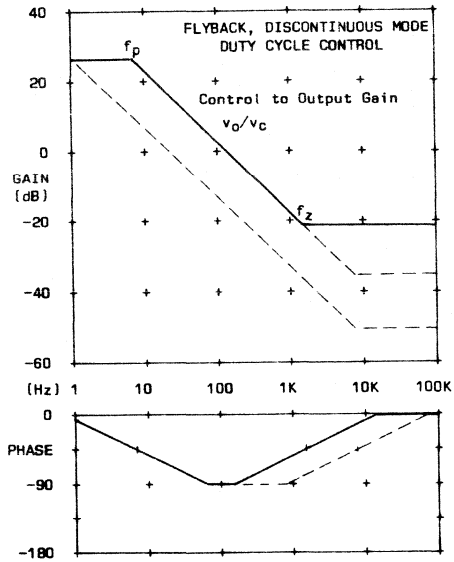
Max. $I_p = 2I_{sc}/(1-D) = 2x6/0.5 = 24$ A

$L = (V_o+V_f)t_d/I_p = 13x6.25/24 = 3.4$ µH

ESR Max for 0.1 V_{pp} Ripple at I_o = 5A:

$R_c = 0.1/20A = 5$ mΩ max (1 mΩ min).

C = 20,000 µF



Basic Equations — Duty Cycle Control:

$D = V_c/V_s$:

DC Relationships:

(1) $V_o = V_{in}D\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = V_{in}\frac{V_c}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}$ (1a) $V_c = \frac{V_oV_s}{V_{in}}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$, $\omega_p = \frac{2}{R_oC}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_c}{V_s}\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}H_e(s) = \frac{V_o}{V_{in}}H_e(s)$

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_oC) = 15.92/R_o$ = 6.63 Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_cC) = 7.95/R_c$ = 1590 Hz at 5 mΩ, 7950 Hz at 1 mΩ

Low Frequency Gain from Equation (2) (V_s = 2.5 V for UC1524A)

$v_o/v_c = .542V_{in}\sqrt{R_o}$ = 20.2 (26.7 dB) at 24 V, 2.4 Ω

= 31.9 (30.1 dB) at 12 V, 24 Ω

V_c must be clamped to 1.25 V to limit Duty Cycle to 0.5 max.

FLYBACK – DISCONTINUOUS INDUCTOR CURRENT – DIRECT DUTY CYCLE CONTROL

<u>Error Amplifier Compensation:</u>

Control I.C.: UC1524A

Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 20$ kHz

E/A gain needed at 20 kHz = 21.5 dB

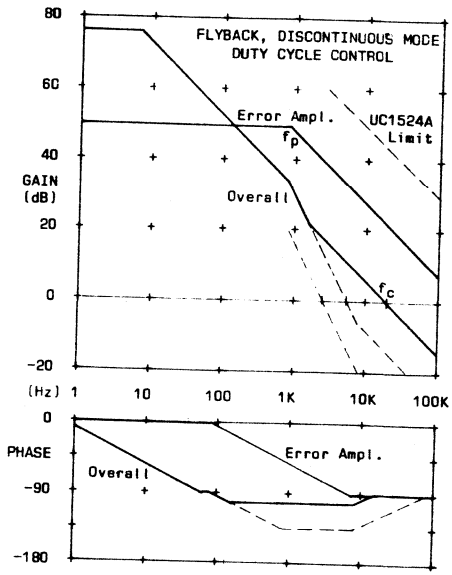
ESR zero, f_z, cancelled by pole f_p at max$f_z/10$. This increases low frequency gain and adds 45° more phase lag, still leaving a phase margin of 45°:

$f_p = \max f_z/10 = 795$ Hz

E/A gain required below f_p is:

$$21.5 + 20\log(20{,}000/795) = 49.5 \text{ dB}$$

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):



$$(1a)\quad V_c = \frac{V_o V_s}{V_{in}}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}} = \frac{12x2.5-/3.4x.08}{V_{in}\sqrt{R_o}} = 0.188 \text{ to } 1.19 \text{ V.} \quad \Delta V_c = 1.0 \text{ V}$$

Output voltage error with actual E/A DC gain of 298 (49.5 dB):

$\Delta V_o = \Delta V_c/298 = 3.4$ mV (120 mV = 1% regulation)

<u>Implementation:</u> Circuit of Appendix A-1 (omit R_p and C_p)

UC1524A has transconductance error amplifier (gm = .002)

With $R_f = 3M\Omega$, max. gain = $gmR_f = 6000$ (75.6 dB, > 64 dB required, OK)

Gain required below $f_p = 298$ (49.5 dB) = R_f/R_i.

$R_i = 3M/298 = 10K$

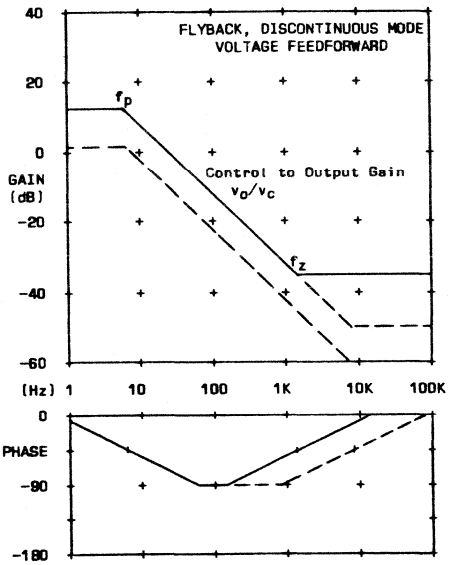
Pole at 795 Hz:

$C_f = 1/(2\pi f_p R_f) = 67$ pF

FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - VOLTAGE FEEDFORWARD CONTROL

Example 2: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 1.



Basic Equations — Voltage Feedforward:

$D = V_c/V_s$, $V_s = V_{in}/K$, $K = V_{in}D/\max V_c$

DC Relationships:

(1) $V_o = V_{in}D\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = KV_c\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}}$ (1a) $V_c = \frac{V_o}{K}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$, $\omega_p = \frac{2}{R_oC}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation and audio susceptibility.

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_oC) = 15.92/R_o$ = 6.63 Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_cC) = 7.95/R_c$ = 1590 Hz at 5 mΩ, 7950 Hz at 1 mΩ

Low Frequency Gain from Equation (2) (max V_c = 3.5 V for UC1840)

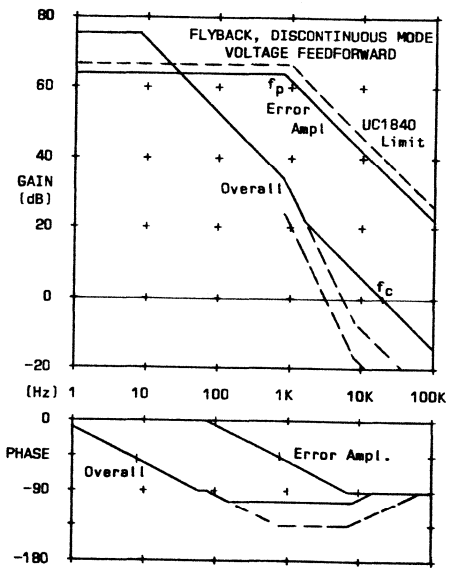
$K = V_{in}D/\max V_c = 12x0.5/3.5 = 1.71$ (feedforward factor)

$v_o/v_c = 2.52\sqrt{R_o}$ = 3.91 (11.8 dB) at 2.4 Ω

= 12.35 (21.8 dB) at 24 Ω

V_{in} = 12 to 24 V

FLYBACK – DISCONTINUOUS INDUCTOR CURRENT – VOLTAGE FEEDFORWARD CONTROL



Error Amplifier Compensation:

Control I.C.: UC1840

Crossover frequency (0 dB loop gain)

$f_c = f_s/4 = 20$ kHz

E/A gain needed at 20 kHz = 35.8 dB

ESR zero, f_z, is cancelled by pole f_p at max $f_z/10$. This increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$f_p = \max f_z/10 = 795$ Hz

E/A gain required below f_p is:

$35.8 + 20\log(20{,}000/795) = 63.8$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

$$(1a)\quad V_c = \frac{V_o}{K}\left(\frac{2Lf}{R_o}\right)^{\frac{1}{2}} = \frac{12\sqrt{2x3.4x.08}}{1.71\sqrt{R_o}} = 1.05 \text{ to } 3.33 \text{ V.} \quad \Delta V_c = 2.28 \text{ V}$$

Output voltage error with actual E/A DC gain of 1550 (63.8 dB):

$\Delta V_o = \Delta V_c/1550 = 1.5$ mV (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Voltage feedforward factor, K, in UC1840 is set by an independent ramp generator whose slope varies directly with V_{in}. A minimum ramp charging current of 36 μA is chosen (near the bottom end of the optimum range).

$R_r = \min V_{in}/\min I_r = 12/36\mu A = 330K$

$dv/dt = I_r/C_r = V_{in}/R_rC_r = \max v_c/t_{on}$. $\quad R_rC_r = V_{in}t_{on}/\max V_c = K/f$

$C_r = K/fR_r = 1.71/(80Kx330K) = 65$ pF

UC1840 has voltage mode amplifier with 65 dB gain, > 63.8 dB required, OK.

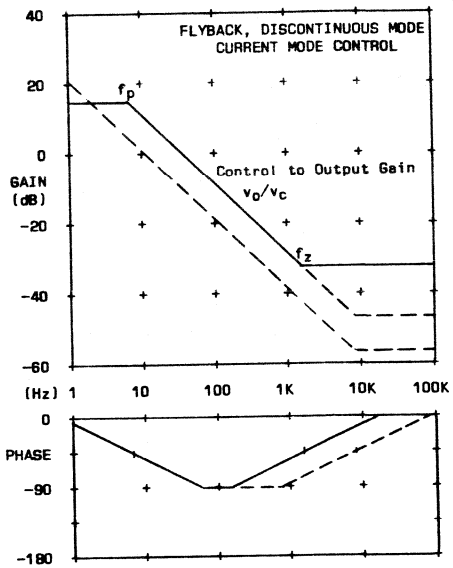
$R_f = 3M$, chosen somewhat arbitrarily because of high gain required.

Gain required below $f_p = 1550$ (64 dB) $= R_f/R_i$. $\quad R_i = 3M/1550 = 2K$.

Pole at $f_p = 795$ Hz: $\quad C_f = 1/(2\pi f_p R_f) = 67$ pF

FLYBACK – DISCONTINUOUS INDUCTOR CURRENT – CURRENT MODE CONTROL

Example 3: 12 Volt, 60 Watt Output



All power circuit parameters are the same as Example 1.

Basic Equations — Current Mode Control:

$$I_p = KV_c, \quad K = \max I_p / \max V_c$$

DC Relationships:

(1) $V_o = V_{in}D\left(\frac{R_o}{2Lf}\right)^{\frac{1}{2}} = KV_c\sqrt{R_oLf/2}$ (1a) $V_c = \frac{V_o\sqrt{2}}{K\sqrt{LfR_o}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K\sqrt{RoLf/2}\ H_e(s)$. $H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$, $\omega_p = \frac{2}{R_oC}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation and audio susceptibility.

Corner Frequencies from Equation (2):

$f_p = 2/(2\pi R_oC) = 15.92/R_o$ = 6.63 Hz at 2.4 Ω, .663 at 24 Ω

$f_z = 1/(2\pi R_cC) = 7.95/R_c$ = 1590 Hz at 5 mΩ, 7950 Hz at 1 mΩ

Low Frequency Gain from Equation (2) (V_c clamped to 2.4 V for 24 A I_{sc})

$K = \max I_p / \max V_c = 24/2.4 = 10$

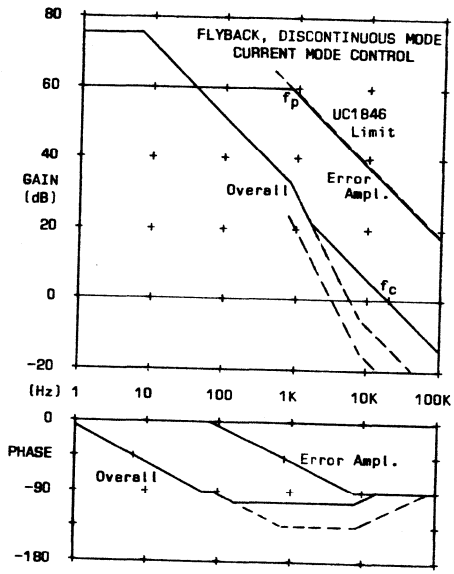
$v_o/v_c = 3.7\sqrt{R_o}$ = 5.73 (15.2 dB) at 2.4 Ω

= 18.1 (25.2 dB) at 24 Ω

V_{in} = 12 to 24 V

FLYBACK – DISCONTINUOUS INDUCTOR CURRENT – CURRENT MODE CONTROL

Error Amplifier Compensation:



Control I.C.: UC1846

Crossover frequency (0 dB loop gain)

$f_c = f_s/4 = 20$ kHz

E/A gain needed at 20 kHz = 32 dB

ESR zero, f_z, is cancelled by pole f_p at max $f_z/10$. This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$f_p = \max f_z/10 = 795$ Hz

E/A gain required at and below f_p is:

$32 + 20\log(20{,}000/795) = 60$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \dfrac{V_o\ -/2}{K-/LfR_o} = \dfrac{12\ -/2}{10-/3.4x.08R_o} = 3.25/-/R_o = 0.664$ to 2.1 V. $\Delta V_c = 1.44$ V

Output voltage error with actual E/A DC gain of 1000 (60 dB):

$\Delta V_o = \Delta V_c/1000 = 1.44$ mV (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Current control factor (K = 10) is set with the UC1846 by the fixed gain (3X) of the current amplifier and the current sampling resistor, R_s:

$K = I_p/V_c = 10 = 1/(3R_s)$. $R_s = 1/(30) = .033\ \Omega$

UC1846 error amplifier gain limit >80 dB with R_f>30K, > 60 dB required, OK.

R_f = 3 M, chosen somewhat arbitrarily because of high gain required.

Gain required below f_p = 1000 (60 dB) = R_f/R_i. $R_i = 3M/1000 = 3K$.

Pole at f_p = 795 Hz: $C_f = 1/(2\pi f_p R_f) = 67$ pF

BUCK - CONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL

Example 4: 12 Volt, 240 Watt Output

f_s = 40 kHz, T = 25 µsec

V_{in} = 30 to 60 V

V_o = 12 V, I_o = 2 to 20 A

R_o = 6 to 0.6 Ohms

I_{sc} = 24 A Short Circuit Limit

Continuous Current Mode Boundary:

Min. I_o = 2 A

Max. $\Delta I_L = 2(\min I_o) = 4$ A

$D = V_o/V_{in}$ = 0.2 to 0.4

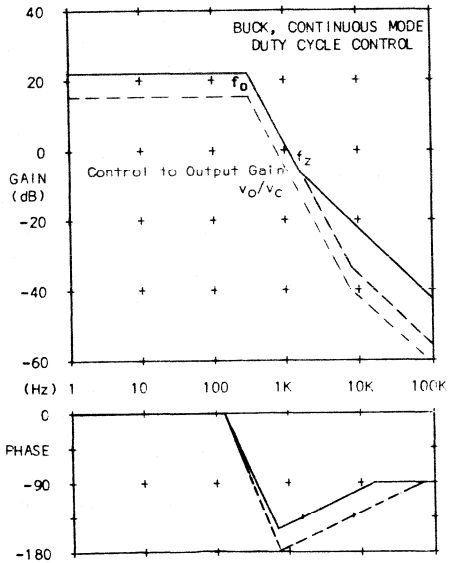
$t_{off} = 0.8 \times 25 = 20$ µs max

$L = V_o t_{off}/\Delta I_L = 12 \times 20/4 = 60$ µH

ESR Max for 0.1 V_{pp} Ripple at ΔI_L = 4 A:

R_c = 25 mΩ max (5 mΩ min)

C = 4000 µF



Basic Equations — Duty Cycle Control:

$D = V_c/V_s$:

DC Relationships:

(1) $V_o = V_{in}D = V_{in}\frac{V_c}{V_s}$ (1a) $V_c = \frac{V_o V_s}{V_{in}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s} H_e(s)$. $H_e(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$, $\omega_o = \frac{1}{\sqrt{LC}}$, $\omega_z = \frac{1}{R_c C}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_c}{V_s} H_e(s) = \frac{V_o}{V_{in}} H_e(s)$ $Q = \frac{R_o}{\omega_o L}$

Corner Frequencies from Equation (2):

$f_o = 1/(2\pi\sqrt{LC}) = 325$ Hz

$f_z = 1/(2\pi R_c C) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

UC1524A ramp is 2.5 V at 80 kHz. One output is not used which limits duty cycle to 50% max. at 40kHz. V_s projects to 5 V over the full 40 kHz cycle.

Low Frequency Gain from Equation (2):

$v_o/v_c = V_{in}/5$ = 12 (21.6 dB) at 60 V

= 6 (15.6 dB) at 30 V

BUCK - CONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL

Error Amplifier Compensation:

Control I.C.: UC1524A
Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 21.5 dB

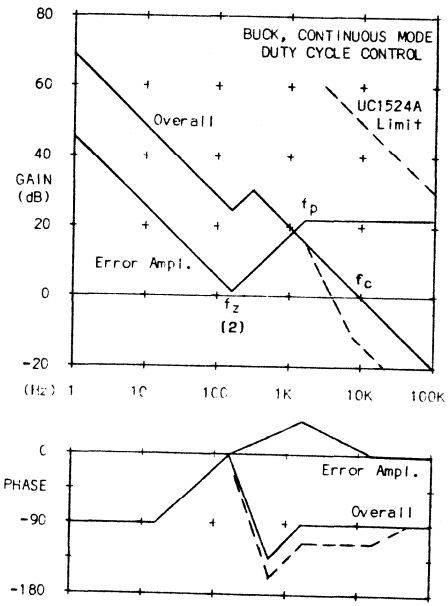
A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o/2$. This provides additional phase shift at f_o for sudden second order transition.

$f_z = 325/2 = 162$ Hz

ESR zero, f_z, is canceled by pole f_p at least 5 times above f_o to avoid adding more phase lag at f_o. This happens to coincide with min. ESR zero, f_z.

$f_p = 1590$ Hz with 21.5 dB gain



E/A gain required at f_z is: $21.5 - 20\log(1590/162) = 1.7$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o V_s}{V_{in}} = \frac{12x5}{V_{in}} = 1$ to 2 V. $\Delta V_c = 1$ V

Output voltage error with actual E/A DC gain of 180 (45 dB at 1 Hz):

$\Delta V_o = \Delta V_c/180 = 5.5$ mV (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-2 (omit R_p, C_p and R_{fp})

UC1524A has transconductance error amplifier (gm = .002). Min. load resistance (min R_{fz}) is 30K. R_{iz} is appx. $1xR_{fz}$ (gain is 1.7 dB at f_z).

Set $R_{iz} = 50K$

Zero 2 at 162 Hz: $C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi\ 162 \times 50K = .02\ \mu F$

Pole 2 at 1590 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1) = 50K/(50K \times 2\pi\ 1590 \times .02) = 5.6K$

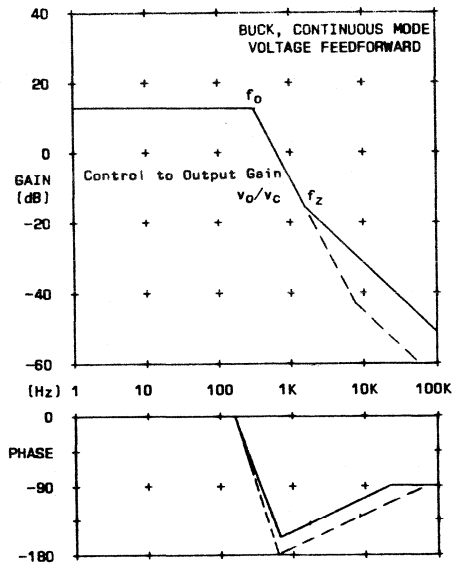
1.7 dB (1.22) gain at 162 Hz: $R_{fz} = 1.22(R_{ip} + R_{iz}) = 68K$

Zero 1 at 162 Hz: $C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi\ 162 \times 68K) = .0144\ \mu F$

Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

BUCK - CONTINUOUS INDUCTOR CURRENT - VOLTAGE FEEDFORWARD CONTROL

Example 5: 12 Volt, 240 Watt Output



All power circuit parameters are the same as Example 4.

Basic Equations — Voltage Feedforward

$D = V_c/V_s$, $V_s = V_{in}/K$, $K = V_{in}D/\max V_c$

DC Relationships:

(1) $V_o = V_{in}D = KV_c$ (1a) $V_c = \frac{V_o}{K}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K\,H_e(s)$. $H_e(s) = \frac{1 + s/\omega_o}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$, $\omega_o = \frac{1}{\sqrt{LC}}$, $\omega_z = \frac{1}{R_cC}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation $Q = \frac{R_o}{\omega_o L}$

Corner Frequencies from Equation (2):

$f_o = 1/(2\pi\sqrt{LC}) = 325$ Hz

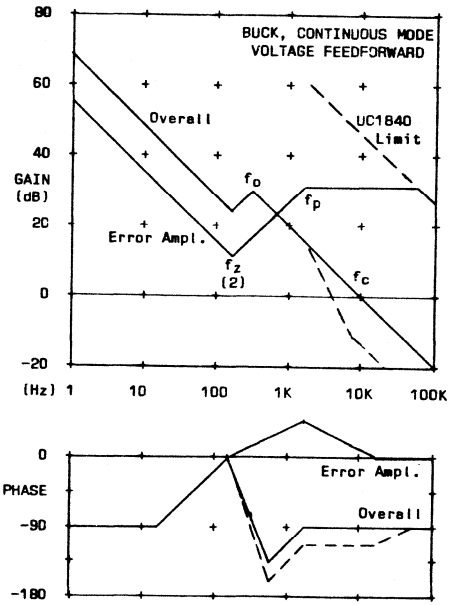
$f_z = 1/(2\pi R_cC) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

Low Frequency Gain from Equation (2) (max V_c = 3.5 V for UC1840):

$K = V_{in}D/\max V_c = 30 \times 0.5/3.5 = 4.29$ (feedforward factor)

$v_o/v_c = V_{in}/5 = 4.29$ (12.6 dB) at 30 to 60 V in.

BUCK - CONTINUOUS INDUCTOR CURRENT - VOLTAGE FEEDFORWARD CONTROL



Error Amplifier Compensation:

Control I.C.: UC1840
Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 31 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o/2$. This provides additional phase shift at f_o for sudden second order transition.

$f_z = 325/2 = 162$ Hz

ESR zero, f_z, is canceled by pole f_p at least 5 times above f_o to avoid adding more phase lag at f_o. This happens to coincide with min. ESR zero, f_z.

$f_p = 1590$ Hz with 31 dB gain

E/A gain required at f_z is: $31 - 20\log(1590/162) = 11.2$ dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o}{V} = \frac{12}{4.29} = 2.8$ V constant DC. $\Delta V_c = 0$

DC Output voltage error is theoretically zero. Loop gain is required only for good dynamic response.

Implementation: Circuit of Appendix A-2 (omit R_p, C_p and R_{fp})

Voltage feedforward factor, K, in UC1840 is set by an independent ramp generator whose slope varies proportional to V_{in}. Minimum ramp charging current of 30 μA is chosen, near the bottom of the optimum range.

$R_r = \min V_{in}/\min I_r = 30/30\mu A = 1M$

$dv/dt = I_r/C_r = V_{in}/R_rC_r = \max v_c/t_{on}$. $R_rC_r = V_{in}t_{on}/\max v_c = K/f$

$C_r = K/fR_r = 4.29/(40Kx1M) = 107$ pF

Set $R_{iz} = 50K$. With gain appx. 4 at 162 Hz (f_z), R_f of 200K is OK to drive.

Zero 2 at 162 Hz: $C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi\ 162 \times 50K = .02$ μF

Pole 2 at 1590 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1) = 50K/(50K \times 2\pi\ 1590 \times .02) = 5.6K$

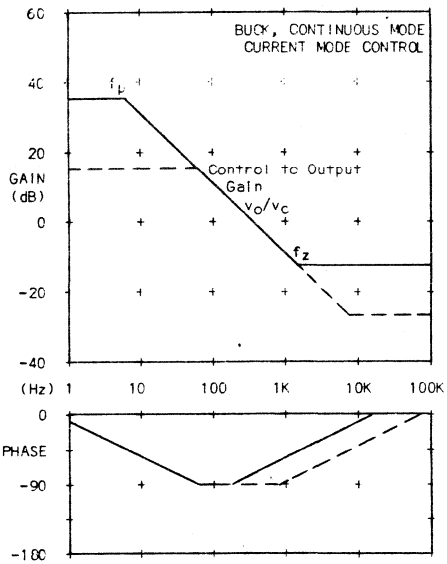
11.2 dB (3.63) gain at 162 Hz: $R_{fz} = 3.63(R_{ip} + R_{iz}) = 202K$

Zero 1 at 162 Hz: $C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi\ 162 \times 200K) = .0049$ μF

Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1840 error amplifier at a frequency below 1 Hz.

BUCK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Example 6: 12 Volt, 240 Watt Output



All power circuit parameters are the same as Example 4.

Basic Equations — Current Mode Control:

$$I_L = KV_c, \quad K = \max I_L / \max V_c$$

DC Relationships:

(1) $V_o = I_L R_o = KV_c R_o$ (1a) $V_c = \frac{V_o}{KR_o}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = KR_o\, H_e(s)$. $H_e(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}$, $\omega_p = \frac{1}{R_o C}$, $\omega_z = \frac{1}{R_c C}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = 0$ Inherent good line regulation and audio susceptibility

Corner Frequencies from Equation (2):

$f_p = 1/(2\pi R_o C)$ = 66.3 Hz at 0.6 Ω, 6.63 Hz at 6 Ω

$f_z = 1/(2\pi R_c C) = 39.8/R_c$ = 1590 Hz at 25 mΩ, 7950 Hz at 5 mΩ

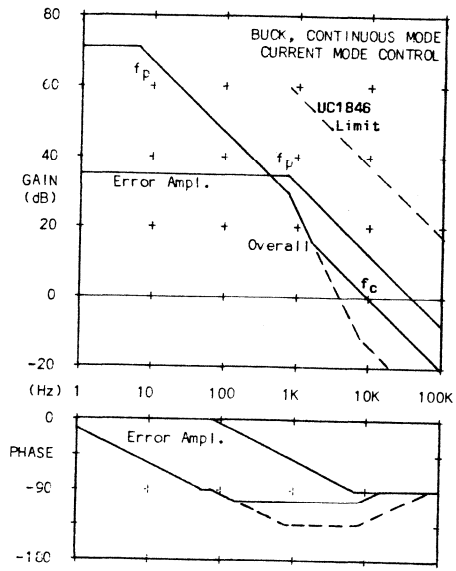
Low Frequency Gain from Equation (2) (max V_c clamped to 2.5 V for 25 A I_{sc}):

$K = \max I_L / \max V_c = 25/2.5 = 10$

$v_o/v_c = KR_o$ = 6 (15.6 dB) at 0.6 Ω, 60 (35.6 dB) at 6 Ω

BUCK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

<u>Error Amplifier Compensation:</u>



Control I.C.: UC1846
Crossover frequency (0 dB loop gain):

$f_c = f_s/4 = 10$ kHz

E/A gain needed at 10 kHz = 12 dB

ESR zero, f_{zc}, is canceled by pole f_p at max $f_z/10$. This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

$$f_p = \max f_z/10 = 795 \text{ Hz}$$

E/A gain required at and below f_p is:

$$12 + 20\log(10000/795) = 34 \text{ dB } (50)$$

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o}{KR_o} = \frac{12}{10R_o} = 0.2$ to 2 V. $\Delta V_c = 1.8$ V

Output voltage error with actual E/A gain of 50 (34 dB):

$$\Delta V_o = \Delta V_c/50 = 36 \text{ mV } (0.3\% \text{ regulation})$$

<u>Implementation:</u> Circuit of Appendix A-1 (omit R_p and C_p)

Current control factor, K = 10, in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor R_s.

$$K = I_L/V_c = 10 = 1/(3R_s). \quad R_s = 1/30 = .033\ \Omega$$

UC1846 error amplifier gain limit is >80 dB with R_f >30K. 34 dB needed, OK

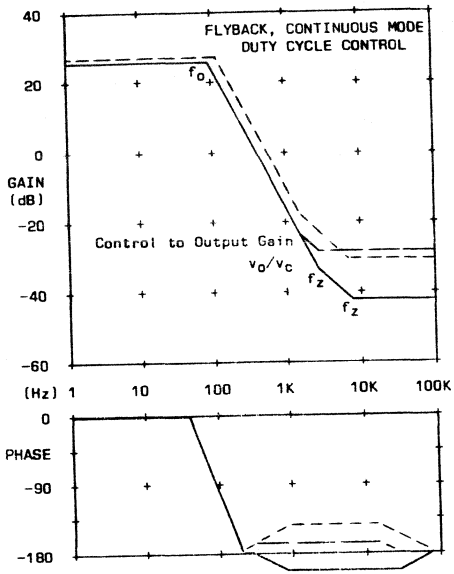
Gain required at and below f_p = 795 Hz is 50 (34 dB) = R_f/R_i.

Let R_f = 500K, $R_i = R_f/50 = 10K$

1 Pole at f_p = 795 Hz. $C_f = 1/(2\pi f_p R_f) = 400$ pF

Slope compensation: Current downslope is 4A/20μs, or 5A projected over 25 μs period, equating to 5x.033 = .165 volts p-p at input of current sense amplifier. Compensation ramp should be .165/2 = .082 V positive ramp. UC1846 oscillator ramp is 2 V. A 24:1 divider provides .083 V. Put 1K between current sense R_s and current sense amplifier input, and 24K from timing capacitor C_t to current sense ampl. input.

FLYBACK - CONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL



Example 7: 12 Volt, 60 Watt Output

f_s = 80 kHz, T = 12.5 µsec

V_{in} = 12 to 24 V

V_o = 12 V, I_o = 0.5 to 5 A

R_o = 24 to 2.4 Ohms

I_{sc} = 6 A Short Circuit Limit

Continuous Current Mode Boundary:

Min. I_o = 0.5 A

$D = V_o/(V_o+V_i)$ = 0.33 to 0.5

Max. $\Delta I_L = 2(\min I_o)/(1-D\min)$ = 1.5 A

$t_{off} = 12.5(1-D)$ = 8.33 µs max

$L = V_o t_{off}/\Delta I_L = 12x8.33/1.5$ = 72 µH

$I_L max = \max I_o/(1-D\max)$ = 10 A

ESR Max for 0.1 V_{pp} Ripple at I_L= 10 A:

R_c = 10 mΩ max (2 mΩ min), C = 10,000 µF

Basic Equations — Duty Cycle Control:

$D = V_c/V_s$: $\omega_o = \frac{1-D}{\sqrt{LC}}$, $\omega_z = \frac{1}{R_c C}$, $Q = \frac{R_o}{\omega_o L}$

DC Relationships:

(1) $V_o = V_{in}D/(1-D) = V_{in}/(V_s/V_c-1)$ (1a) $V_c = V_s\frac{V_o}{V_i+V_o}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s}(1+V_o/V_i)^2 f1(s)\ He(s)$. $He(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$,

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_c}{V_s} He(s) = \frac{V_o}{V_{in}} He(s)$ RHP zero: $f1(s) = 1 - \frac{sL}{R}\frac{V_o(V_o + V_i)}{V_i^2}$

Corner Frequencies:

$f_o = (1-D)/(2\pi\sqrt{LC})$ = 94 Hz at 12 V, 125 Hz at 24 V

f_z (ESR) $= 1/(2\pi R_c C)$ = 1590 Hz at 10 mΩ, 7950 Hz at 2 mΩ

f_z (RHP) = 2728 Hz at 12 V and 2.4 Ω, = 7275 Hz at 24 V and 2.4 Ω

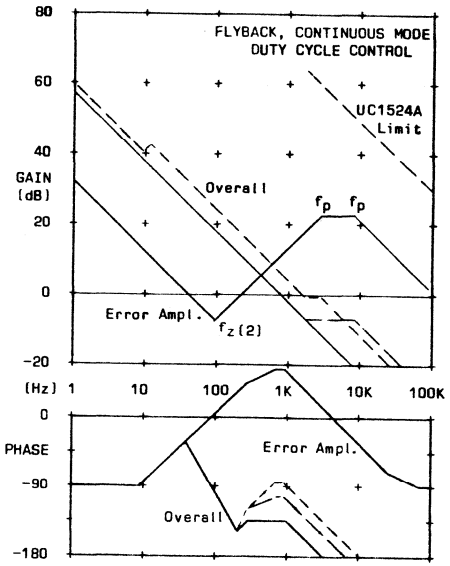
UC1524A ramp V_s = 2.5 V. The two outputs of the UC1524A are paralleled.

Low Frequency Gain from Equation (2):

v_o/v_c = 19.2 (25.6 dB) at 12 V, = 21.6 (26.7 dB) at 24 V

FLYBACK - CONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL

Error Amplifier Compensation:



Control I.C.: UC1524A
Crossover frequency (0 dB loop gain):

f_c = 800 Hz (best achievable - RHPzero)

E/A gain needed at 800 Hz = 11.6 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at f_o are compensated by two zeros at $f_z = f_o$.

f_z = 94 Hz

E/A gain required at f_z: -7 dB

Two additional poles cancel the ESR zero and right-half-plane zero. The location of these two poles is adjusted by trail and error. Although above the crossover frequency these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

f_p = 2700 Hz at 22.2 dB gain, f_p = 8000 Hz also at 22.2 dB

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = V_s \frac{V_o}{V_{in}+V_o}$ = 0.833 to 1.25 V. ΔV_c = .417 V

Output voltage error with actual E/A DC gain of 40 (32 dB at 1 Hz):

$\Delta V_o = \Delta V_c/40$ = 10 mV (0.1% regulation)

Implementation: Circuit of Appendix A-2 (omit R_{fp})

UC1524A has transconductance error amplifier (gm = .002). Min. load resistance (min R_{fz}) is 30K. R_{iz} is appx. 2xR_{fz} (gain is -7 dB at f_z).

Set R_{iz} = 100K

Zero 2 at 94 Hz: $C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi\ 94 \times 100K$ = .017 µF

Pole 2 at 2700 Hz: $R_{ip} = R_{iz}/(R_{iz}\omega_{p2}C_i - 1) = 100K/(100K \times 2\pi\ 2700 \times .017-1)$ = 3.6K

-7 dB (.45) gain at 94 Hz: $R_{fz} = .45(R_{ip} + R_{iz})$ = 47K

Zero 1 at 94 Hz: $C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi\ 94 \times 47K)$ = .036 µF

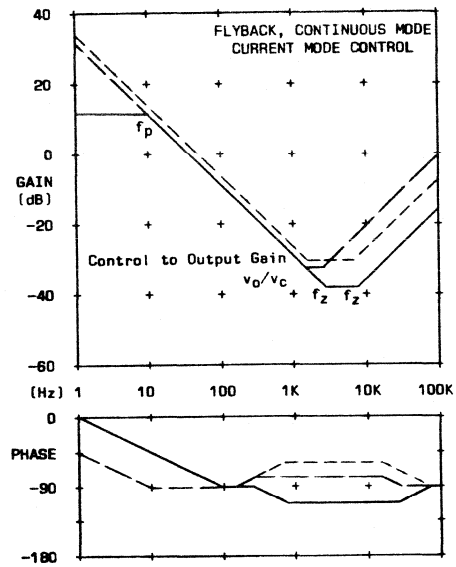
Pole 1 at 0 Hz: Omitting R_{fp} (open), $\omega_{p1} = 0$. Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

Pole 3 at 8000 Hz. $R_p = R_{ip}/10$ = 360 Ω. $C_p = 1/(2\pi f_{p3}R_p)$ = .055 µF

FLYBACK – CONTINUOUS INDUCTOR CURRENT – CURRENT MODE CONTROL

Example 8: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 7.



Basic Equations — Current Mode Control:

$I_o = I_L(1-D)$, $I_L = KV_c$, $K = \max I_L/\max V_c$, $\omega_z = \frac{1}{R_c C}$, $\omega_p = \frac{1+D}{R_o C}$, $D = \frac{V_o}{V_o + V_{in}}$

DC Relationships:

(1) $V_o = V_{in}\, D/(1-D) = K V_c R_o \frac{V_{in}}{V_o+V_{in}}$ (1a) $V_c = \frac{V_o(V_o+V_{in})}{K R_o V_{in}}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = K R_o \frac{V_{in}}{(2V_o + V_{in})}\, f1(s)\, H_e(s)$. $H_e(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o^2}{2V_oV_{in} + V_{in}^2} H_e(s)$ RHP zero: $f1(s) = 1 - \frac{sL}{R}\frac{V_o(V_o + V_{in})}{V_{in}^2}$

Corner Frequencies:

$f_p = (1+D)/(2\pi R_o C) = 0.884$ Hz at 24 V, 24 Ω, = 9.95 Hz at 12 V, 2.4 Ω

f_z (ESR) $= 1/(2\pi R_c C)$ = 1590 Hz at 10 mΩ, 7950 Hz at 2 mΩ

f_z (RHP) = 2728 Hz at 12 V and 2.4 Ω, = 7275 Hz at 24 V and 2.4 Ω

Low Frequency Gain from Equation (2):

$$K = \frac{\max I_L}{\max V_c} = \frac{\max I_o}{(1-D)\max V_c} = \frac{6}{(1-.5)2.5} = 4.8$$

v_o/v_c = 57.6 (35.2 dB) at 24 V, 24 Ω, = 3.84 (11.7 dB) at 12 V, 2.4 Ω

FLYBACK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Error Amplifier Compensation:

Control I.C.: UC1846
Crossover frequency (0 dB loop gain):

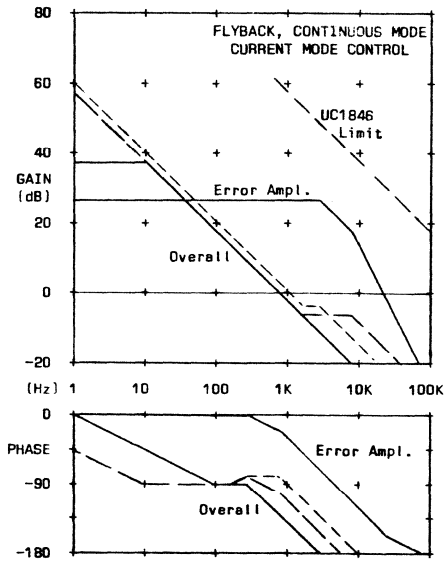
f_c = 800 Hz (best achievable - RHPzero)

E/A gain needed at 800 Hz = 26.4 dB

Two poles cancel the ESR zero and right-half-plane zero. The location of these two poles is set by trail and error. Although above the crossover frequency, these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

f_p = 2700 Hz at 26.4 dB gain
f_p = 8000 Hz at 17.1 dB

The E/A gain is flat (26.4 dB) below the first pole at 2700 Hz.



Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) $V_c = \frac{V_o(V_o+V_{in})}{KR_o\ V_{in}}$ = 0.156 to 2.08 V. ΔV_c = 1.92 V

Output voltage error with actual E/A DC gain of 20.1 (26.4 dB below 2700 Hz):

$\Delta V_o = \Delta V_c/20.1 = 1.92/20.1 = 95$ mV (1% regulation)

Implementation: Circuit of Appendix A-1

Current control factor, K = 4.8, in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor R_s.

$K = I_L/V_c = 4.8 = 1/(3R_s)$. $R_s = .069\ \Omega$

UC1846 error amplifier gain limit is >80 dB with R_f >30K. 26.4 dB needed, OK

Gain required (26.4 dB) = 20.9 = R_f/R_i. Let R_f = 500K, R_i = 500K/20.9 = 24K.

Pole 1 at f_p = 2700 Hz. $C_f = 1/(2\pi f_p R_f) = 120$ pF
Pole 2 at f_p = 8000 Hz $R_p = R_i/10 = 2.4K$. $C_p = 1/(2\pi f_p R_p) = 8200$ pF

Slope compensation: Current downslope is 1.5A/8.33 µs, or 2.25A projected over the 12.5 µs period. This equates to 2.25x.069 = .155 volts p-p at the current sense amplifier input. Compensation ramp should be .155/2 = .078 V positive ramp. UC1846 oscillator ramp is 2 V. A 25:1 divider provides .077 V. Put 1K between current sense resistor R_s and current sense amplifier input, and 24K from timing capacitor C_t to current sense amplifier input.

BOOST CONFIGURATIONS — BASIC EQUATIONS

Boost regulator topologies have the same general characteristics as their flyback circuit counterparts. The Bode plots have the same shape, and the same type of compensation is employed. The specific values of gain and pole/zero frequencies are slightly different because of modifying factors in the various basic equations: Accordingly, only the basic equations are given for the boost circuits.

BOOST — Discontinuous Inductor Current — Duty Cycle Control:

DC Relationships:

(1) $V_O = V_{in}(1/2 + \sqrt{1/4 + D^2/J})$, $\quad D = V_c/V_s$, $\quad J = 2Lf_s/R_O$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s\sqrt{J}} \frac{(1-V_{in}/V_O)^{1/2}}{1-V_{in}/2V_O} H_{e(s)}$. $\quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o}{V_{in}} H_e(s)$, $\quad \omega_z = \frac{1}{R_cC}$, $\quad \omega_p = \frac{2+1/\sqrt{1+4D^2/J}}{R_OC}$

BOOST — Discontinuous Inductor Current — Voltage Feedforward:

DC Relationships: $\quad V_s = V_{in}/K$, $\quad K = V_{in}D/\max V_c$

(1) $V_O = V_{in}(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_{in}^2})$, $\quad D = V_c/V_s = \frac{KV_c}{V_i}$, $\quad J = 2Lf_s/R_O$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{K}{\sqrt{J}} \frac{(1-V_{in}/V_O)^{1/2}}{1-V_{in}/2V_O} H_{e(s)}$. $\quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o}{2V_O-V_{in}} H_e(s)$, $\quad \omega_z = \frac{1}{R_cC}$, $\quad \omega_p = \frac{2+1/\sqrt{1+4D^2/J}}{R_OC}$

BOOST — Discontinuous Inductor Current — Current Mode Control:

DC Relationships: $\quad I_p = KV_c$, $\quad K = \max I_p/\max V_c$

(1) $V_O = V_{in}(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_{in}^2})$, $\quad D = V_c/V_s = \frac{KV_c}{V_i}$, $\quad J = 2Lf_s/R_O$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{K}{\sqrt{J}} \frac{(1-V_{in}/V_O)^{1/2}}{1-V_{in}/2V_O} H_{e(s)}$. $\quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o}{2V_O-V_{in}} H_e(s)$, $\quad \omega_z = \frac{1}{R_cC}$, $\quad \omega_p = \frac{2+1/\sqrt{1+4D^2/J}}{R_OC}$

BOOST CONFIGURATIONS — BASIC EQUATIONS

Boost — Continuous Inductor Current — Direct Duty Cycle Control:

$$D = V_c/V_s, \quad (1-D) = V_i/V_o, \quad \omega_o = \frac{1-D}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_cC}, \quad Q = \frac{R_o}{\omega_oL}$$

DC Relationships:

(1) $V_o = V_{in}/(1-D) = V_{in}/(1-V_c/V_s)$ (1a) $V_c = V_s\frac{V_o-V_{in}}{V_o}$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{V_{in}}{V_s}\frac{V_o^2}{V_{in}^2} f1(s)\, He(s)$. $He(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_o)/Q + (s/\omega_o)^2}$,

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o}{V_{in}} He(s)$ RHP zero: $f1(s) = 1 - \frac{sL}{R}\frac{V_o^2}{V_i^2}$

Boost — Continuous Inductor Current — Current Mode Control:

$$I_o = I_L(1-D), \quad I_L = KV_c, \quad \omega_p = \frac{2}{R_oC}, \quad \omega_z = \frac{1}{R_cC}, \quad D = \frac{V_o-V_{in}}{V_o}$$

DC Relationships:

(1) $V_o = -\sqrt{KV_cR_oV_i}$ (1a) $V_c = V_o^2/(KR_oV_i)$

Control to Output Gain:

(2) $\frac{v_o}{v_c} = \frac{KR_o}{2}\frac{V_{in}}{V_o} f1(s)\, He(s)$. $He(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}$

Line to Output Gain:

(3) $\frac{v_o}{v_{in}} = \frac{V_o}{2V_{in}} He(s)$ RHP zero: $f1(s) = 1 - \frac{sL}{R}\frac{V_o^2}{V_i^2}$

Voltage feedforward control does not perform effectively with continuous mode boost and flyback circuits, and this use is not recommended.

THE RIGHT-HALF-PLANE ZERO -- A SIMPLIFIED EXPLANATION

In small signal loop analysis, poles and zeros are normally located in the left half of the complex s-plane. The Bode plot of a conventional or left-half-plane zero has the gain magnitude rising at 20 dB/decade above the zero frequency with an associated phase lead of 90°. This is the exact opposite of a conventional pole, whose gain magnitude *decreases* with frequency and the phase *lags* by 90°. Zeros are often introduced in loop compensation networks to cancel an existing pole at the same frequency; likewise poles are introduced to cancel existing zeros in order to maintain total phase lag around the loop less than 180° with adequate phase margin.

The right-half-plane (RHP) zero has the same 20 dB/decade rising gain magnitude as a conventional zero, but with 90° phase *lag* instead of lead. This characteristic is difficult if not impossible to compensate. The designer is usually forced to roll off the loop gain at a relatively low frequency. The crossover frequency may be a decade or more below what it otherwise could be, resulting in severe impairment of dynamic response.

The RHP zero never occurs in circuits of the buck family. It is encountered only in flyback, boost and Ćuk circuits, and then only when these circuits are operated in the continuous inductor current mode.

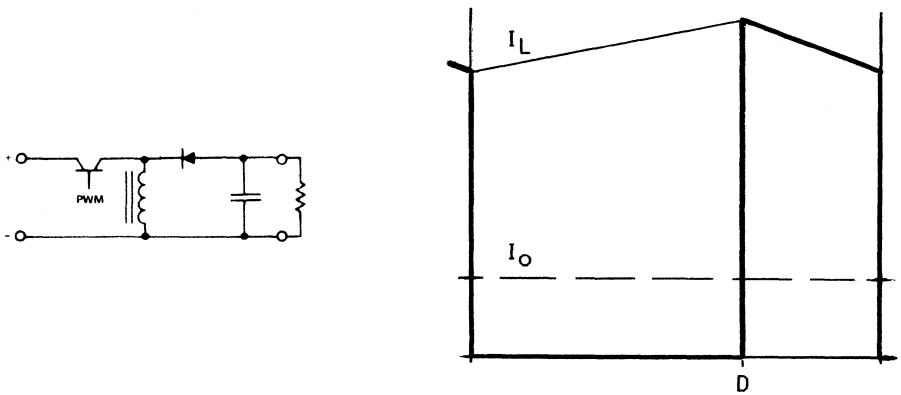


Figure 1 -- Flyback Circuit, Continuous Inductor Current Mode

Figure 1 shows the basic flyback circuit operating in the continuous mode with its current waveforms. In flyback as well as boost circuits, the diode is the output element. All current to the output filter capacitor and load must flow through the diode, so the steady-state DC load current must equal the average diode current. As shown in the Fig. 1 waveforms, the inductor current equals the peak diode current, and it flows through the diode only during the "off" or free-wheeling portion of each cycle. The average diode current (and load current) therefore equals the average inductor current, I_L, times (1-D), where D is the duty ratio (often called duty cycle).

If D is modulated by a small AC signal, $\hat{d}$, whose frequency is much smaller than the switching frequency, this will cause small changes in D from one switching cycle to the next. Figure 2 shows the effects of a small increase in duty ratio (during the positive half-cycle of the applied signal).

The first effect is that the temporarily larger duty ratio causes the peak inductor current to increase each switching cycle, with an accompanying increase in the average inductor current. If the signal frequency is quite low, the positive deviation in duty ratio will be present for many switching cycles. This results in a large cumulative increase in inductor current, whose phase lags $\hat{d}$ by 90°. This change in inductor current flows through the diode during the "off" time causing a proportional change in output current, in phase with the inductor current.

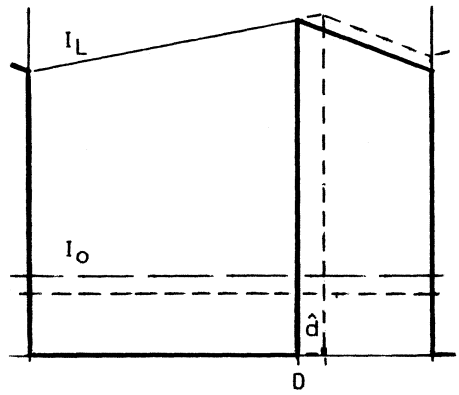


Figure 2.

The second effect is more startling: The temporary increase in duty ratio during the positive half-cycle of the signal causes the diode conduction time to correspondingly *decrease*. This means that if the inductor current stays relatively constant, the average diode current (which drives the output) actually decreases when the duty ratio increases. This can be clearly seen in Figure 2. In other words, the output current is 180° out of phase with $\hat{d}$. This is the circuit effect which is mathematically the right-half-plane zero. It dominates when the signal frequency is relatively high so that the inductor current cannot change significantly.

Duty Ratio Control Equations: The equations for the flyback circuit are developed starting with the voltage V_L across the inductor, averaged over the switching period:

$$V_L = V_i D - V_o(1-D) \quad = (V_i+V_o)D - V_o \tag{1}$$

Modulating the duty ratio D by a small AC signal $\hat{d}$ whose frequency is much smaller than the switching frequency generates an AC inductor voltage, $\hat{v}_L$:

$$\hat{v}_L = (V_i+V_o)\hat{d} + \hat{v}_o(1-D) \quad \simeq (V_i+V_o)\hat{d} \tag{2}$$

Assuming V_i is constant, $\hat{v}_L$ is a function of $\hat{d}$ and of $\hat{v}_o$, the AC voltage across the output filter capacitor. At frequencies above filter resonance, $\hat{v}_o$ becomes much smaller than $\hat{v}_L$, and the second term may be omitted.

AC inductor current, $\hat{i}_L$, varies inversely with frequency and lags $\hat{v}_L$ by 90°. Substituting Eq. 2 for $\hat{v}_L$ gives $\hat{i}_L$ in terms of $\hat{d}$:

$$\hat{i}_L = \frac{\hat{v}_L}{j\omega L} = -j\frac{(V_i+V_o)}{\omega L}\hat{d} \tag{3}$$

Referring to Figure 1, the inductor provides current to the output through the diode only during the "off" portion of each cycle:

$$I_o = I_L(1-D) \tag{4}$$

Differentiating Eq. 4, the AC output current, $\hat{i}_o$, has two components (ref. Fig. 2 discussion) -- one component in phase with $\hat{i}_L$ and the other 180° out of phase with $\hat{d}$:

$$\hat{i}_o = \hat{i}_L(1-D) - I_L\hat{d} \tag{5}$$

Substituting Eq. 3 for $\hat{i}_L$ gives $\hat{i}_o$ in terms of the control variable $\hat{d}$. In a continuous mode flyback circuit, $(1-D) = V_i/(V_i+V_o)$:

$$\hat{i}_o = -j\frac{(V_i+V_o)(1-D)}{\omega L}\hat{d} - I_L\hat{d} = -j\frac{V_i}{\omega L}\hat{d} - I_L\hat{d} \tag{6}$$

The first term is the inductor pole, which dominates at low frequency. Its magnitude decreases with frequency and the phase lag is 90°. At a certain frequency the magnitudes of the two terms are equal. Above this frequency, the second term dominates. Its magnitude is constant and the phase lag is 180°. This is the RHP zero occurring at frequency ω_z where the magnitudes are equal.

Figure 3 is a Bode plot of Eq. 6 (arbitrary scale values). Above f_z, the rising gain characteristic of the RHP zero cancels the falling gain of the inductor pole, but the 90° lag of the RHP zero *adds* to the inductor pole lag, for a total lag of 180°. The Bode plot of the entire power circuit would also include the output filter capacitor pole, which combines with the inductor pole resulting in a second order resonant characteristic at a frequency well below the RHP zero. The ESR of the filter capacitor also results in an additional conventional zero.

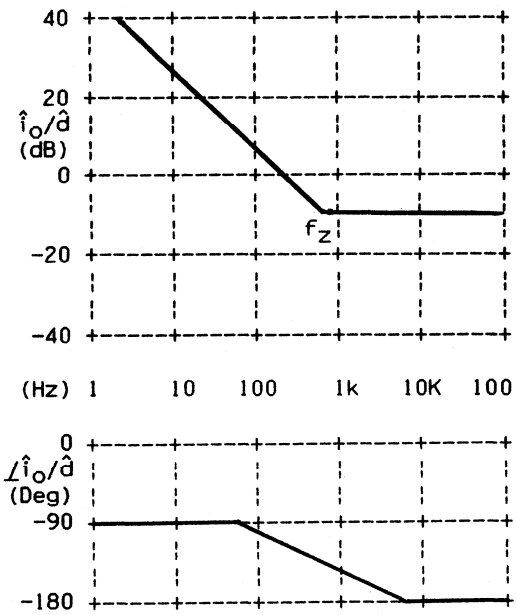


Figure 3

The RHP zero frequency is calculated by equating the magnitudes of the two terms in Eq. 6, and solving for ω_z:

$$\omega_z = \frac{V_i}{L\ I_L} \tag{7}$$

Substitute Eq. 4 for I_L, V_o/R_o for I_o.
In a flyback circuit, $V_i/V_o = (1-D)/D$; $(1-D) = V_i/(V_i+V_o)$:

$$\omega_z = \frac{R_o\ V_i(1-D)}{L\ V_o} = \frac{R_o\ (1-D)^2}{L\ \ D} = \frac{R_o\ \ V_i^2}{L\ V_o(V_i+V_o)} \tag{8}$$

Current Mode Control Equations: Equations 1, 2, 4, and 5 pertain to the flyback continuous mode power circuit, and are valid for any control method including current mode control. Eq. 3 is valid for current mode control, but it applies to the inner, current control loop. Solve Eq. 3 for $\hat{d}$ in terms of $\hat{i}_L$ and substitute for $\hat{d}$ in Eq 5:

$$\hat{i}_o = \hat{i}_L(1-D) - j\frac{\omega L\, I_L}{(V_i+V_o)}\hat{i}_L = \frac{V_i}{(V_i+V_o)}\hat{i}_L - j\frac{\omega L\, I_L}{(V_i+V_o)}\hat{i}_L \qquad (9)$$

Equations 6 and 9 are the same, except that in Eq. 6 the control variable is $\hat{d}$ for duty ratio control, while in Eq. 9 the control variable is $\hat{i}_L$ established by the inner loop and consistent with current mode control.

Unlike Eq. 6 for duty ratio control, the first term in Eq. 9 is constant with frequency and has no phase shift. This term dominates at low frequency. It represents the small signal inductor current which is maintained constant by the inner current control loop, thus eliminating the inductor pole. The second term *increases* with frequency yet the phase *lags* by 90°, characteristic of the RHP zero. It dominates at frequencies above ω_z where the magnitudes of the two terms are equal. The RHP zero frequency ω_z may be calculated by equating the two terms of Eq. 9. The result is the same as Eq. 7 for duty ratio control.

Figure 4 is the Bode plot of Eq. 9. The output filter capacitor will of course add a single pole and an ESR zero. Because the inductor pole is eliminated by the inner loop, the outer voltage control loop does *not* have a 2-pole resonant (second order) characteristic. However, the RHP zero is clearly still present with current mode control.

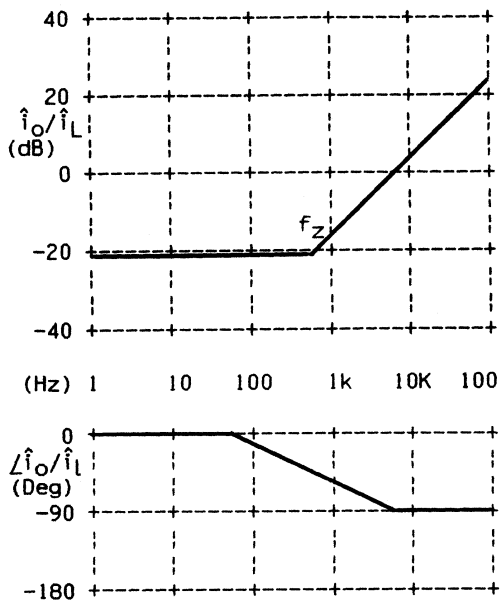


Figure 4

L.H.D. 10/84

CURRENT MODE CONTROL OF SWITCHING POWER SUPPLIES

Introduction: This paper examines the current mode control method applied to Buck, Boost and Flyback circuits operated in the continuous and discontinuous inductor current modes.

The current mode control method uses two control loops -- an inner, current control loop and an outer loop for voltage control. Figure 1 shows a forward converter (buck family) using current mode control. When the switching transistor is on, current through R_{sense} is proportional to the upward ramping filter inductor current. When the ramp voltage V_s reaches V_e (the amplified output voltage error), the switching transistor turns off. Thus, the outer voltage control loop defines the level at which the inner loop regulates peak current through the switch and through the filter inductor.[1]

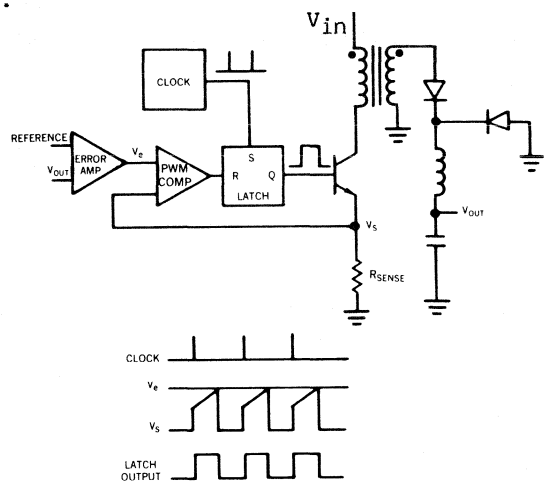


Figure 1.

ADVANTAGES:
- Input voltage feed-forward, resulting in good open-loop line regulation.
- Simplified loop -- inductor pole and 2nd order characteristic eliminated.
- Optimum large-signal behavior.
- No conditional loop stability problems.
- Flux balancing (symmetry correction) in push-pull circuits.
- Automatic pulse-by-pulse current limiting.
- Current sharing of paralleled supplies for modular power systems.
- Less complexity/cost (current sense/amp is *not* an added complication).

DISADVANTAGES AND PROBLEMS (continuous mode only):
- Peak/avg. current error and instability -- slope compensation.
- Noise immunity is worse because of shallower ramp.
- Half Bridge runaway
- DC open loop load regulation is worse.
- (1-D) current error in Boost or Flyback circuits.
- Loop irregularities with multiple output buck circuits.

THE BUCK REGULATOR (Continuous Inductor Current mode)

The buck family includes the Forward Converter, Full Wave Center-Tap, Full Bridge and Half Bridge.

Peak vs. Average Current Error: As shown in Figure 2, current mode control regulates the *peak* inductor current. However, in a buck regulator operated in the continuous mode, the inductor drives the output so that load current equals the *average* inductor current. The difference between peak and average inductor current is an error, which is greatest when V_{in} is large.

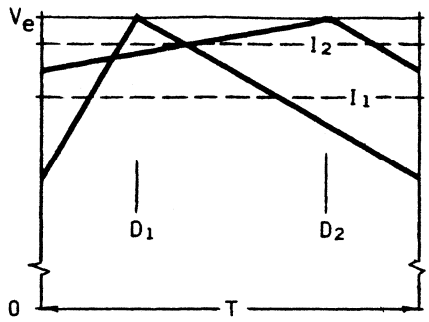


Figure 2. Current Error

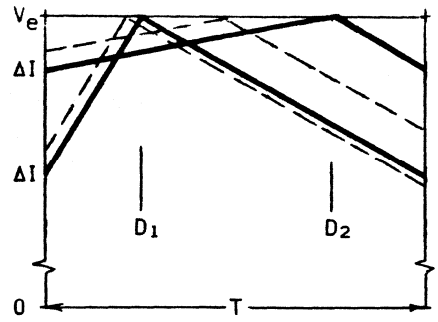


Figure 3. Instability

Instability: With continuous mode operation, controlling the peak inductor current results in circuit instability when the duty ratio, D, is greater than 0.5. Figure 3 shows how a small perturbation in the inductor current is magnified when D is greater than 0.5 (when V_{in} is low) because the downslope is greater than the upslope.

Slope Compensation: The correct amount of slope compensation eliminates both problems simultaneously. The *average* inductor current does not then change regardless of changes in V_{in} and D, and the circuit becomes stable at any duty ratio, as shown in Figure 4. However, in boost and flyback circuits, the large (1-D) error between average inductor current and output diode current is not improved through slope compensation.

Slope compensation is achieved as shown in Figs. 4 and 5 by summing a negative sawtooth ramp voltage with the amplified error voltage, V_e, at the control input of the comparator (Ref. Fig. 1). For perfect compensation, the compensation ramp must have a slope equal to exactly 1/2 the downslope of the voltage waveform at the other comparator input, which is the voltage analog of the inductor current downslope as seen across the current sense resistor.

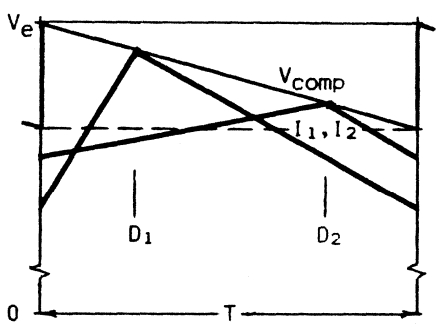


Figure 4. Slope Compensation

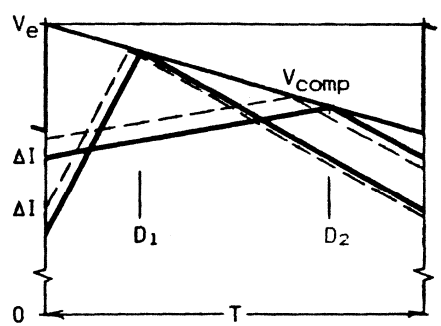


Figure 5. Slope Compensation

A negative ramp is not usually available within the control IC, but a positive going ramp is available from the IC's clock pulse generator. As shown in Figure 6, it is possible to use this *positive* ramp for slope compensation by applying it through a voltage divider to the *opposite* comparator input, summing it with the voltage analog of the inductor current from the current sense resistor. The voltage divider should set the slope of this positive ramp to be the same magnitude -- 1/2 the downslope of the voltage waveform representing the inductor current.

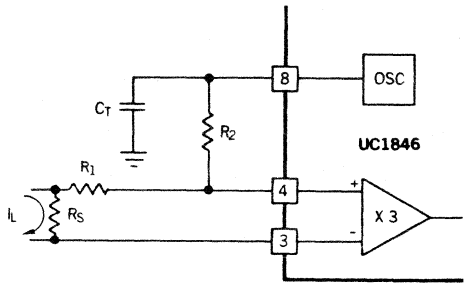


Figure 6. Compensation Circuit

Line Regulation: Current mode control has an inherent input voltage feed-forward characteristic which means the open loop D.C and dynamic line regulation is excellent. This reduces the closed loop gain needed in the outer voltage control loop. The good line regulation is caused by the inner current control loop which maintains constant peak inductor current regardless of changes in V_{in}. With slope compensation, this results in constant *average* inductor current. V_{in} changes of any kind -- large signal step changes, spikes, A.C. signals or noise riding on the line are rejected, even with the outer voltage control loop open.

Load Regulation: With voltage mode (duty ratio) control, open loop DC load regulation is inherently excellent, although dynamic load regulation is very bad. With current mode control, and with the outer voltage control loop open, the load regulation is very poor. This because the inner current control loop makes the circuit into a current source. Any current source has poor load regulation. This is not nearly as bad as it seems, because it is so much easier to get high closed loop gain-bandwidth which corrects the problem and gives many other performance advantages.

Paralleling Outputs: With current mode control, it is easy to parallel several supplies for the sake of redundancy or for modular power supply systems. If all the supplies to be paralleled have identical current sense resistors and identical current control loops, a single control voltage common to all supplies will cause them to deliver identical currents. Their outputs may then be paralleled to drive a common load, and they will share this common load current equally. A single voltage reference and error amplifier is used, and this amplified error voltage is the control voltage used to program the current in all the paralleled supplies.

Flux Balancing in Push-Pull Circuits: In any transformer coupled push-pull circuit, small differences in V_{sat} and/or storage time between the switching transistors cause a slight asymmetry in the voltage waveform, resulting in a net small DC voltage across the transformer primary. This DC voltage causes the magnetizing current and core flux to slowly move in one direction until finally, the transformer saturates. The magnetizing current flowing through the DC resistance of the primary circuit causes IR drops that are in a direction to correct this problem, but the resistance is usually nowhere near large enough. This has been a severe problem in push-pull circuits.

Current mode control automatically solves the unbalanced flux problem, by sensing and controlling the emitter currents of the switching transistors. These transistor currents represent the inductor current reflected from the secondary, *plus the transformer magnetizing current*. When the magnetizing current drifts off in one direction, it adds to the inductor current in one transistor and subtracts from it in the other transistor, making the push-pull current pulses unequal in amplitude. With duty ratio control, current pulse inequality will get worse and worse until the transformer saturates. However, with current mode control this cannot happen because the controller terminates each pulse when the same specific current is reached. Thus the pulses must always have the same amplitude, although the pulse widths will be slightly different. This pulse width differential that is created effectively corrects for the original asymmetry.

Runaway in Half-Bridge Circuits: As noted above, when current mode control is applied to any push-pull circuit, small differences in the alternate pulse widths will be created in order to correct any volt-second asymmetry applied to the transformer. Unfortunately, this *causes asymmetry in the current waveforms* drawn through each transistor -- the peak currents are maintained identical, therefore different pulse widths result in small differences in ampere-seconds, or charge, drawn alternately through the switching transistors.

In the half-bridge, one side of the transformer primary is connected to the midpoint of a capacitive voltage divider. When the charge flowing in alternate directions is slightly different because the alternate pulse widths are not the same, the capacitor divider voltage will drift in one direction. The direction is unfortunately such that it tends to reinforce the original volt-second asymmetry. This causes the current mode controller to further correct the volt-second asymmetry, making the charge unbalance worse. Thus, the capacitive divider voltage will run away until it reaches one or the other source voltage extreme.

This small charge imbalance is of no consequence in full bridge or full-wave center-tap circuits which do not involve a "soft" source such as the capacitive divider in the half bridge.

Noise Immunity: In continuous inductor current mode circuits, current mode control suffers from poorer noise immunity than duty ratio control. Both methods acheive control by comparing the amplified output voltage error to a ramp voltage. Referring to Figure 2, with current mode control the ramp represents inductor current. It sits on a pedestal and is quite shallow, especially when V_i is low, making D large. The ramp voltage is never far away from the control voltage, V_e. A relatively small noise spike will cause the current pulse to terminate prematurely. This problem is solved by: using care in circuit layout and proper location of ground returns to avoid pulses generated by

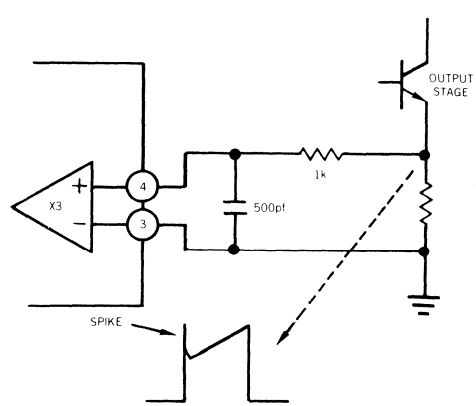


Figure 7.

fast switched high currents through wiring inductance, using differential input current sense amplifiers, using a small filter inductor (consistent with keeping out of the discontinuous mode at minimum load current), and by filtering out any remaining noise spikes with a simple RC filter at the input of the current sense amplifier as shown in Figure 7.

Small-Signal Loop Compensation: When current mode control is used with a continuous mode buck regulator, the inner (current control) loop includes the filter inductor. This eliminates the inductor from the small signal model of the outer (voltage control) loop. The voltage control loop then has only the single pole of the output filter capacitor and load resistance, as shown in Figure 9. Because the 90° phase lag of a single pole is inherently stable without additional compensation, it is easy to get high loop gain and excellent small signal dynamic performance.

With conventional duty ratio control applied to the buck regulator, the LC power filter has a two-pole second order charactistic as shown in Figure 8. There is an abrupt 180° phase lag at filter resonance (often near 100 Hz). This will cause ringing and instability if not compensated. At least one and usually two zeros near filter resonance must be provided in the error amplifier compensation network. This requires much more error amplifier gain-bandwidth than with current mode control and requires large compensation capacitors with time constants in the order of milliseconds.

When properly compensated (although with much greater difficulty), the small signal dynamic behavior of the buck regulator with conventional duty ratio control may be nearly as good as with current mode control. With a 50 kHz switching frequency, small-signal response times in the order of 100 microseconds can be achieved with either control method.

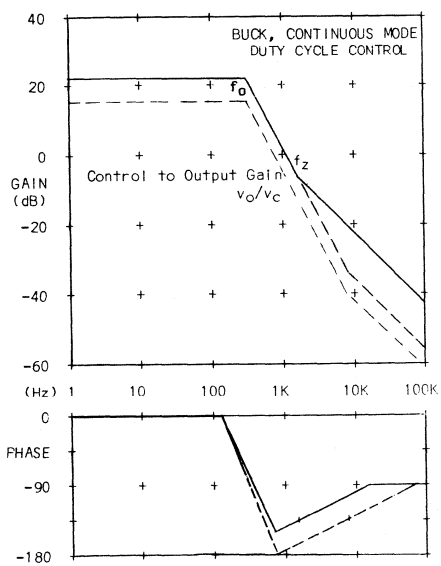


Figure 8.

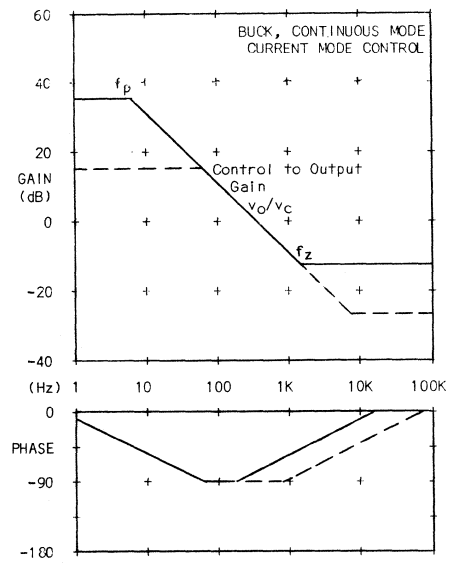


Figure 9.

Loop Gain Irregularities with Multiple Outputs: Figure 1 is a current mode controlled circuit of the buck family with one output. It is clear that the current which is sensed and controlled on the primary side is directly controlling the current through the single filter inductor to the output on the secondary side.

Additional outputs can be created by adding additional transformer secondaries, rectifiers, independent LC filters and loads. The current controlled on the primary side now suppies all of the outputs, which are effectively in parallel. Since the DC output of each LC filter must equal the average of the input voltage waveform (above the critical minimum load current), the DC voltages of the different outputs are absolutely related by their secondary turns ratios. The current supplied and controlled from the primary side will automatically apportion itself according to the demands of each load. Otherwise the voltages would diverge, which is not possible at DC and at frequencies below filter resonance. The DC and low frequency AC gain from the control input to the controlled output is proportional to the paralleled combination of all load resistances, adjusted by the square of the turns ratios.

At or above filter resonance, the story is different. With only one output, the single filter inductor is in series with the current source, causing the inductor to disappear. With multiple outputs, there are several LC filters being driven in parallel from one common current source. The inductors now do *not* disappear unless the resonant frequency *and the Q of each filter are exactly the same*, which would make the paralleled filters look like a single common unit. This is not likely, because the Q values are largely determined by load resistances which normally vary considerably.

Only one output is usually sensed and fed back to become part of the closed voltage control loop. The input of the LC filter of this controlled output is driven from the primary current source, but the LC filters of the other outputs attached in parallel to this same driving point. These other LC filters are really series resonant circuits which shunt the common driving point to ground. At the resonant frequency of each of these series resonant filters, they become a very low impedance, especially if its Q is high under lightly loaded conditions. The low shunt impedance at resonance chops a hole in the gain characteristic of the controlled output, with dramatic unexpected phase shifts. This problem is really severe if the controlled output is a lower power output and is shunted by a much higher power output, especially when the high power output is lightly loaded making its Q high.

The best solution to this problem is to couple the filter inductors together by winding them on a common core. The filters are no longer independent and do not have separate resonances. This also dramatically improves the dynamic cross regulation, which is very poor with independent filters.

Large Signal Behavior: Unlike small-signal behavior, when large-signal conditions prevail, such as at startup or with large and rapid load changes, there is a dramatic difference in performance between the two control methods. The large filter inductance values inherent in continuous mode circuits make it impossible for the inductor current to follow rapid changes in load *regardless of the control method*. This limitation in the slew rate of inductor current causes the power supply output voltage to go out of regulation temporarily. The error amplifier is driven into the stops,

causing the voltage control loop to become temporarily open until after the inductor current reaches the new load current level.

Under small-signal conditions, error amplifier feedback keeps the inverting input at a DC level within a millivolt of the DC reference voltage applied to the inverting input. But while the inductor current is slew rate limited and the error amplifier is in the stops, the voltage at the inverting input is uncontrolled. Referring to Figure 10, during this large-signal transition the compensation capacitors required with the duty ratio method will charge to voltage levels totally unrelated to normal operation. After the inductor current reaches the new value of load current (in perhaps 100 microseconds) and the error amplifier starts to regulate again, the power supply output voltage will be regulated with a significant error offset (perhaps 6 volts instead of 5) because of the unusual compensation capacitor voltages. The time constants to discharge the capacitors and bring the power supply output voltage back to normal will be 2 to 5 milliseconds.

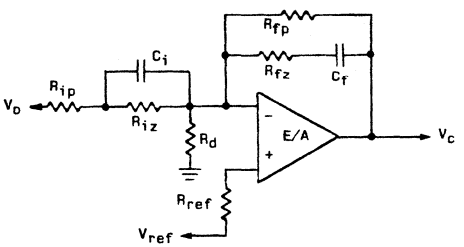


Figure 10.

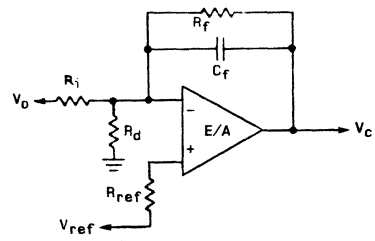


Figure 11.

In other words, the compensation capacitors necessary for good small-signal performance with duty ratio control cause poor large-signal performance -- large output glitches which take a long time to recover. In contrast to the above, current mode control achieves excellent small-signal performance without compensation capacitors other than one small capacitor which cancels the output capacitor's ESR zero. It recovers accurate regulation much more rapidly -- as soon as the inductor current reaches the new value of load current. The circuit of Figure 11 shows the simplicity of the current mode control error amplifier circuit. The single capacitor used is less than one tenth the value and time constant of the 2 capacitors necessary with duty ratio control.

Violation of Conditional Loop Stability: During large-signal episodes such as above, the time averaged loop gain is reduced. The crossover frequency is effectively lowered, which may cause a serious problem with simple duty cycle control if the control loop is undercompensated. If the loop is only conditionally stable (phase shift exceeding 180 degrees at frequencies well below crossover), the reduction in crossover frequency will initiate large-signal oscillation. The circuit will most likely remain in this oscillatory state until it is shut down and restarted. For this reason, conditional loop stability should be avoided in the design of switching power supplies. This is very easy to achieve with current mode control.

BOOST AND FLYBACK (Continuous Inductor Current Mode)

(1-D) Current Error: In boost or flyback continuous mode regulators, there is a large error between the average inductor current, I_L (regulated by the current control loop) and the load current, I_o. This is because I_L is provided to the output only during periods of diode conduction and *not* continuously as in the buck regulator. The load current I_o equals the average diode current I_D which equals I_L (1-D). For any continuous mode regulator, the duty ratio, D, is a direct function of V_{in}. Referring to Figure 12, if V_{in} changes, D must also change, and this changes the relationship between I_o and I_L. If V_{in} changes, I_L must then be changed to accomodate a constant load. In other words, the open loop line regulation is poor, unlike the buck regulator where I_L always equals I_o, making it independent of V_{in}.

The error between peak and average inductor current and the inherent instability of continuous mode circuits can both be eliminated by using slope compensation, just as with the buck regulator. The (1-D) error between I_L and I_o cannot be eliminated dynamically (this is what causes the right-half-plane zero), but the low frequency (1-D) error can be eliminated by appropriate feed-forward of V_{in} into the current control loop.

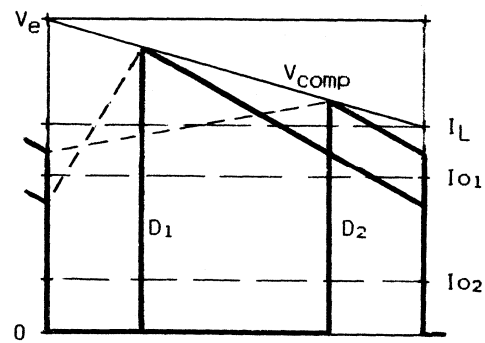


Figure 12.

Right-Half-Plane Zero: Current mode control does *not* eliminate the right half-plane zero inherent in boost and flyback continuous mode circuits, although it does eliminate the inductor pole and the 2nd order resonant filter characteristic. The RHP zero gives a 20 dB/decade gain boost with a 90° phase *lag*, which is considered impossible to compensate, and usually forces the designer to roll the loop gain off a decade or more below what could otherwise be achieved. Current mode control does not help in this respect. Refer to the separate paper titled "The Right-Half-Plane Zero -- a Simplified Explanation"

DISCONTINUOUS INDUCTOR CURRENT MODE

In the discontinuous inductor current mode, the inductor current by definition is at zero during part of each switching cycle, as shown in Figure 13. There are therefore three states during each cycle, rather than two as in the continuous mode. Most of the relevant problems encountered with continuous mode operation are not present in the discontinuous. Likewise, many of the advantages of current mode control in continuous mode operation are irrelevant in the discontinuous mode.

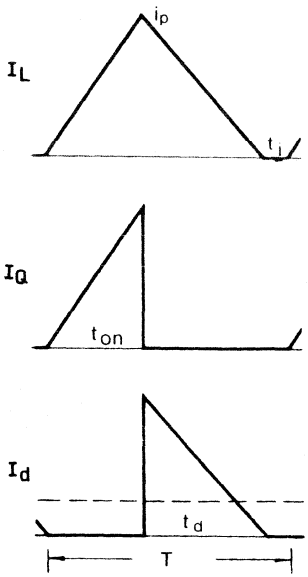


Figure 13.

Current mode control does have one important advantage as applied to the discontinuous mode -- good line regulation by virtue of the inherent feed-forward capability. It shares this advantage with feed-forward ICs such as the UC3840. The choice would be mainly on the cost of the IC vs. its functionality. Voltage feed-forward and current mode control are both much better than simple duty ratio control.

In the discontinuous mode, all of the energy stored in the inductor is delivered to the load each cycle. Power output equals the energy stored in the inductor each cycle times the frequency. This inductor energy (and the power delivered to the load) is established by the peak inductor current at the time the transistor switch is turned off. With fixed V_{in}, current mode control and duty ratio control methods both determine the peak inductor current -- one directly, the other indirectly. With current mode control, the peak current value and the the power output do not change when V_{in} changes. With simple duty ratio control, the peak current varies proportional to V_{in}, therefore the open loop line regulation is inherently poor. With voltage feedforward, such as in the UC3840, the open loop line regulation is good because the duty cycle is automatically changed in inverse proportion to V_{in}. This results in constant peak inductor current and power output regardless of V_{in} changes.

REFERENCES:

(1) B. Holland, "A New Integrated Circuit for Current Mode Control," Powercon 10 Proceedings, B-2, 1983.

(2) B. Holland, "Modelling, Analysis and Compensation of the Current-Mode Controller," Powercon 11 Proceedings, I-2, 1984.

(3) Shi-Ping Hsu, A. Brown, L. Rensink, R. Middlebrook, "Modelling and Analysis of Switching DC to DC Converters in Constant Frequency Current Programmed Mode," PESC '79 Record, pp 284-301.

SIMULATION OF SWITCHING POWER SUPPLY PERFORMANCE USING THE PERSONAL COMPUTER

Lloyd H. Dixon, Jr.

The ubiquitous personal computer is capable of simulating switching power supply performance using simple programs written in BASIC interpreter language. Performing integration by parts, the computer calculates small changes in current and voltage in each circuit element, working its way through the entire circuit and iterating around this loop many times in a single switching cycle. The only mathematics required is simple algebra. Complex equivalent circuit models are completely avoided. The actual circuit is exercised in the computer just as it would be on the lab bench. Successful simulation depends only on how faithfully the computer version of the circuit conforms to the actual power supply circuit.

Benefits and Limitations:

This technique provides a method of "software breadboarding" for checking out the design of any switching power supply. Not an artificially derived model, the computer program simulates operation of the actual circuit. Small signal loop stability and large signal behavior are observed. The circuit can be exercised almost effortlessly by the computer under a wide range of conditions, including startup and overload. Using an interpreter language permits the program to be interrupted and any values may be changed before continuing program execution. This is useful in simulating step changes in load current or line voltage.

This method is not intended to supplant a strong initial design effort, but to provide a fast and accurate method to check out and optimize the design. It provides excellent visibility into unforseen problems and facilitates a more knowledgable approach to solving these problems much more easily than in the lab. As a debugging tool, it is a simple matter to change the displayed variables or add new ones, then rerun the program to more clearly define the problem and its solution. Behavior under operating condition extremes is easily checked out.

Neither is this method a substitute for final lab checkout, although it does minimize the need for hardware debugging. When the computer simulation checks out with the design expectation and the final lab tests confirm it, there is a high probability of success.

The very act of writing the few BASIC program lines for the circuit being evaluated provides much insight into its operation. The implied question "Do I have the circuit correctly captured in the program?" often uncovers problems that were initially overlooked.

On the IBM PC, the running time for 1 cycle at the switching frequency is typically 4 seconds. Depending on the topology and L-C filter values of the specific application, it may take 1/2 to 5 minutes to run from startup until equilibrium operation is reached. The running time is just about right to permit the designer to comfortably observe its progress, noting whether it

conforms to expectations and attempting to understand why any deviations occur. Execution continues indefinitely until it is stopped by keyboard interrruption (CTRL-BREAK on the PC).

The simulation program as presented makes 20 to 50 iterations per switching period and provides an accurate representation of circuit behavior at or below the switching frequency. It is obviously incapable of dealing with higher frequency phenomena such as noise spikes and leakage inductance effects, although these could conceivably be handled by smaller iteration intervals and increased circuit/program complexity which would greatly slow down execution time.

The continuous mode buck regulator with simple duty cycle control used as the program example herein can serve as the basis for any other power supply circuit by changing a few program lines.

Program Features:

A brief overview of the program listing printed at the end of this paper:

Lines 1000-1280 set up miscellaneous definitions including title strings and a menu providing the choices of viewing the program conditions, running the program, and directing output to the printer. Except for the title in line 1000, these lines need not be changed for different applications.

Line 2010 defines the data column headings that are displayed at the top of each page. Lines 2020-2060 display the initial RUNtime title and data column headings. Lines 2080-2250 are subroutines which output the desired data, in this case twice during each switching period -- when the power switch turns on and when it turns off.

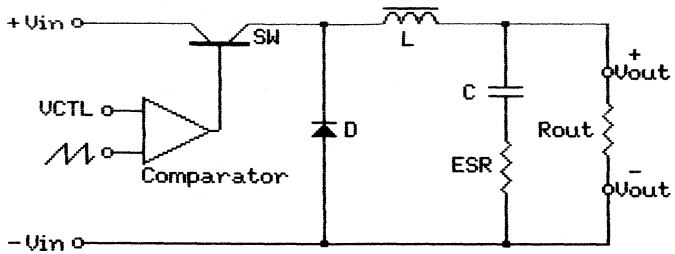
Lines 2260-2400 define circuit parameter variable names and initial values in a set of READ and DATA statements. Any of these values may be changed before running the program by editing the DATA lines. If the program is then SAVEd, the changed values will become the initial values the next time the program is loaded. When the menu choice is made to display operating conditions, lines 1240 and 1250 accomplish this by LISTing lines 2260-2400. Thus it is not necessary to duplicate variable names for displaying the operating conditions, making it easier to change these variable names for different applications. When it is desired to change a parameter value, this technique facilitates the process by showing the actual lines to be edited along with their line numbers.

Lines 2410-2500 define other initial values. Load resistance, ROUT, is calculated from the specified output voltage/current, VO/IO. Counters and other conditions are also set up. Note line 2490 defining resistor RD which divides the 5 volt output down to the 2 volt reference level, VNI (see Fig. 2). RD has no effect on the loop gain. RD is defined in this way so that it will be adjusted automatically to maintain the desired output voltage if RIP or RIZ are changed before running the program. RD could be defined in the parameter listings, instead.

The heart of the program is the computation section, lines 3000-3440. This section is most uniquely related to the specific circuit, yet perhaps half of the lines could be used without change in most applications.

Throughout this program, frequency is expressed in MHz, time in µs, inductance in µH, and capacitance in µF, in order to avoid the repeated use of 10^{-6}, thus simplifying the equations.

The Power Switching Circuit -- Figure 1:



The power switching circuit and filter are shown in Figure 1. Component values are listed at the beginning of the sample run at the end of this section. For the values given, the L-C filter resonance is at 2770 Hz, contributing a 2-pole second order characteristic above that frequency. One of these poles is compensated by the tantalum capacitor's ESR zero which occurs above 21,200 Hz. The gain from the pulse width modulator control terminal to the output of the supply at low frequencies is 8.15, or 18.2 dB. The control to output gain is .118, or -18.5 dB at 25 kHz, which is the intended crossover frequency (1/4 the switching frequency).

The program branches to line 3040 on the first iteration of each switching cycle. Cycle counter CCNT is incremented, iteration interval TI is initally set to 1/100 of the switching period, and cumulative interval TC is zeroed. The SWITCH is set "on" and VIN1, the voltage at the input of the filter, is set equal to VIN. A forward converter or push-pull version of the buck regulator with transformer coupling would have the identical circuit and equations except VIN1 above would be set equal to VIN/N - VD (Primary side Vin divided by turns ratio minus rectifier drop). On successive iterations, the program will branch to line 3130 until it is time for the switch to turn off.

When the comparator output changes state to turn the switch off, the program branches to line 3090, VIN1 is set to -VD (the circuit free-wheels through the rectifier), and the iteration interval is made exactly 1/10 of the time remaining to the end of the switching period. Thus there will be exactly 10 iterations during the "off" time which helps reduce the running time. Except for initial turn on and turn off, the program jumps to line 3130 at the beginning of each iteration.

The cumulative time interval TC within the current period is updated by line 3130. Line 3140 updates the filter inductor current. The new IL value equals the old IL plus ΔIL, which is VL*ΔT/L. The voltage across the inductor is (VIN1-VOUT), and ΔT is the iteration interval, TI. VIN1 equals VIN during the "on" time, and equals -VD, the freewheeling diode drop, during the "off" time. To greatly simplify the calculation, an important assumption is made: that VOUT, at the inductor output, is constant during each iteration. This assumption may not be valid in an abstract theoretical sense, but in a practical power supply it is certainly acceptable. The VOUT

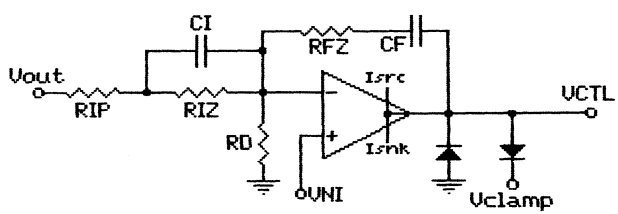
variation over the entire switching period (the output ripple voltage) is typically only 1-2%, so it will change less than 0.1% during the iteration interval. Any small error that occurs will not cumulatively increase, but self-corrects during the next iteration.

The second statement in line 3140 is used when the inductor current becomes discontinuous, i.e. the current is zero during a portion of each switching period. This occurs whenever load current drops below the critical inductor current level. In the actual circuit, the rectifier prevents the current from going negative. In the program, the second part of 3140 performs the same function.

Line 3150 computes IC from the new IL and old VOUT values, 3160 computes the new VC, and 3170 calculates the new VOUT value based on the new VC and new IL values (changes in VC and VOUT are *very* small for each iteration).

Line 3180 finds the minimum and maximum values of VOUT which define the peak-to-peak ripple. This may occur at any time during the switching cycle, not necessarily at switch on and switch off. The determination is made by looking for a change in sign of the ΔVOUT between the present and the previous iteration. The subroutine at line 2180 prints these min/max VOUT values to the right of the normal data columns, including the time within the cycle that they occur.

The Error Amplifier/Compensation Network -- Figure 2:



This remaining portion of the power supply using a UC3524 control IC is shown in Figure 2. A low frequency pole provides high DC gain. Two zeros come in at 2770 Hz to compensate the two filter resonance poles. A single pole compensates the ESR zero keeping the overall loop gain trending ever downward with a net single pole characteristic to well above the crossover frequency. The gain of the error amplifier with its compensation network is +18.5 dB at 25 kHz and above, so that the overall loop gain including the power circuit is 0 dB at 25 kHz, the crossover frequency. The error amplifier gain is also +18.5 dB at the 100 kHz switching frequency. This amplifies the 0.1 volt ripple component of VOUT to 0.85 volts at the output of the error amplifier. It is then applied to the control terminal of the modulator and compared against the sawtooth ramp whose amplitude is 2.7 volts. If the amplified ripple exceeds the sawtooth amplitude (which would happen with a higher crossover frequency), the circuit becomes unstable. In this case, the loop gain has been pushed about as high as it should, and the circuit response is excellent as shown by the demonstration run.

The computer iterates its way through the error amplifier circuit in lines 3220-3280. A simplifying assumption is made that the circuit gain-bandwidth envelope is determined completely by the external components, i.e. the small signal gain-bandwidth of the error amplifier is so high it is negligible. This is indeed what should be expected, otherwise the poles and zeros of the compensation circuit cannot function as intended. Always compare the Bode plot of the overall compensation circuit against the error amplifier alone to make certain it it up to the task. So the error amplifier is assumed to be ideal except for its large signal limitations which will be discussed shortly.

Lines 3220 and 3230 presume the error amplifier is functioning normally, in which case the voltage at the inverting input is essentially equal (within a fraction of a millivolt) to the 2 V reference voltage on the non-inverting input, VNI. Using the old values of VCI and VCF, the input and feedback currents II and IFB are calculated, and error amplifier output voltage VCTL (which is applied to the control terminal of the modulator) is calculated in line 3240.

Before proceeding to update the capacitor voltages VCI and VCF, lines 3250 and 3260 check whether VCTL has violated the E/A output clamp voltages or whether IFB has exceeded the E/A output current source or sink capability. If so, the program jumps to the subroutines at 3350 and/or 3400. The assumption of normal operation is abandoned, and the output is constrained by either the voltage clamp or current limits. The error amplifier gain is temporarily zero in this condition and the non-inverting input voltage is not maintained equal to VNI. II and IFB are recalculated based on the appropriate situation in lines 3360-3370 or 3410-3420. This is done so that even during "abnormal" circuit operation the voltages on VCI and VNI will be correctly updated. These equations for recalculating II and IFB and VCTL were developed by algebraically combining several simpler sequential steps. There is no need to retain any intermediate values and this speeds up program execution. VCI and VCF are updated in 3270 and 3280 based on the final current values.

If the power switch is off, 3290 looks for the end of the switching period and when it occurs, causes the data to be viewed/printed and then branches to 3040, the beginning of the next cycle.

If the switch is on, 3300 checks the comparator input and the current limit to determine whether to turn the switch off. If so, data is viewed/printed and the program branches to 3090, the beginning of the "off" period. If the switch is on and the end of the "on" period has not yet been reached, 3310 makes an estimate on how close it is to turn-off and adjusts the iteration interval accordingly. The interval needs to be small as the end of the "on" time approaches in order to terminate the "on" time with adequate precision. If the program always used this small increment it would run very slowly. So line 3310 speeds up execution time considerably.

Techniques to Improve Speed and Accuracy:

In execution time of the BASIC interpreter program in this application depends, in order of importance, on:

1. Each variable must be looked up each time it is encountered (even in the same equation) in the variables table maintained by BASIC. The look-up time depends on how many variables are in the entire program, which determines the length of the table. It is worth the effort to minimize the number of variables encountered in the iteration loops.

2. Of next importance is the time BASIC spends interpreting each statement. This can be minimized by combining statements algebraicly, omitting intermediate variables. It is only necessary to update and save (as a named variable) capacitor voltages, inductor currents, and those values which may be viewed/printed as data. All other values can be eliminated if possible by combining equations. This also minimizes variable look-up time as above.

3. Computation time is the least important in this application because the calculations are so simple: +,-,/,and *.

With one exception, the iteration interval can be quite large -- 1/10 to 1/20 of the switching period -- without impairing accuracy. This means 10 or 20 iterations per cycle which will run at a good speed. Try running the same program with the iteration interval changed. If the results are close to each other use the larger increment which will run faster. However, using a long interval throughout results in insufficient accuracy in defining the length of the "on" time, which must always terminate at an interval boundary. If the duty ratio is supposed to be .31, but there are only 10 iterations per cycle, the switch will turn off at .4, which is a great deal of overshoot. An interval of 1/100 is more appropriate when approaching the turn-off point, but is too slow for general use. The only solution is to use some method of estimating proximity to turn-off and using a fine increment when it gets close. This is probably the biggest source of error in using this simulation method.

Unlike the buck regulator, flyback equivalent circuits are very different in the "on" state compared to the "off" state. In writing a single program section to cover both states, there will be several lines that apply to one state and not the other, and several IF....THEN statements to direct program execution to the proper lines. All this slows up program execution, and makes writing the program more difficult. In such cases, it is better to use two completely separate program segments, one for each state. Switching to the proper segment is done no more than once per iteration. This will slightly increase the total program length, but it will run faster.

```
1000 T2$="BUCKDC1 -- Buck, Continuous, Duty Cycle Control"
1010 T1$="SWITCHING POWER SUPPLY PERFORMANCE SIMULATION          "
1020 '    L. H. Dixon      UNITRODE  CORP.              1/15/85
1030 '
1040 'System definitions:
1050 PLEN=66:TLEN=24:'          Printer, Terminal #lines/pg
1060 LF$=CHR$(13)+CHR$(10):'    1 line feed
1070 LF2$=LF$+LF$:'             2   "   "
1080 FF$=CHR$(12):'             Form Feed
1090 TITL$=T1$+DATE$+",  "+TIME$+LF2$+T2$+LF$
1100 '
1110 PRINT FF$+TITL$+LF$
1120 PRINT "    1    Display/change operating conditions
1130 PRINT "    2    Run simulation on terminal
1140 PRINT "    3    Print operating conditions
1150 PRINT "              (First make sure printer is at page top)
1160 PRINT "    4    Run simulation with printout
1170 PRINT
1180 PRINT"         CTRL/BREAK to terminate.
1190 PRINT LF2$
1200 PRINT "         Enter 1, 2, 3, or 4:  _"+CHR$(29);
1210 '
1220 S$=INKEY$:IF S$="" THEN 1220 ELSE PRINT S$
1230 '
1240 IF S$="1" THEN PRINT FF$+TITL$:LIST 2260-2400
1250 IF S$="3" THEN PRINT FF$+LF2$+"RUN again":LPRINT TITL$:LLIST 2260-2380
1260 '  STOP is inherent after execution of LIST statements in the above lines
1270 IF S$<>"2" AND S$<>"4" THEN 1200
1280 '
2000 '    Print column headings
2010 HDR$="Cycle   Time     IL      IC      Vout     "
2020 HDR$=HDR$+DATE$+",   "
2030 IF S$="4" THEN LPRINT LF$+TITL$ +HDR$+TIME$ ELSE PRINT FF$+TITL$
2040 PRINT LF$+HDR$+TIME$
2050 TCNT=0:PCNT=20:'   Init terminal, printer line count
2060 GOTO 2260
2070 '
2080 '    Display/print results
2090 PRINT:TCNT=TCNT+1:IF TCNT>=TLEN-2 THEN PRINT HDR$+TIME$:TCNT=0
2100 PRINT USING "####";CCNT;
2110 PRINT USING "#####.##";TC/T;IL;IC;VOUT;
2120 IF S$<>"4" THEN RETURN
2130 LPRINT:PCNT=PCNT+1:IF PCNT>PLEN-10 THEN LPRINT FF$+HDR$+TIME$+LF$:PCNT=0
2140 LPRINT USING "####";CCNT;
2150 LPRINT USING "#####.##";TC/T;IL;IC;VOUT;
2160 RETURN
2170 '
2180 '    Max/min values
2185 IF CCNT=1 THEN RETURN
2190 PRINT USING " ####.##";(TC-TI)/T;
2200 PRINT USING "####.##";M2;
2210 IF S$<>"4" THEN RETURN
2220 LPRINT USING " ####.##";(TC-TI)/T;
2230 LPRINT USING "####.##";M2;
2240 RETURN
2250 '
2260 '
2270 '    Power Circuit Parameters:
2280 READ   F,     VIN,   VO,    IO,    ILIM,  L,     C,     ESR
2290 DATA   0.1,   16,    5,     20,     25,   11,   300,    .025
2300 '
2310 '    Error Amplifier Values:
2320 READ   VNI,   RIP,   RIZ,   CI,    RFZ,   CF,    ISRC,  ISNK
2330 DATA   2.0,   4504,  30000, .0019, 36000, .0015, .0001, .0002
2340 '
```

```
2350 '    Modulator:
2360 READ   VSMIN, VSMAX, VCLAMP
2370 DATA   0.8,   3.5,   2.2
2380 '
2390 '    To change values, edit DATA statements above.  SAVE program (optional)
2400 '    Then RUN again.
2410 '
2420 '   Initial values
2430 T=1/F:'       Period
2440 TC=0:'        Cumulative interval (time within cycle)
2450 CCNT=0:'      Cycle count
2460 ROUT=VO/IO:'  Load resistance
2470 IF VNI=VO THEN RD=1E+10 ELSE RD=VNI*(RIP+RIZ)/(VO-VNI):'   Divider Resistor
2480 VS=VSMAX-VSMIN:'   Ramp amplitude
2490 VD=.6:'      Rectifier drop
2500 '
3000 '    COMPUTATION
3010 '
3020 '    Power Switch ON
3030 '
3040 CCNT=CCNT+1:TI=T/100:TC=0:SWITCH=1:'     Switch ON, Begin  new cycle
3050 VIN1=VIN:GOTO 3130
3060 '
3070 '     Power switch OFF
3080 '
3090 TI=(T-TC)/10:SWITCH=0:'            Switch OFF
3100 VIN1=-VD
3110 '
3120 '     Power switch and filter
3130 TC=TC+TI
3140 IL=IL+(VIN1-VOUT)*TI/L:IF IL<0 THEN IL=0
3150 IC=IL-VOUT/ROUT
3160 VC=VC +IC*TI/C
3170 VOUT=VC+IC*ESR
3180 M3=M2:M2=M1:M1=VOUT:IF SGN(M2-M3)<>SGN(M1-M2) THEN GOSUB 2180
3190 '
3200 'E/A Type 2
3210 '
3220 II=(VOUT-VNI-VCI)/RIP
3230 IFB= II - VNI/RD
3240 VCTL=VNI-VCF-IFB*RFZ
3250 IF VCTL>VCLAMP OR VCTL<0 THEN GOSUB 3350
3260 IF IFB>ISNK OR IFB<-ISRC THEN GOSUB 3400
3270 VCI=VCI+(II-VCI/RIZ)*TI/CI
3280 VCF=VCF+IFB*TI/CF
3290 IF SWITCH=0 THEN IF TC>.999*T THEN GOSUB 2090:GOTO 3040 ELSE GOTO 3130
3300 IF VCTL<=(VS*TC/T+VSMIN) OR IL>ILIM THEN GOSUB 2090:GOTO 3090
3310 IF VCTL-(VS*TC/T+VSMIN)<.2 OR IL>.9*ILIM THEN TI=T/100 ELSE TI=T/20
3320 GOTO 3130
3330 '
3340 '    Vctl clamped
3350 IF VCTL>VCLAMP THEN VCTL=VCLAMP ELSE VCTL=0
3360 IFB=((VOUT-VCI)*(1-RIP/(RD+RIP))-VCF-VCTL)/(RFZ+RD*RIP/(RD+RIP))
3370 II=(VOUT-VCI+IFB*RD)/(RD+RIP)
3380 RETURN
3390 '    Ifb too great
3400 IF IFB<-ISRC THEN IFB=-ISRC ELSE IFB=ISNK
3410 II=(VOUT-VCI+IFB*RD)/(RD+RIP)
3420 VCTL=VOUT-II*RIP-VCI-IFB*RFZ-VCF
3430 RETURN
3440 END
```

```
SWITCHING POWER SUPPLY PERFORMANCE SIMULATION          02-07-1985,

BUCKDC1 -- Buck, Continuous, Duty Cycle Control

2260 '
2270 '    Power Circuit Parameters:
2280 READ   F,     VIN,   VO,    IO,     ILIM,  L,     C,     ESR
2290 DATA   0.1,   16,    5,     20,     25,    11,    300,   .025
2300 '
2310 '    Error Amplifier Values:
2320 READ   VNI,   RIP,   RIZ,   CI,    RFZ,   CF,    ISRC,  ISNK
2330 DATA   2.0,   4504,  30000, .0019, 36000, .0015, .0001, .0002
2340 '
2350 '    Modulator:
2360 READ   VSMIN, VSMAX, VCLAMP
2370 DATA   0.8,   3.5,   2.2
2380 '
```

SWITCHING POWER SUPPLY PERFORMANCE SIMULATION 02-07-1985,

BUCKDC1 -- Buck, Continuous, Duty Cycle Control

Cycle	Time	IL	IC	Vout
1	0.52	7.52	6.62	0.23
1	1.00	7.14	5.92	0.31
2	0.52	14.49	12.01	0.63
2	1.00	13.92	10.86	0.78
3	0.52	21.04	16.42	1.16
3	1.00	20.23	14.82	1.37
4	0.37	25.10	18.46	1.67
4	1.00	23.72	15.97	1.97
5	0.11	25.12	16.95	2.05
5	1.00	22.84	13.34	2.41
6	0.18	25.06	14.96	2.53
6	1.00	22.62	11.50	2.80
7	0.20	25.01	13.31	2.93
7	1.00	22.37	9.84	3.15
8	0.23	25.04	11.92	3.29
8	1.00	22.26	8.49	3.46
9	0.25	25.10	10.74	3.59
9	1.00	22.19	7.31	3.73
10	0.26	25.08	9.65	3.86
10	1.00	22.04	6.20	3.97
11	0.28	25.09	8.70	4.10
11	1.00	21.98	5.28	4.18
12	0.29	25.08	7.87	4.31
12	1.00	21.89	4.45	4.36
13	0.30	25.05	7.11	4.49
13	1.00	21.80	3.70	4.53
14	0.31	25.02	6.44	4.65
14	1.00	21.72	3.04	4.67
15	0.30	24.79	5.69	4.78
15	1.00	21.37	2.23	4.78
16	0.28	24.21	4.72	4.88
16	1.00	20.63	1.19	4.85
17	0.29	23.56	3.79	4.95
17	1.00	19.99	0.34	4.90
18	0.30	23.00	3.05	4.99
18	1.00	19.46	-0.31	4.93
19	0.31	22.57	2.51	5.02
19	1.00	19.06	-0.79	4.95
20	0.31	22.16	2.09	5.03
20	1.00	18.65	-1.21	4.95
21	0.33	21.95	1.82	5.04
21	1.00	18.54	-1.34	4.96
22	0.34	21.94	1.78	5.04
22	1.00	18.57	-1.33	4.97
23	0.33	21.87	1.70	5.05
23	1.00	18.45	-1.46	4.97
24	0.34	21.85	1.67	5.05
24	1.00	18.48	-1.44	4.97
25	0.33	21.78	1.60	5.05
25	1.00	18.36	-1.55	4.97
26	0.34	21.76	1.58	5.05
26	1.00	18.39	-1.52	4.97

INT.- ROUT .25→1.0Ω

27	0.31	21.49	16.46	5.44
27	1.00	17.64	12.01	5.65
28	0.01	17.73	12.08	5.66
28	1.00	12.03	6.23	5.80
29	0.01	12.12	6.32	5.81
29	1.00	6.36	0.58	5.77
30	0.01	6.45	0.68	5.77
30	1.00	0.79	-4.79	5.56
31	0.08	1.55	-4.01	5.56
31	1.00	0.00	-5.38	5.37
32	0.18	1.74	-3.64	5.38
32	1.00	0.00	-5.22	5.21
33	0.24	2.35	-2.88	5.23
33	1.00	0.00	-5.08	5.06
34	0.29	2.88	-2.22	5.10
34	1.00	0.00	-4.95	4.94
35	0.35	3.51	-1.48	4.99
35	1.00	0.25	-4.61	4.84
36	0.38	4.09	-0.81	4.91
36	1.00	1.02	-3.78	4.78
37	0.39	4.98	0.13	4.86
37	1.00	1.98	-2.79	4.76
38	0.37	5.75	0.91	4.84
38	1.00	2.66	-2.10	4.75
39	0.36	6.33	1.49	4.84
39	1.00	3.18	-1.59	4.76
40	0.34	6.65	1.80	4.84
40	1.00	3.40	-1.38	4.77
41	0.34	6.86	2.00	4.86
41	1.00	3.60	-1.19	4.78
42	0.33	6.96	2.09	4.87
42	1.00	3.64	-1.17	4.80
43	0.33	6.99	2.11	4.89
43	1.00	3.67	-1.16	4.81
44	0.33	7.01	2.11	4.90
44	1.00	3.68	-1.16	4.83
45	0.33	7.02	2.11	4.92
45	1.00	3.68	-1.17	4.84
46	0.33	7.01	2.09	4.93
46	1.00	3.66	-1.20	4.85
47	0.33	7.00	2.06	4.94

Cycle	Time	IL	IC	Vout
47	1.00	3.64	-1.24	4.87
48	0.33	6.97	2.02	4.95
48	1.00	3.60	-1.28	4.88
49	0.33	6.93	1.97	4.96
49	1.00	3.56	-1.33	4.88
50	0.33	6.88	1.92	4.97
50	1.00	3.51	-1.39	4.89
51	0.33	6.83	1.86	4.98
51	1.00	3.45	-1.45	4.89
52	0.33	6.78	1.80	4.98
52	1.00	3.40	-1.51	4.90
53	0.34	6.82	1.84	4.98
53	1.00	3.49	-1.43	4.90
54	0.33	6.80	1.82	4.99
54	1.00	3.42	-1.50	4.91
55	0.34	6.84	1.84	4.99
55	1.00	3.50	-1.43	4.91
56	0.33	6.81	1.82	5.00
56	1.00	3.42	-1.51	4.92
INT.	VIN 16→11 V			
57	0.34	6.84	1.84	5.00
57	1.00	3.49	-1.44	4.92
58	0.41	5.75	0.78	4.98
58	1.00	2.78	-2.12	4.89
59	0.47	5.38	0.44	4.94
59	1.00	2.73	-2.14	4.86
60	0.50	5.51	0.60	4.92
60	1.00	3.02	-1.84	4.84
61	0.51	5.86	0.95	4.91
61	1.00	3.42	-1.43	4.84
62	0.49	6.15	1.24	4.91
62	1.00	3.61	-1.25	4.84
63	0.48	6.28	1.37	4.91
63	1.00	3.69	-1.17	4.85
64	0.48	6.36	1.44	4.92
64	1.00	3.76	-1.10	4.86
65	0.47	6.37	1.45	4.92
65	1.00	3.72	-1.14	4.86
66	0.48	6.39	1.46	4.93
66	1.00	3.79	-1.09	4.87
67	0.47	6.40	1.46	4.94
67	1.00	3.74	-1.14	4.87
68	0.48	6.40	1.46	4.94
68	1.00	3.80	-1.09	4.88
69	0.48	6.45	1.51	4.95
69	1.00	3.84	-1.05	4.89
70	0.47	6.44	1.49	4.96
70	1.00	3.78	-1.12	4.89
71	0.47	6.38	1.42	4.96
71	1.00	3.71	-1.19	4.89
72	0.48	6.36	1.40	4.96
72	1.00	3.74	-1.16	4.90
73	0.48	6.39	1.43	4.97
73	1.00	3.77	-1.14	4.90
74	0.47	6.37	1.40	4.97
INT.	ROUT 1.0→.25Ω			
74	1.00	3.73	-14.41	4.50
75	0.52	6.83	-10.70	4.38
75	1.00	4.70	-12.04	4.16
76	0.52	7.95	-8.38	4.08
76	1.00	5.95	-9.73	3.90
77	0.52	9.31	-6.12	3.86
77	1.00	7.40	-7.51	3.71
78	0.52	10.84	-3.97	3.70
78	1.00	8.99	-5.42	3.59
79	0.52	12.49	-1.98	3.62
79	1.00	10.66	-3.51	3.53
80	0.52	14.18	-0.16	3.59
80	1.00	12.37	-1.78	3.53
81	0.52	15.88	1.44	3.61
81	1.00	14.05	-0.27	3.58
82	0.52	17.54	2.83	3.68
82	1.00	15.67	1.01	3.66
83	0.52	19.12	3.99	3.78
83	1.00	17.20	2.07	3.78
84	0.52	20.59	4.93	3.92
84	1.00	18.61	2.90	3.93
85	0.52	21.93	5.64	4.07
85	1.00	19.88	3.52	4.09
86	0.52	23.12	6.15	4.24
86	1.00	21.00	3.93	4.27
87	0.52	24.14	6.47	4.42
87	1.00	21.95	4.16	4.45
88	0.52	25.01	6.61	4.60
88	1.00	22.73	4.22	4.63
89	0.40	25.03	6.07	4.74
89	1.00	22.11	3.07	4.76
90	0.39	24.31	4.89	4.86
90	1.00	21.28	1.88	4.85
91	0.39	23.45	3.74	4.93
91	1.00	20.39	0.77	4.90
92	0.41	22.65	2.76	4.97
92	1.00	19.67	-0.07	4.93
93	0.43	22.03	2.05	5.00
93	1.00	19.14	-0.65	4.94
94	0.45	21.61	1.60	5.00
94	1.00	18.82	-0.98	4.94
95	0.47	21.40	1.37	5.01
95	1.00	18.71	-1.11	4.95
96	0.48	21.34	1.30	5.01
96	1.00	18.70	-1.13	4.95
97	0.48	21.33	1.28	5.01
97	1.00	18.68	-1.15	4.95
98	0.48	21.31	1.26	5.01
98	1.00	18.67	-1.17	4.95
99	0.48	21.30	1.24	5.02
INT.	VIN 11→21 V			
99	1.00	18.66	-1.19	4.95
100	0.33	23.45	3.17	5.08
100	1.00	20.01	-0.12	5.02
101	0.26	23.77	3.29	5.13
101	1.00	19.94	-0.36	5.07
102	0.25	23.55	2.92	5.16
102	1.00	19.64	-0.76	5.09
103	0.24	23.10	2.40	5.18
103	1.00	19.13	-1.29	5.09
104	0.25	22.74	2.02	5.18
104	1.00	18.82	-1.60	5.09
105	0.25	22.43	1.73	5.18
105	1.00	18.51	-1.87	5.08
106	0.26	22.27	1.65	5.17
106	1.00	18.41	-1.93	5.07
107	0.26	22.17	1.59	5.16
107	1.00	18.32	-1.99	5.06
108	0.26	22.07	1.54	5.15
108	1.00	18.23	-2.02	5.05
109	0.26	21.99	1.51	5.14
109	1.00	18.16	-2.05	5.04
110	0.26	21.92	1.49	5.13
110	1.00	18.10	-2.06	5.03
111	0.26	21.87	1.48	5.11
111	1.00	18.05	-2.06	5.01
112	0.27	21.96	1.55	5.10
112	1.00	18.20	-1.89	5.01
113	0.26	21.97	1.65	5.10
113	1.00	18.16	-1.90	5.00
114	0.26	21.94	1.64	5.09
114	1.00	18.13	-1.90	5.00
115	0.26	21.91	1.64	5.09
115	1.00	18.11	-1.89	4.99
116	0.26	21.89	1.65	5.08
116	1.00	18.09	-1.89	4.98
117	0.26	21.87	1.66	5.07
117	1.00	18.08	-1.87	4.98
118	0.27	22.00	1.74	5.07
118	1.00	18.26	-1.70	4.98
119	0.26	22.04	1.84	5.07
119	1.00	18.25	-1.71	4.98
120	0.26	22.03	1.83	5.07
120	1.00	18.24	-1.71	4.98
121	0.26	22.02	1.82	5.07
121	1.00	18.23	-1.72	4.98
122	0.26	22.01	1.82	5.07

PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant $V_{OUT}\ L_{SEC}$.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current I1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

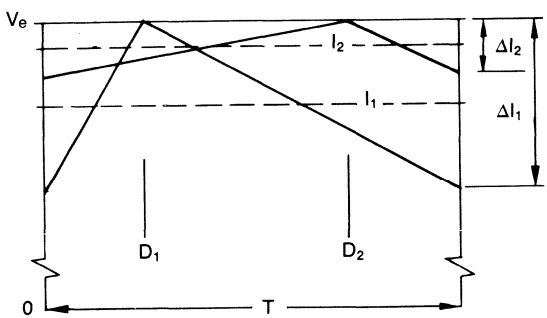


Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

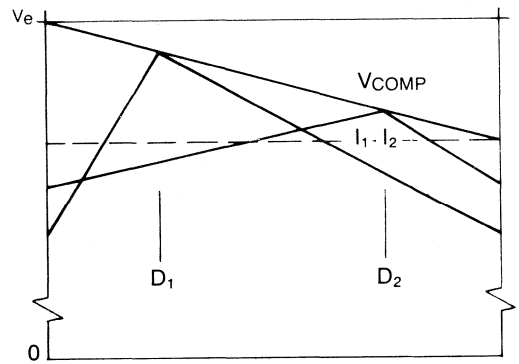


Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator
	ΔV Oscillator (PK-PK Ramp Amplitude)
	I Sense Threshold (Max)
Output	V Secondary (Min)
	L Output
	I AC Secondary
	(Secondary Ripple Current)
General	R Sense (Current Sensing Resistor)
	M (Amount of Slope Compensation)
	N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

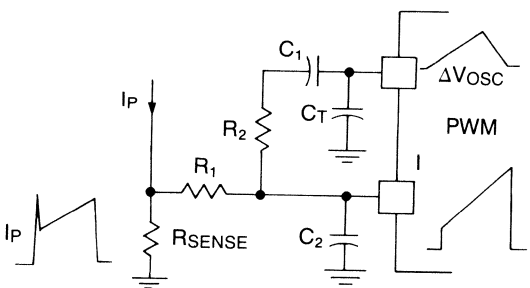


Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

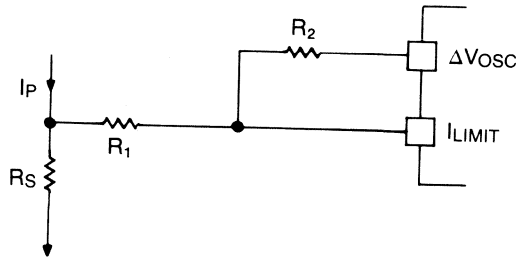


Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d\,(V_{OSC}) / T\ on$ (Volts/Second)

Step 5. Generate the Ramp Equations
Using superposition, the circuit can be illustrated as:

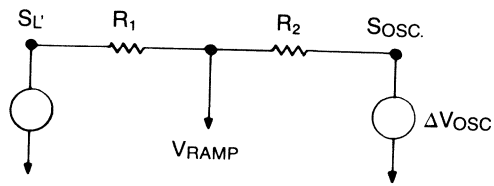


Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$ simplifying,

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)}$$ where

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}$$, and $$V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation
$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

Equating $$\frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of down-slope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

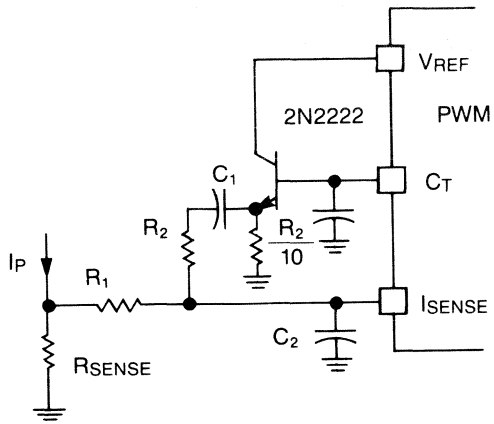


Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 μS
T Deadtime: 500 ns, T on Max = 4.5 μS
Turns Ratio: 15 / 1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<10% I DC)
L Output: 5.16 μh

1. Calculate the Inductor Downslope on the Secondary Side

S (L) = di/dt = V_{SEC}/L_{SEC} = 6 v/5.16 μh = 1.16 A/μs

2. Calculate the Transformed Inductor Slope to the Primary Side

S (L)' = S (L) • Ns/Np = 1.16 • 1/15 = 0.0775 A/μS

3. Calculate the Transformed Slope Voltage at Sense Resistor

V S(L)' = S (L)' • Rsense = 7.72 • 10^{-2} • 0.250 = 1.94•10^{-2} V/μS

4. Calculate the Oscillator Slope at the Timing Capacitor

$S_{(OSC)}$ = d V osc/T on max = 1.8/4.5 = 0.400 V/μS

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M} \quad ; R2 = \frac{1K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

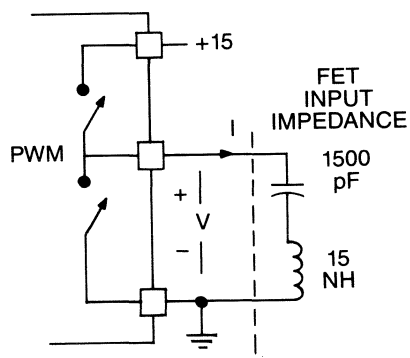


Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

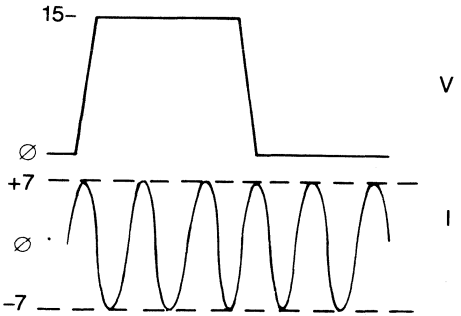


Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (V_C) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

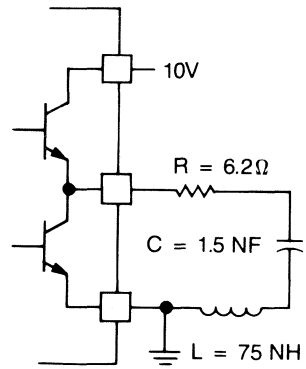


Figure 9. Circuit Parameters

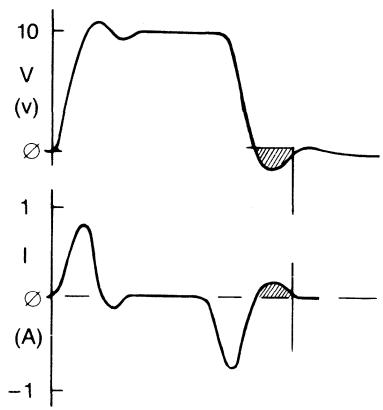


Figure 10. Circuit Response

The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$R\ (gate) \geq 2 \bullet \sqrt{L/C}$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS — highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure xx when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

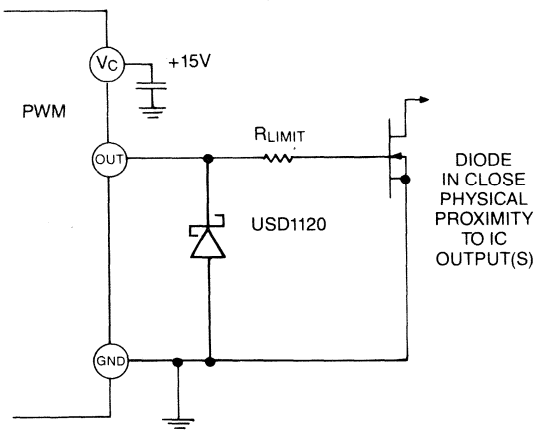


Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1.0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET, high speed applications.

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resultng in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

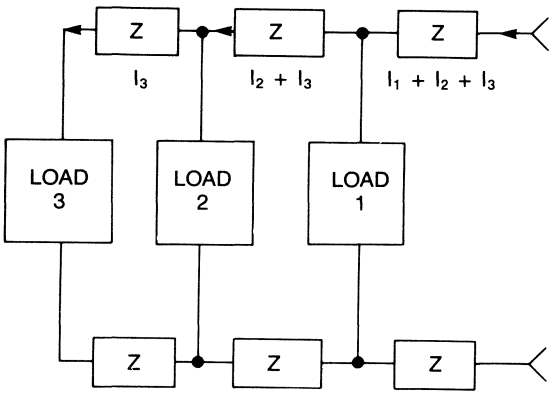


Figure 12.

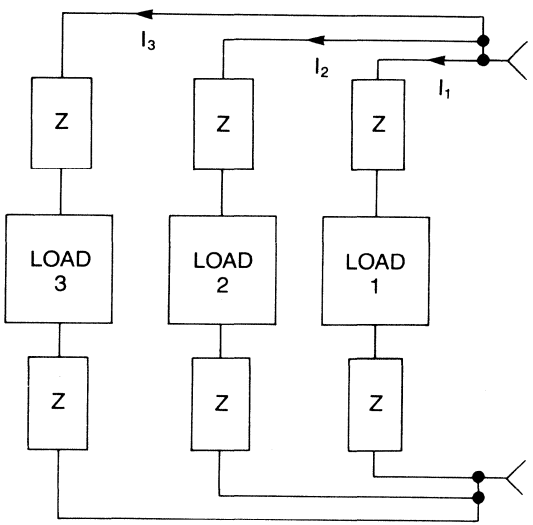


Figure 13.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator. Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

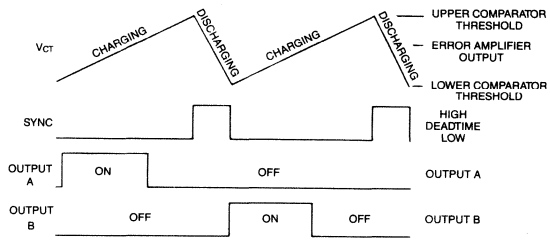


Figure 14. Voltage Mode Control – Normal Operation

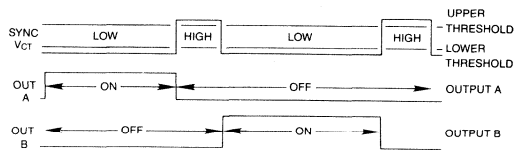


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator. In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

- Sync any PWM to/from any other PWM
- Sync any PWM to/from any number of other PWMs
- Sync from digital levels for simple system integration
- Bidirectional sync signal
- Any PWM can be master or slave with no modifications
- Each control circuit will start and run independently of sync if sync signal is not present
- Localized ramp at Ct for slope compensation
- No critical frequency settings on each module
- High speed — minimum delays
- High noise immunity
- Low power requirements
- Remote off capability
- Minimal effect on frequency, duty cycle, and dead time
- Low cost and component count
- Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

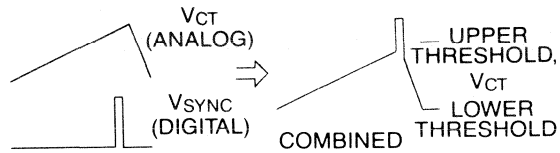


Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor. Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

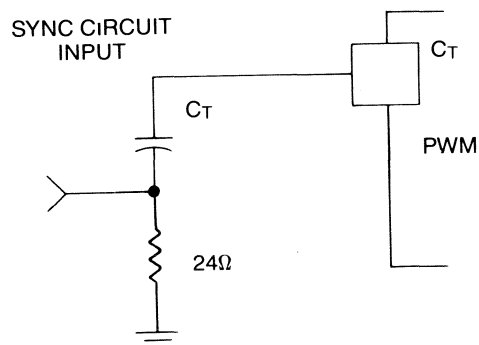


Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail.)

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

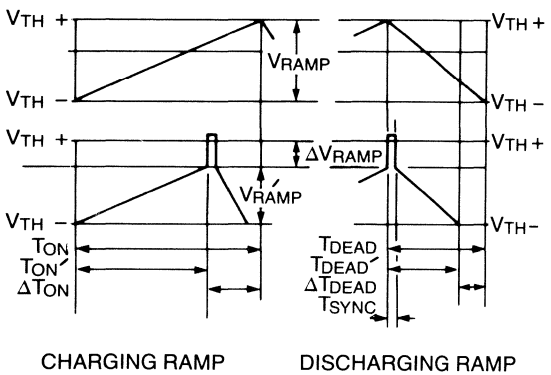


Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\ osc = \frac{1}{Ct}\int I\ chg\ dT = \frac{I\ chg}{Ct}\Big]_0^t \quad T$$

$$T\ chg = \{\ \Delta V\ osc \bullet Ct\ \} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\ osc = Vth\ upper - Vth\ lower$$

$$\Delta V\ osc' = \Delta V\ osc \frac{(tchg')}{t\ chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\ chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator. Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\ chg'}{T\ chg(o)} = \frac{T\ sync}{T\ orig} = \frac{F\ orig}{F\ sync} = P\ \text{"relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\ chg' = T\ chg(o) \bullet P = 0.85\ T\ chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta\ [Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\ [Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) – ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\ dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\ dchg' = T\ dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\ dchg(o) \bullet [\Delta V\ dchg' / \Delta Vosc(o)]$$

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

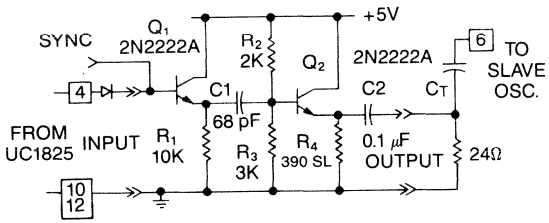


Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor C1, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master. This high speed pulse amplifier circuit adds a minimum of delay ($\approx$ 50 ns) between the master to slave timing relationship.

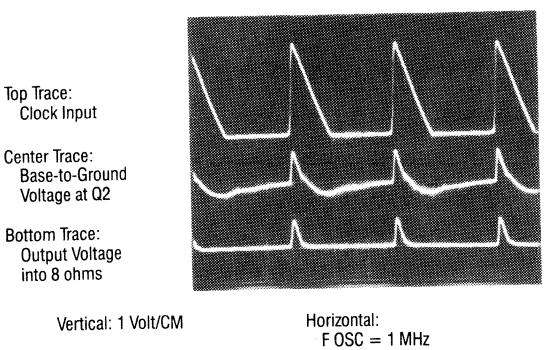


Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.

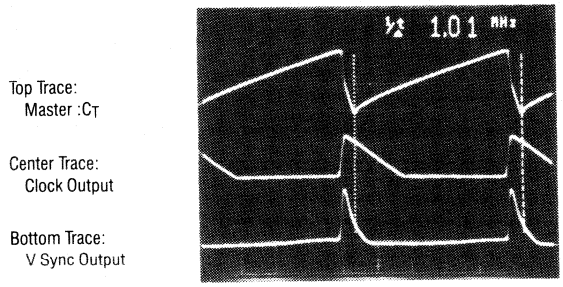


Figure 21. Circuit Timing Waveforms

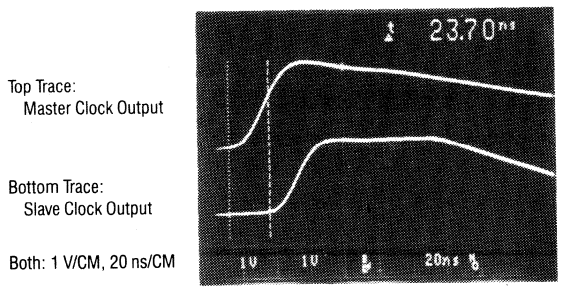


Figure 22. Sync Circuit Delay; Input to Output

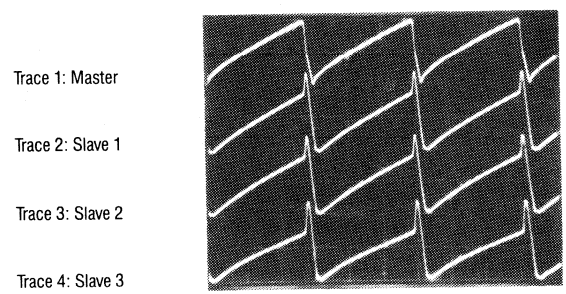
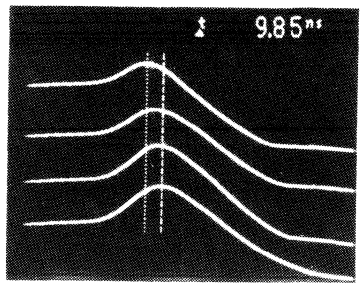


Figure 23. Oscillator Waveforms: Master and Slaves



Trace 1: Master

Trace 2: Slave 1

Trace 3: Slave 2

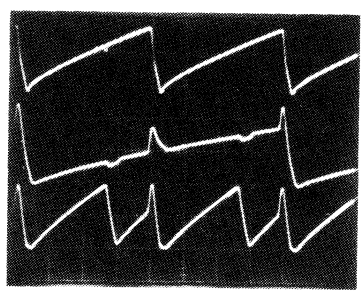
Trace 4: Slave 3

Vertical: 1 V/CM All

Horizontal: 20 ns/CM

Figure 24. Typical Sync Delay at C_T: Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator. In this instance, the sync pulse forces synchronization at alternate cycles to the master.



Top Trace: Master C_T
F OSC = 1.0 MHz

Center Trace: Slave 1
F OSC = 500 KHz

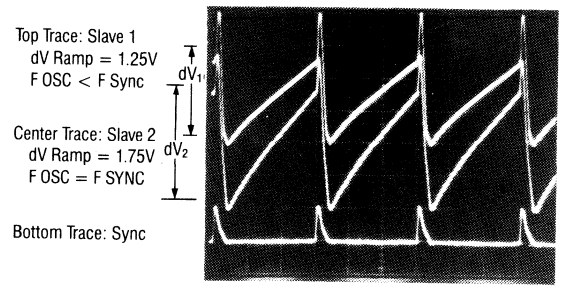
Bottom Trace: Slave 2
F OSC = 1.7 MHz

Vertical: 1 V/CM All

Horizontal: 250 ns/CM

Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.



Top Trace: Slave 1
dV Ramp = 1.25V
F OSC < F Sync

Center Trace: Slave 2
dV Ramp = 1.75V
F OSC = F SYNC

Bottom Trace: Sync

Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

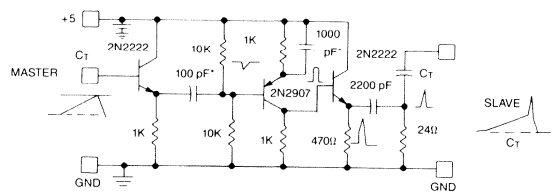


Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

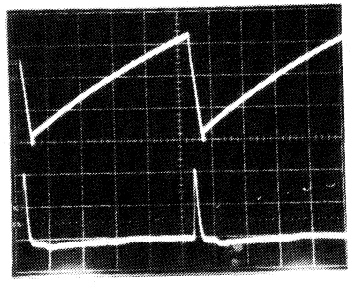


Figure 28. Operating Waveforms at 500 KHz

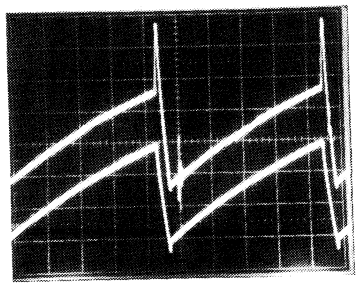


Figure 29. Master/Slave Sync Waveforms at C_T

IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.

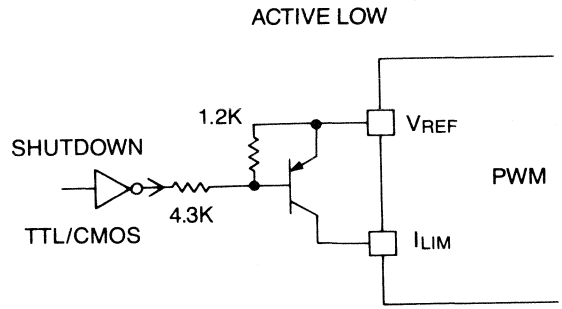


Figure 30. PWM Shutdown Circuits

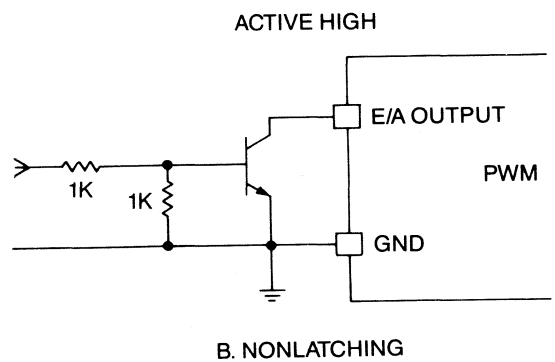
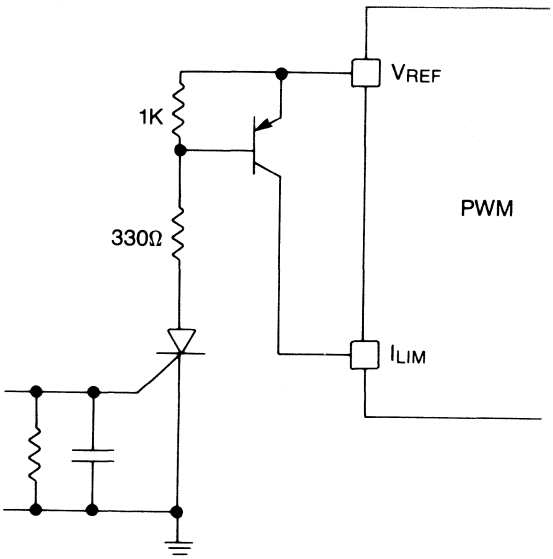


Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

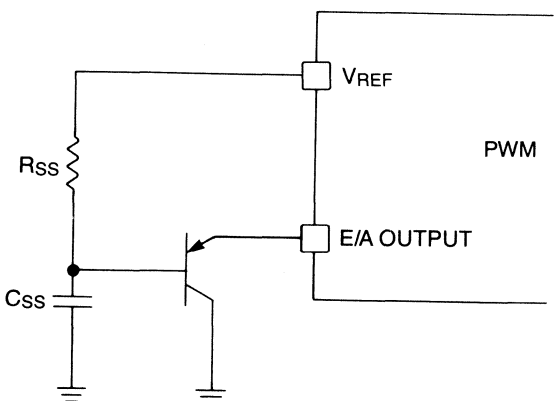


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror. The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

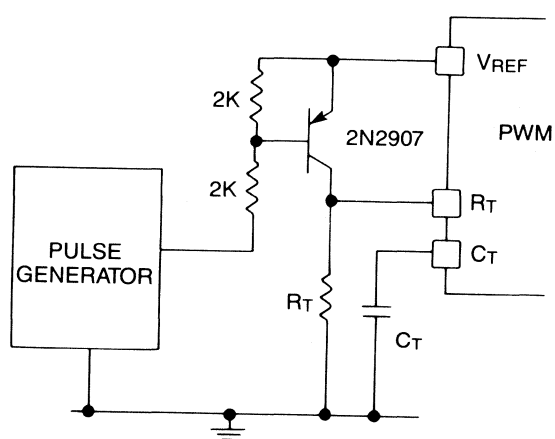


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

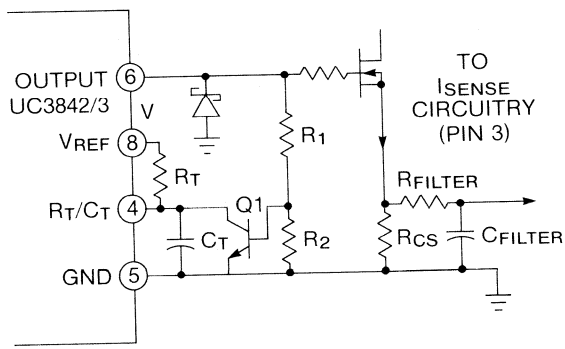
Fixed "Off-Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

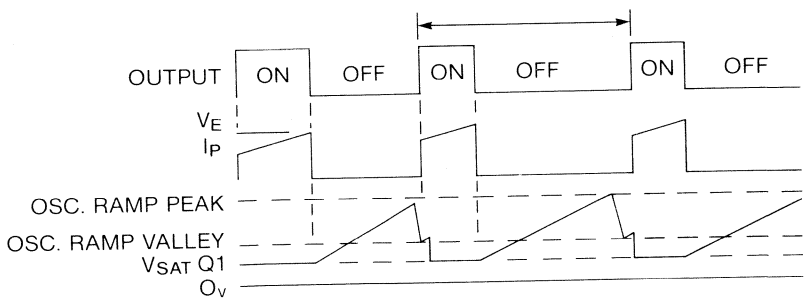
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold. The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

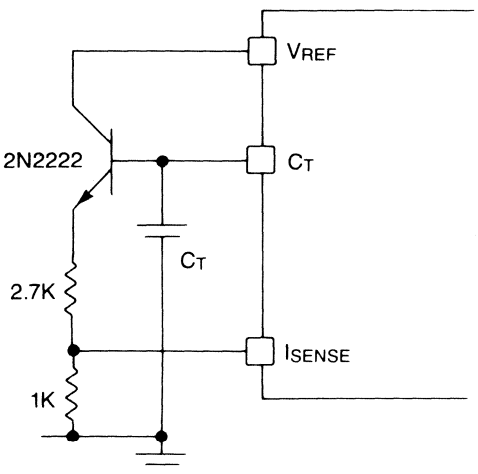


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

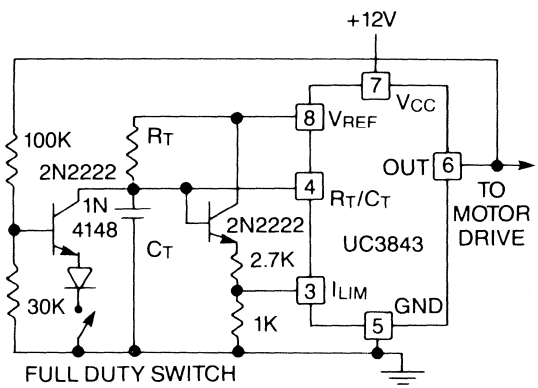


Figure 37. Full Duty Cycle Implementation

VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (<35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

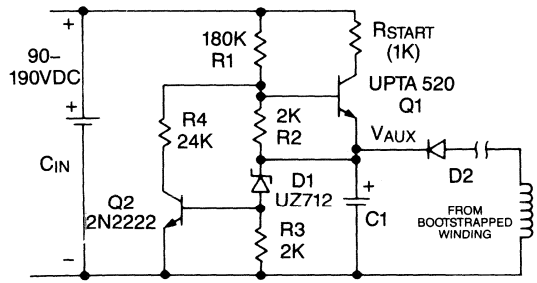


Figure 38. NPN Switches

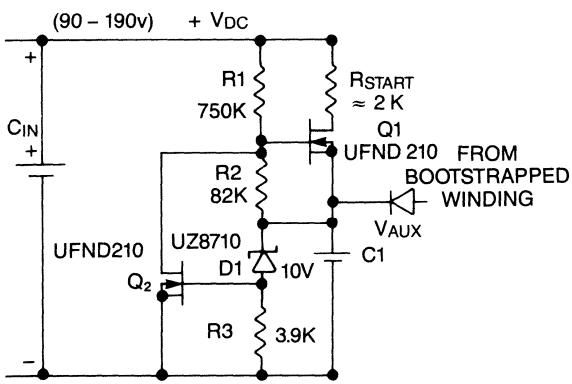


Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor C1 is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to C1 from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and C1 is charged through R start-up from the high voltage DC, as during start-up.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

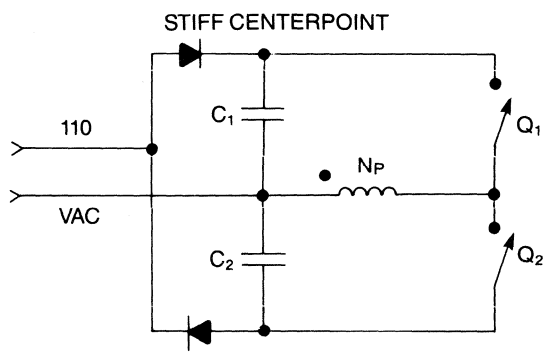


Figure 40.

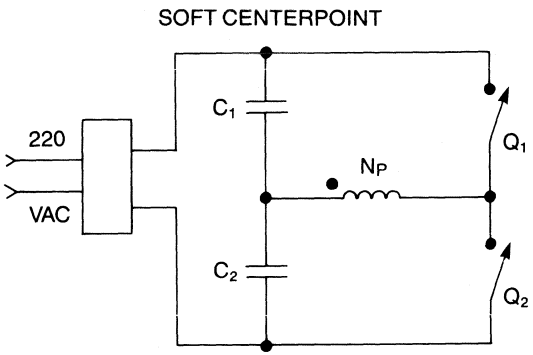


Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

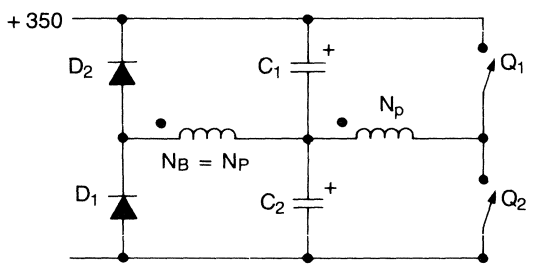


Figure 42. Schematic – Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

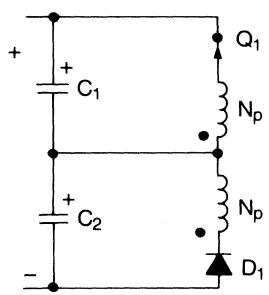


Figure 43. Transistor Q1 On

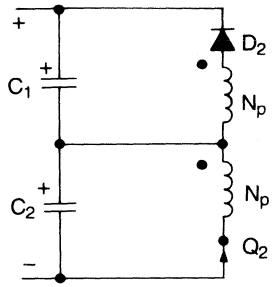


Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

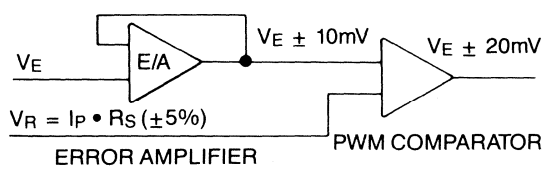


Figure 45. PWM Diagram

In reality, small offets of ± 10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ± 20 millivolt offset represents a ± 2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ± 20 millivolts introduces only ± 0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ± 5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (± 2%) / Rs (± 5%); therefore Ip' = Ip (± 7%) The primary currents (hence output currents) will share within ± seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

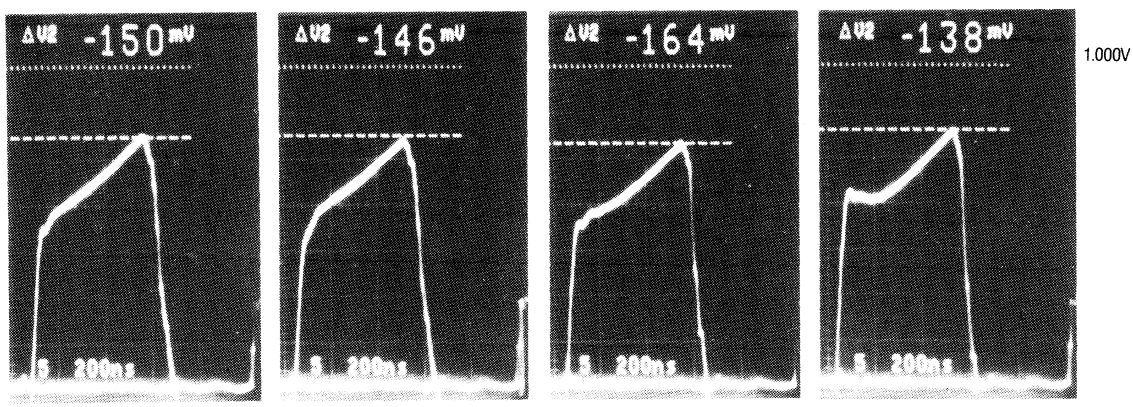


Figure 46. Primary Currents – Parallel Operation

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor. These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

Top Trace:
V_E: Error Voltage with Noise

Lower Trace:
V_R: Primary Current

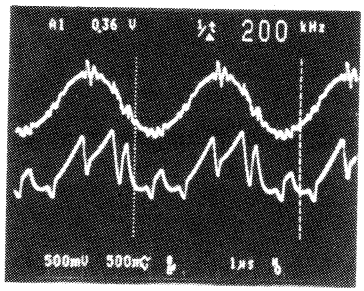


Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter. Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

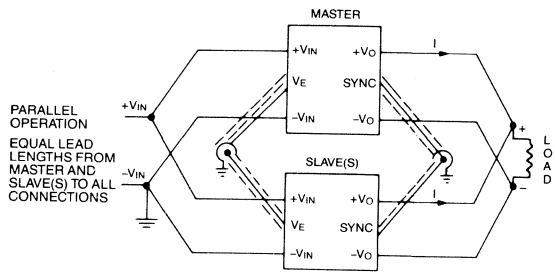


Figure 48.

LINE INPUT AC TO DC CONVERSION AND INPUT FILTER CAPACITOR SELECTION

The input rectifier/filter section of an off-line power supply converts the 50-60Hz AC line voltage to a DC voltage, V_{in}, which powers the downstream high frequency switching section. A circuit diagram typical of a dual range input rectifier/filter section is shown in Figure 1. For 230 volt line operation, the input rectifiers are configured as a full-wave bridge. For 117 volt operation, the input circuit is reconfigured as a voltage doubler, so that V_{in} will be approximately the same as under 230 volt operation. While it is technically possible to operate the input section as a bridge at both 230V and 117V, the switching regulator would have to be designed to operate over a much larger V_{in} range which would significantly increase its cost.

Figure 1. Circuit Diagram

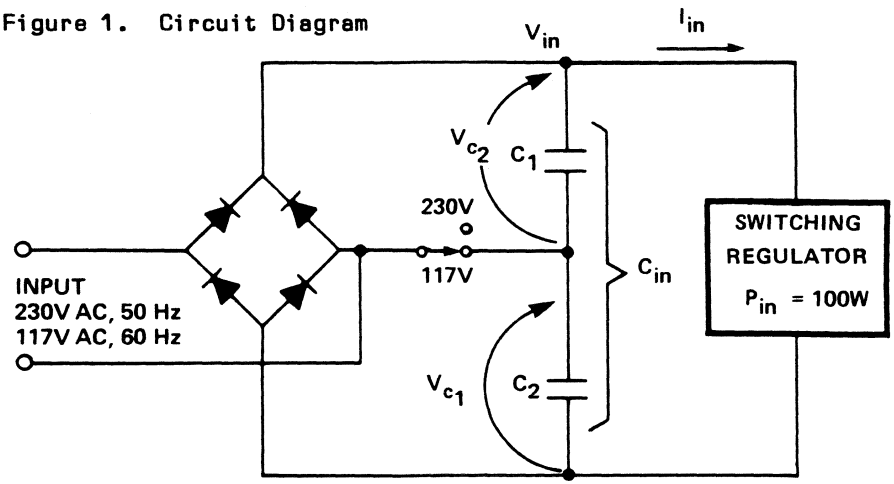


TABLE I - 100 WATT INPUT RECTIFIER/FILTER SECTION

		117V BRIDGE (60Hz)	117V DOUBLER (60Hz)	230V BRIDGE (50Hz)	
RMS Line Voltage	V_{ac}	99-135	99-135	195-265	V
Peak Line Voltage	V_{pk}	140-191	280-382	276-375	V
Max Ripple Voltage	V_r	40	80	76	V
DC Input Voltage	V_{in}	100-191	200-382	200-375	V
Input Capacitance	*C_{in}	203	80	61	µF
Doubler Capacitance	*C1,C2	-	160	(122)	µF
Charging Time	t_c	1.954	2.275	2.345	ms
Peak Charge Current	*i_{chg}	3.64	3.28	1.82	A
RMS AC Chrg Current	*I_{chg}	1.54	1.126	.771	A

* For power levels other than 100 watts, multiply capacitance and current values by $P_{in}/100$ ($P_{in} = P_o/L$).

Input filter capacitance C_{in} determines V_r, the 100/120Hz peak to peak ripple voltage component of V_{in} (see Figure 2). At low line voltage, V_r determines the minimum input voltage, V_{min}, which is an important consideration in the design of the switching supply. V_{min} defines the transformer turns ratio required to achieve the specified output voltage at maximum duty cycle.

If the input filter capacitance is too small, the resulting large ripple voltage will require increased duty cycle range and control loop gain to maintain the specified output voltage. V_{min} will be less, resulting in poor transformer utilization, higher peak current through the switching transistors, and higher peak inverse voltage across the output rectifiers.

Input filter capacitance larger than necessary will not only cost more, the recharging current pulses drawn from the line will be narrower and larger in amplitude (Figure 2). This hurts the line power factor and increases EMI. The higher RMS input current causes increased losses in the line, input rectifiers and filter capacitors, and can impair reliability.

A reasonable rule of thumb is to compromise on a ripple voltage 25-30% of the minimum peak line voltage, resulting in acceptable capacitor size, weight and cost. Table I shows the resulting values for 117V bridge operation with V_{min} of 100V, and 117V doubler and 230V bridge operation with V_{min} of 200V, for a switching supply with 100 watt power input. The input filter capacitors are designed to supply the full load energy of the supply and hold V_{in} above the desired V_{min} between AC line peaks. With the switched dual range input section (117V doubler or 230V bridge) filter capacitor requirements are determined by the voltage doubler configuration.

DESIGN EQUATIONS AND CALCULATIONS:

The following examples are given for full-wave bridge operation from the 230 volt line (195-265V), and full-wave bridge and voltage doubler operation from the 117 volt line (99-135V).

Since virtually all the losses in the switching power supply are downstream of the input rectifer/filter, the input section must handle the entire power input, P_{in} (equal to full load power output divided by efficiency). Power input in these examples is assumed to be 100 watts at full load. The resulting capacitance and current values can be adjusted for any other power input by multiplying by the actual $P_{in}/100$.

Between line peaks, the input filter capacitor must supply the entire full load energy requirement of the supply. Ripple voltage V_r must be small enough to maintain V_{in} greater than the desired V_{min} under worst case conditions of low line frequency, low line voltage and full load. Energy required at 100 watts for

one entire line cycle at 50Hz (worst case used with 230V line):

$$W_{in} = \frac{P_{in}}{f} = \frac{100}{50} = 2.0 \text{ Joules (Watt-seconds)} \quad (1)$$

At 60Hz, the energy required for one line cycle at 100 watts is reduced to 1.667 Joules.

FULL WAVE BRIDGE OPERATION

Referring to Figures 1 and 2, input filter capacitor Cin (C1 in series with C2) charges to peak line voltage each half cycle. Cin then discharges, providing all the energy required by the switching supply until it is recharged at the next half cycle. Energy from Cin each half line cycle is:

$$W_{in}/2 = \frac{1}{2} C_{in}(V_{pk}^2 - V_{min}^2)$$

$$C_{in} = \frac{W_{in}}{V_{pk}^2 - V_{min}^2} \quad (2)$$

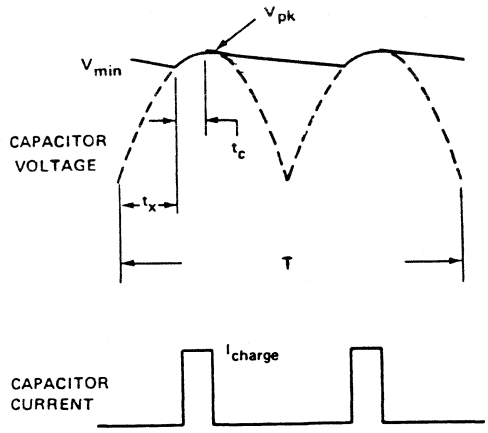


Figure 2. Bridge Waveforms

As shown in Figure 2, the recharging time, t_c, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{min} = V_{pk} \cos(2\pi f\, t_c)$$

$$t_c = \frac{\cos^{-1}(V_{min}/V_{pk})}{2\pi f} \quad (3)$$

Assuming a rectangular charging current pulse of peak amplitude ichg (constant current during the charging interval):

$$\Delta Q = i_{chg}\, \Delta t = C\, \Delta V$$

$$i_{chg} = C\,(V_{pk} - V_{min})/t_c \quad (4)$$

The RMS AC component of the charging current, Ichg, is conducted through the filter capacitors and contributes to capacitor heating due to their equivalent series resistance (ESR). The DC component of the total RMS charging current does not pass through the capacitor and does not contribute to capacitor heating.

$$I_{chg} = \sqrt{ICHG^2 - IDC^2} = \sqrt{ichg^2 tc\ 2/T - ichg^2 (tc\ 2/T)^2}$$

$$I_{chg} = ichg\sqrt{tc\ 2f - (tc\ 2f)^2} \quad (5)$$

The switching supply discharges the input capacitors by drawing high frequency pulses of current. The AC component of the RMS

discharge current, I_{dis}, also causes filter capacitor heating. The filter capacitors must be selected to have RMS current ratings greater than the total RMS AC current components. This is an important consideration for capacitor reliability.

$$\text{Total } I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} \qquad (6)$$

The DC component of the high frequency discharge current pulses equals the DC component of the charging current from the line. Because the form factor of the high frequency discharge current at low line is much better (closer to 1.0) than the charging current waveform, the RMS AC discharge current, I_{dis}, is much less than I_{chg}, depending somewhat on the switching circuit topology.

For 230V (50Hz) bridge operation: At 195V minimum line voltage, the minimum peak voltage, Vpk, is 276V. Conservatively assume 270V peak, allowing for drops in rectifiers and line. From Equation (2):

$$C_{in} = \frac{2}{270^2 - 200^2} = 61\ \mu F$$

Charging pulse width from Equation (3):

$$t_c = \frac{\cos^{-1}(200/270)}{2\pi\ 50} = 2.345\ ms$$

Peak charging current from Equation (4):

$$i_{chg} = 61(270-200)/2.345 \times 10^{-3} = 1.82\ A$$

RMS charging current from Equation (5):

$$t_c\ 2f = 2.345 \times 10^{-3}\ 2\ 50 = .2345$$

$$I_{chg} = 1.82\sqrt{.2345 - .2345^2} = .771\ A$$

For 117V (60Hz) bridge operation (normally used only for single range 117V input): At 99 volts minimum line, minimum Vpk is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line:

$$C_{in} = \frac{1.667}{135^2 - 100^2} = 203\ \mu F$$

$$t_c = \frac{\cos^{-1}(100/135)}{2\pi\ 60} = 1.954\ ms$$

$$i_{chg} = 203(135-100)/1.95 \times 10^{-3} = 3.64\ A$$

$$t_c\ 2f = 1.954 \times 10^{-3}\ 2\ 60 = .2345$$

$$I_{chg} = 3.64\sqrt{.2345 - .2345^2} = 1.54\ A$$

VOLTAGE DOUBLER OPERATION, 117 VOLT (60Hz) LINE:

Referring to Figures 1 and 3, at minimum line voltage (99V), the peak voltage is 140V. Conservatively assume 135V peak, allowing for drops in rectifiers and line.

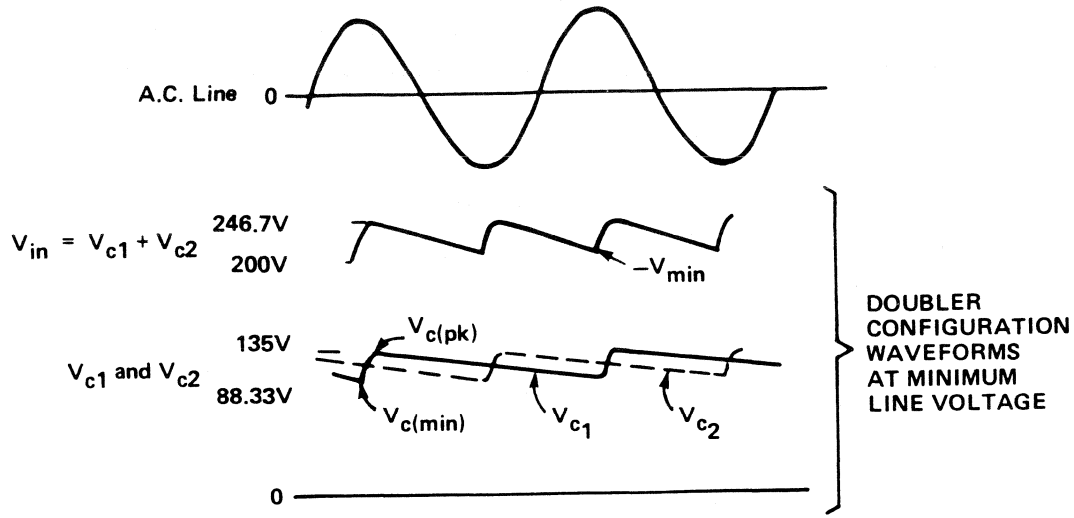


Figure 3. Voltage Doubler Waveforms

C_1 and C_2 alternately charge to peak line voltage. Note that whenever the input voltage, V_{in}, is at instantaneous minimum, one capacitor is at its minimum, but the other capacitor is half way between peak and minimum voltage. The minimum voltage on each capacitor corresponding to an overall V_{min} of 200V can be approximated as follows:

$$V_{min} = VC1min + VC2avg = VCmin + \frac{VCmin + VCpk}{2}$$

$$VCmin = \frac{2V_{min} - VCpk}{3} = \frac{2(200) - 135}{3} = 88.33\ V \qquad (7)$$

C1 and C2 each discharge for a complete cycle. Each capacitor must supply half the energy required by the switching regulator for an entire line cycle:

$$W/2 = \frac{1}{2} C_1 (VCpk^2 - VCmin^2)$$

$$C1 = C2 = \frac{W}{VCpk^2 - VCmin^2} = \frac{1.667}{135^2 - 88.33^2} = 160\ \mu F \qquad (8)$$

C_{in}, the series combination of C_1 and C_2, equals 80 µF

Note that the voltage doubler operated from the 117V line requires larger C_{in} than the 230V bridge input, so that for supplies with dual range 117/230 volt input, the 117V doubler

operation dictates the filter capacitor requirements.

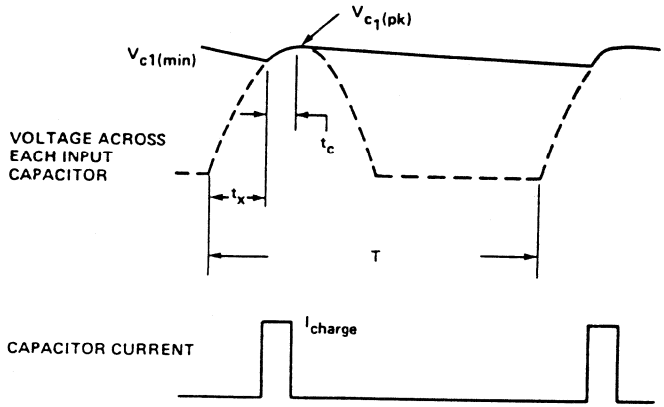


Figure 4. Voltage Doubler Charging Current

Figure 4 shows the waveforms associated with charging each of the input capacitors in the voltage doubler configuration at full load and minimum line voltage. Recharge time, t_c, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{C1min} = V_{C1pk} \cos(2\pi f\, t_c)$$

$$t_c = \frac{\cos^{-1}(V_{C1min}/V_{C1pk})}{2\pi f} \qquad (9)$$

$$t_c = \frac{\cos^{-1}(88.3/135)}{2\pi\ 60} = \qquad 2.275 \text{ ms}$$

Assuming a rectangular charging current pulse of peak amplitude ichg (constant current during the charging interval):

$$\Delta Q = i_{chg}\,\Delta t = C\,\Delta V$$

$$i_{chg} = C\,(V_{pk} - V_{min})/t_c \qquad (10)$$

$$i_{chg} = 160(135-88.3)/2.275 \times 10^{-3} = \qquad 3.28 \text{ A}$$

The RMS current in each capacitor is:

$$I_{chg} = i_{chg}\text{-}/t_c f - t_c f^2 \qquad (11)$$

$$t_c f = 2.275\text{x}10^{-3}\ 60 = .1365$$

$$I_{chg} = 3.28\text{-}/.1365 - .1365^2 = \qquad 1.126 \text{ A}$$

MAGNETICS DEFINITIONS AND EQUATIONS

SYMBOLS, UNITS, AND CONVERSION FACTORS:

Parameter	Symbol	SI Units	CGS Units	CGS to SI
Magnetic Flux Density	B	Tesla	Gauss	10^{-4}
Magnetic Field Intensity	H	A-T/m	Oersted	$1000/4\pi$
Permeability (Free Space)	μ_o	$4\pi \cdot 10^{-7}$	1	$4\pi \cdot 10^{-7}$
Permeability (Relative)	μ_r			1
Effective Magnetic Area	A_e	m^2	cm^2	10^{-4}
Mean Magnetic Path Length	ℓ_e	m	cm	10^{-2}
Air Gap Length	ℓ_g	m	cm	10^{-2}
Magnetic Flux ($\int BdA$)	Φ	Weber	Maxwell	10^{-8}
Magnetic Potential ($\int Hdl$)	mmf	Amp-Turn	Gilbert	$10/4\pi$
Inductance	L	Henry	*Henry	1
Inductance Index	AL	nH (1turn)	nH (1turn)	1
Window Area of Core	A_w	m^2	cm^2	10^{-4}
Wire Cross Section Area	A_x	m^2	cm^2	10^{-4}
Number of turns	N			1
Mean Length per Turn	lt	m	cm	10^{-2}
Current Density	J	A/m^2	A/cm^2	10^4
Resistivity	ρ	Ω-m	Ω-cm	10^{-2}
Area Product, A_wA_e	AP	m^4	cm^4	10^{-8}
Energy	W	Joule	Erg	10^{-7}

*Commonly used in place of Abhenrys = Henries.10^9.

BASIC EQUATIONS AND DERIVATIONS (SI Units):

International standard (SI) units (rationalized MKS) are used in the following derivations. The equations are often dimensionally modified in application to allow the use of centimeters instead of meters.

Assumptions used (within the region of interest):

1. Uniform distribution of Flux Density, B
2. Uniform distribution of Field Intensity, H
3. Constant Permeability, μ_r (Linear B/H characteristic)

Magnetic Field Relationship:

$$B = \mu_o \mu_r H \tag{1}$$

Magnetic Potential, from Ampere's Law:

$$mmf = \int H\, d\ell = H\ell = NI \quad \text{Ampere-Turns} \tag{2}$$

Faraday's Law of Induction:

$$E = N\frac{d\Phi}{dt} = N A_e \frac{dB}{dt} \quad \text{Volts} \tag{3}$$

Energy Storage:

from (3): $E\,dt = N A_e dB$ (3A)

from (2): $I = \frac{H\ell}{N}$ (2A)

combining, $W = \int E\,I\,dt = \int N A_e dB \cdot H\ell/N = A_e \ell_e \int H\,dB$

$$W = \frac{1}{2} B\,H\,A_e \ell_e = \frac{B^2 A_e \ell_e}{2\mu_o \mu_r} \text{ Joules} \quad (4)$$

$$W/m^3 = \frac{B^2}{2\mu_o \mu_r} \text{ Joules}/m^3 \quad (4A)$$

$$W = \frac{1}{2} L\,I^2 \text{ Joules (Watt-Seconds)} \quad (5)$$

Inductance:

(4)+(5): $\frac{1}{2} L\,I^2 = \frac{1}{2} B\,H\,A_e \ell_e$

Subst. (2A): $L = B\,H\,A_e \ell_e \frac{N^2}{H^2 \ell_e^2} = \frac{B\,N^2 A_e}{H\ \ \ell_e}$

$$L = \mu_o \mu_r N^2 \frac{A_e}{\ell_e} \text{ Henries} \quad (6)$$

Core Hysteresis Losses — Steinmetz Law:

Assumes symmetrical flux density swing +/- B_m about origin.

$$P_h = \eta_h f \int B_m^k\,dv = \eta_h f B_m^k \quad \text{Watts}/m^3 \quad (7)$$

For silicon steel: $k = 1.6$ $\eta_h = 80$
For 3C8 power ferrite: $k = 2.6$, $\eta_h = 159$

Core Eddy Current Losses:

For flat laminations.
t = thickness (m), ρ = resistivity (Ω-m)

$$P_e = \frac{4(f\,t\,B_m)^2}{3\ \ \rho} \quad \text{Watts}/m^3 \quad (8)$$

For transformer steel: $\rho = 0.3\text{-}0.5 \times 10^{-6}$ Ω-m

WINDING DATA

WIRE TABLE — Copper Wire — Heavy Insulation:

AWG	DIAMETER Copper cm	AREA Copper cm^2	DIAMETER Insulatd cm	AREA Ins. cm^2	OHMS/CM 20 C	OHMS/CM 100 C	AMPS for 450A/cm^2
10	.259	.052620	.273	.058572	.000033	.000044	23.679
11	.231	.041729	.244	.046738	.000041	.000055	18.778
12	.205	.033092	.218	.037309	.000052	.000070	14.892
13	.183	.026243	.195	.029793	.000066	.000088	11.809
14	.163	.020811	.174	.023800	.000083	.000111	9.365
15	.145	.016504	.156	.019021	.000104	.000140	7.427
16	.129	.013088	.139	.015207	.000132	.000176	5.890
17	.115	.010379	.124	.012164	.000166	.000222	4.671
18	.102	.008231	.111	.009735	.000209	.000280	3.704
19	.091	.006527	.100	.007794	.000264	.000353	2.937
20	.081	.005176	.089	.006244	.000333	.000445	2.329
21	.072	.004105	.080	.005004	.000420	.000561	1.847
22	.064	.003255	.071	.004013	.000530	.000708	1.465
23	.057	.002582	.064	.003221	.000668	.000892	1.162
24	.051	.002047	.057	.002586	.000842	.001125	.921
25	.045	.001624	.051	.002078	.001062	.001419	.731
26	.040	.001287	.046	.001671	.001339	.001789	.579
27	.036	.001021	.041	.001344	.001689	.002256	.459
28	.032	.000810	.037	.001083	.002129	.002845	.364
29	.029	.000642	.033	.000872	.002685	.003587	.289
30	.025	.000509	.030	.000704	.003386	.004523	.229
31	.023	.000404	.027	.000568	.004269	.005704	.182
32	.020	.000320	.024	.000459	.005384	.007192	.144
33	.018	.000254	.022	.000371	.006789	.009070	.114
34	.016	.000201	.020	.000300	.008560	.011437	.091
35	.014	.000160	.018	.000243	.010795	.014422	.072
36	.013	.000127	.016	.000197	.013612	.018186	.057
37	.011	.000100	.014	.000160	.017165	.022932	.045
38	.010	.000080	.013	.000130	.021644	.028917	.036
39	.009	.000063	.012	.000106	.027293	.036464	.028
40	.008	.000050	.010	.000086	.034417	.045981	.023
41	.007	.000040	.009	.000070	.043399	.057982	.018

American Wire Gauge (AWG) Table Formulae:

$D_X = \frac{2.54}{\pi} 10^{-AWG/20}$ cm — Conductor Diameter

$D_X' = D_X + .028 - /\overline{D_X}$ cm — Includes Heavy Insulation

$A_X = \pi D_X^2/4$ cm^2 — Wire Cross-Section Area

$R_X = \rho/A_X$ Ω/cm — Resistance/Length

Resistivity (Copper) at temperature T:

$$\rho = 1.724\,(1+.0042(T-20)) \times 10^{-6} \quad \Omega\text{-cm}$$

(ρ (copper) at 20°C = 1.724×10^{-6} Ω-cm)

Current density limit:

An RMS current density of 450 A/cm² (2900 A/in²) causes approximately 30°C temperature rise with natural convection cooling for a transformer or inductor whose core area product ($AP = A_w A_e$) is 1 cm⁴. With larger cores, the current density for 30 °C rise diminishes because the heat dissipating surface area increases less rapidly than the heat producing volume:

$$J_{max} = 450\ AP^{-.125} \quad A/cm^2$$

Winding Area:

The core window area, A_w, is multiplied by the factor K_u to obtain the total area of all conductors, and by K_p to obtain A_p, the area of the primary winding (A_p = 1/2 of center-tapped primary):

$$A_p = K_u K_p A_w.$$

K_u, Window Utilization Factor is the fraction of the window area that is actual conductor area. K_u accounts for the insulation between windings, creepage distances at ends of windings, wire insulation, and fill factor (wire shape and lay). K_u of 0.4 is typical with high voltage insulation, round AWG 20 wire and no bobbin. With bobbin, K_u reduces to 0.3.

K_p, Primary Area Factor indicates the relative area of the primary winding with respect to the total area of all windings, proportioned so that all windings operate at the same RMS current density and power density.

Configuration	K_p	A_{pri}	A_{sec}
SE/SE	0.5	0.5	0.5
SE/CT	.414	.414	.293-.293
CT/CT (Half)	.25	.25-.25	.25-.25

SE/SE: Single-Ended primary/secondaries (Forward Converter, Flyback, Boost)
SE/CT: Single-Ended primary/Center-Tap secondaries (Bridge, Half Bridge)
CT/CT: Center-Tap primary/secondaries (Full Wave Center-Tap)

Insulation requirements between windings for off-line applications:

Requirements are complex, depending upon application and specification.
International spec info: EMACO, 7562 Trade Street, San Diego, CA 92121.
IEC specs: ANSI, 1430 Broadway, New York, NY.

Per VDE 0806 and IEC 380, for office equipment:

Thickness: 3 layers, 1 mil Mylar (6.6 mil/.016cm with adhesive)
Creepage, PtoS: 0.6cm (0.23inch)
Faraday Shields: 1.4 mil Copper foil (3 mil/.0076cm with adhesive)

RMS Current Components:

The relationships between peak current, I_p, total rms current, I, and its DC and AC components, I_{DC} and I_{AC}, are given below for several of the current waveshapes commonly encountered in switching power supplies. Eddy current losses are a function of the AC winding resistance and the rms AC current component, I_{AC}, whereas low frequency losses are a function of the DC winding resistance and the *total* rms current, I.

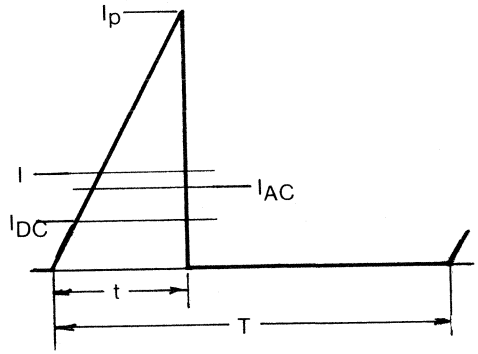
$$I^2 = I_{DC}^2 + I_{AC}^2 \; ; \qquad d = t/T$$

Discontinuous mode waveform:

$$I_{DC} = I_p d/2$$

$$I_{AC} = I_p(d/3 - d^2/4)^{1/2}$$

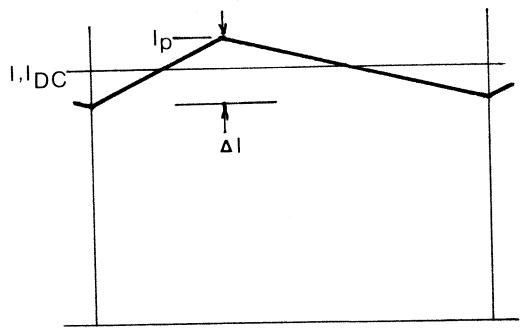
$$I = I_p(d/3)^{1/2}$$



Continuous mode - filter inductor:

$$I \simeq I_{DC} = I_p - \Delta I/2$$

$$I_{AC} = \Delta I/(12)^{1/2}$$

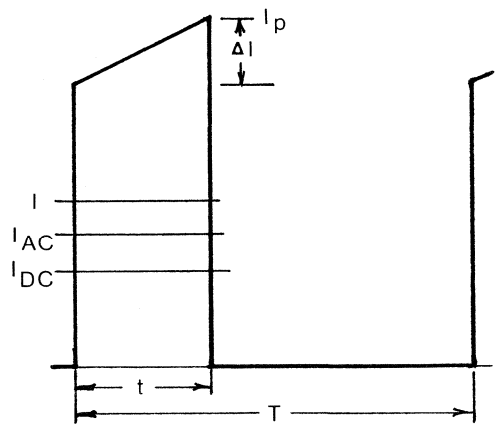


Continuous mode - transformer winding:

$$I_{DC} = (I_p - \Delta I/2)d$$

$$I_{AC} \simeq (I_p - \Delta I/2)[d(1-d)]^{1/2}$$

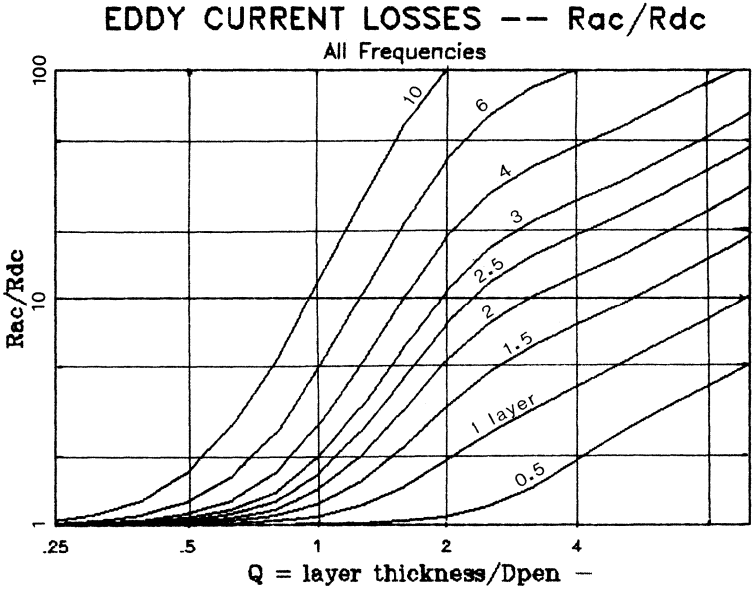
$$I \simeq (I_p - \Delta I/2)d^{1/2}$$



Eddy Current Losses: The curve below shows F_R, the ratio of AC to DC resistance, for closely wound windings of round wire or for flat strip. F_R is a function of penetration (skin) depth, D_{pen}, conductor thickness, h, layer copper factor, F_L, and the number of layers in the winding portion. When the windings are not interleaved, the entire primary is one winding portion, as is the entire secondary group. With the primary divided into two halves interleaved inside and outside the secondary group, each half primary is a winding portion. The also secondary becomes two portions, each facing one half the primary. This halves the number of layers in each portion and dramatically reduces eddy current losses.

To find the AC resistance factor, F_R, first calculate the penetration depth, D_{pen}, at the switching frequency from the formula given below. The value Q equals $0.8(d/D_{pen})$ for close spaced round wires, or h/D_{pen} for flat strip, where d = wire diameter, h = strip thickness.

The resulting F_R value is for a sinusoidal waveform, ignoring the harmonic content of the actual waveforms encountered in switching power supplies. Although the resulting error can be quite large with narrow pulses which have high harmonic content, worst case losses are usually at duty cycles of greater than 0.4, where the error is 20-30%. When greater accuracy is needed, compute F_R and losses for each of the Fourier waveform components.



Penetration depth for copper at 100°C: $D_{pen} = 7.5\ f^{-1/2}$ cm

Q depends upon the layer copper factor, F_L, which is a function of the spacing and shape of the conductors in a layer. In Eq. 1, $h(F_L)^{1/2}$ equals 1 for solid copper strip and approximately 0.8 for close spaced round wire. For round wire of any spacing, F_L may be calculated using Eq. 2.

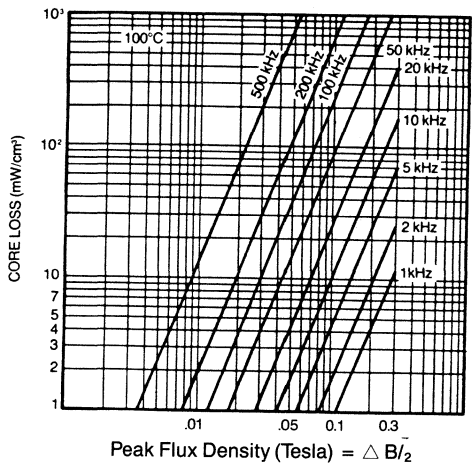
(1) $Q = h(F_L)^{1/2}/D_{pen}$; h = .866 dia for round wire

(2) F_L = .866 dia•$N\ell/b_W$; $N\ell$ = turns/layer, b_W = winding breadth

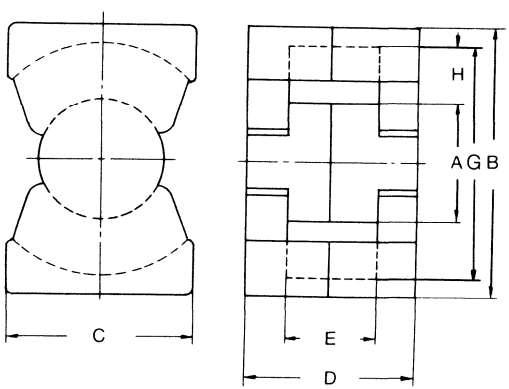
DATAFILE: CORE.DAT 11-18-1985, 09:45:35

Rec #	Description	Core Type	AP	B	G	D	C	A	E bw	H hw	Ae	le	Ve	Aw	MLT	As	Rt
1	EC70	ER	17.83	7.00	4.45	6.90	1.64	1.64	4.55	1.41	2.79	14.40	40.10	6.39	9.57	142.19	7.50
2	EC70 with bobbin	ER	14.36	7.00	4.45	6.90	1.64	1.64	4.15	1.24	2.79	14.40	40.10	5.15	10.08	142.19	7.50
3	ETD49	ER	7.87	4.87	3.70	4.94	1.63	1.63	3.62	1.03	2.11	11.40	24.20	3.73	8.39	80.10	11.00
4	PQ40/40	PQ	6.40	4.00	3.70	4.00	2.80	1.52	2.92	1.09	2.01	10.20	20.50	3.18	8.20	76.80	12.00
5	EC52	ER	5.59	5.22	3.30	4.84	1.34	1.34	3.17	0.98	1.80	10.50	18.80	3.11	7.29	77.49	11.00
6	ETD44	ER	5.28	4.40	3.33	4.46	1.48	1.48	3.30	0.92	1.74	10.30	18.00	3.04	7.57	65.47	12.00
7	EC52 with bobbin	ER	4.63	5.22	3.30	4.84	1.34	1.34	3.06	0.84	1.80	10.50	18.80	2.57	7.73	77.49	11.00
8	PQ35/35	PQ	4.21	3.50	3.20	3.50	2.60	1.46	2.47	0.87	1.96	8.79	17.26	2.15	7.32	60.90	16.00
9	ETD39	ER	3.21	3.91	3.01	3.96	1.25	1.25	2.92	0.88	1.25	9.21	11.50	2.57	6.69	50.64	15.00
10	EC41	ER	2.59	4.06	2.70	3.90	1.16	1.16	2.78	0.77	1.21	8.93	10.80	2.14	6.06	50.14	16.50
11	PQ32/30	PQ	2.33	3.20	2.75	3.06	2.20	1.37	2.10	0.69	1.61	7.46	11.97	1.45	6.47	47.13	18.50
12	EC41 with bobbin	ER	1.90	4.06	2.70	3.90	1.16	1.16	2.45	0.64	1.21	8.93	10.80	1.57	6.47	50.14	16.50
13	ETD34	ER	1.83	3.42	2.63	3.46	1.08	1.08	2.42	0.78	0.97	7.86	7.64	1.89	5.81	38.53	19.00
14	EC35	ER	1.36	3.43	2.27	3.46	0.95	0.95	2.45	0.66	0.84	7.74	6.53	1.62	5.06	36.83	18.50
15	PQ32/20	PQ	1.31	3.20	2.75	2.08	2.20	1.37	1.12	0.69	1.70	5.55	9.42	0.77	6.47	36.54	22.00
16	PQ26/25	PQ	0.96	2.65	2.25	2.50	1.90	1.22	1.58	0.52	1.18	5.55	6.53	0.81	5.45	32.82	24.00
17	EC35 with bobbin	ER	0.94	3.43	2.27	3.46	0.95	0.95	2.16	0.52	0.84	7.75	6.53	1.12	5.50	36.83	18.50
18	PQ26/20	PQ	0.69	2.65	2.25	2.04	1.90	1.22	1.12	0.52	1.19	4.63	5.49	0.58	5.45	28.63	30.00
19	PQ20/20	PQ	0.39	2.05	1.80	2.04	1.40	0.90	1.40	0.45	0.62	4.54	2.79	0.63	4.24	19.82	36.00
20	PQ20/16	PQ	0.28	2.05	1.80	1.64	1.40	0.90	1.00	0.45	0.62	3.74	2.31	0.45	4.24	17.06	42.00

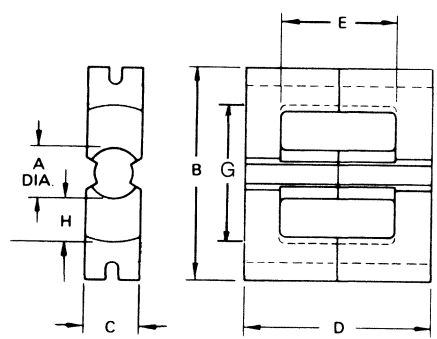
3C8 Core Loss vs. Flux Density



PQ Cores



EC, ETD Cores



Ferrite Core Loss: The temperature rise contribution due to core losses is a function of the loss/cm³, P_C/cm^3, the core volume, V_e, and the thermal resistance, R_t. Core volume and thermal resistance vs. area product are shown in the two curves. The data points are actual cores from the EC, ETD, RM, and PQ families. The empirical equations given have been fitted to this data. Thermal resistance data is for natural convection cooling.

Core losses are a function of the peak-to-peak flux swing, ΔB, the frequency at which flux changes in the core (single-ended $f = f_S$, push-pull $f = f_S/2$). k_H is the hysteresis loss coefficient and k_E is the eddy current loss coefficient.

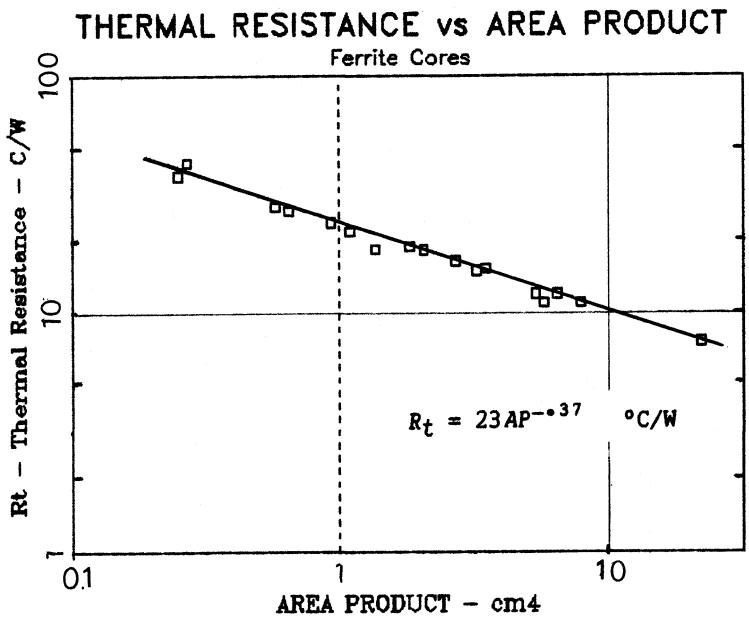
The scale labeled "flux density" at the bottom of most published core loss curves usually means the *peak* flux density (1/2 the total swing). Divide ΔB values by two before using such curves.

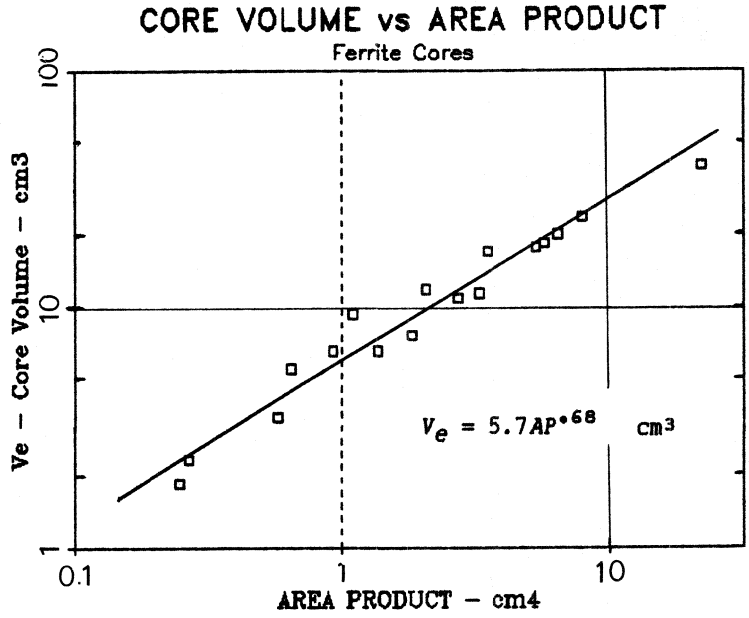
$$\Delta T = R_T V_e (P_C/cm^3)$$

$$P_C/cm^3 = \Delta B^{2.4}(k_H f + k_E f^2)$$

For typical power ferrites:

$k_H = 4 \cdot 10^{-5}$; $k_E = 4 \cdot 10^{-10}$





REVIEW OF BASIC MAGNETICS
THEORY, CONCEPTUAL MODELS AND DESIGN EQUATIONS

by

Lloyd H. Dixon, Jr.

This paper develops the basic theory and fundamental equations used in the design of magnetic components, with a strong emphasis on developing the ability to conceptualize physical models of the magnetic fields within these devices.

Fortunately, magnetics design for switching power supplies does not require an extremely rigorous approach, and many simplifying assumptions may be successfully employed. It is much more profitable to simplify, compartmentalize the problem into two or three regions within which the assumptions are valid, and subsequently make empirical corrections when necessary.

Inductance is a concept which represents magnetically stored energy in electrical circuits. Many design engineers find it impossible to concepualize inductance in direct physical terms within the magnetic device structure. It is best to abandon this attempt. Instead, it is much easier and more useful to conceptualize energy storage in the magnetic fields. Inductance values in the equivalent circuit represent energy stored in various physical regions of the device.

Symbols, definitions, equations and conversion factors from CGS to International Standard (SI) units are defined in section M1 in the back of this seminar book.

Magnetic Field Relationships:

Single Wire. Figure 1 shows the end view of the magnetic field near a straight-line conductor carrying 8 amperes (or a bundle of eight conductors each carrying one ampere). The current return path is either at infinity or a coaxial cylinder beyond the the extent of the illustration. The circles represent flux lines, and the radial lines represent an edge view of the magnetic field equipotential surfaces.

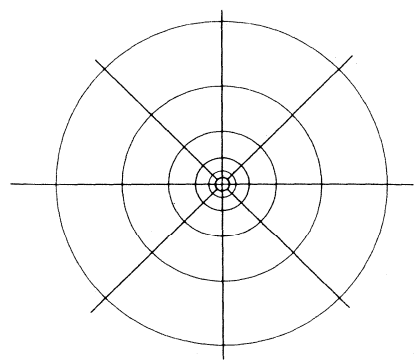


Figure 1.

It is important to remember the following rules which govern the magnetic field:

1. Magnetic field equipotentials are surfaces, not lines. (The magnetic field can also be expressed as a vector normal to the field surface. This a often a useful mathematical representation, but it is less helpful in conceptualizing the physical model.)

2. Magnetic field equipotential surfaces are bounded and terminated by the ampere-turns generating the field. They are not closed surfaces like electric field equipotentials are.

3. The total magnetic field, Hl, integrated around any path equals the total ampere-turns enclosed by that path (Amperes Law):

$$\int H\,dl = NI \quad \text{Ampere-Turns} \tag{1}$$

Note that the magnitude of the total magnetic field is independent of the permeability, $\mu = B/H$, of the regions traversed, although the field may be severely distorted in a magnetically non-homogeneous structure such as a gapped core.

The total magnetic field (often called magneto-motive force, mmf), is independent of the path taken around the conductor. In Figure 1 the magnetic field intensity, H, is inversely proportional to the distance, r, from the center of the conductor, as indicated by the increased spacing between the equipotential surfaces:

$$H = NI/l, \quad l = 2\pi r$$

$$H = \frac{NI}{2\pi r} \quad \text{Ampere-Turns/meter} \tag{2}$$

The flux density, B, behaves in the following manner:

1. Magnetic flux is in the form of lines, not surfaces.

2. Flux lines are always closed loops. Flux lines never begin or end. In any arbitrary volume, anywhere in the universe, the number of flux lines entering that volume must equal the number of lines leaving it. This is true even if the given volume contains magnetic material or current-carrying coils of wire.

3. The flux density, B, is always proportional to the magnetic field intensity and permeability:

$$B = \mu H, \qquad \mu = \mu_o \mu_r = B/H \tag{3}$$

4. Flux lines are always normal to the magnetic field equpotential surfaces (aligned with the vector magnetic field).

Assuming the permeability is constant (linear B/H characteristic), the energy stored per unit volume in the magnetic field is:

$$W/m^3 = \int H\,dB = \frac{1}{2}BH \quad \text{Joules/m}^3 \qquad (4)$$

Specifically for the field surrounding a straight wire as shown in Figure 1, substituting Equations 3 and 2 into Equation 4 shows that the energy density varies inversely with the square of the distance from the center of the wire:

$$W/m^3 = \frac{\mu}{2}\left(\frac{NI}{2\pi r}\right)^2$$

The energy density integrated throughout the volume surrounding the wire represents the inductance of the straight wire. It is difficult to conceptualize this inductance directly, but easy to conceive of it as stored energy.

Another important relationship between magnetic parameters and the electrical circuit derives from Faraday's Law of Induction. If a coil is placed in a magnetic field, a voltage will be induced in the coil proportional to the rate of change of the flux, Φ, within the coil:

$$E = N\frac{d\Phi}{dt} = NAe\frac{dB}{dt} \quad \text{Volts} \qquad (5)$$

Two Wires. Figure 2 shows the field around two parallel conductors with the same current flow in opposite directions, i.e. the current return path is now in close proximity. Each wire has a field identical to Figure 1, but of opposite polarity. The fields reinforce between the two wires, but elsewhere they tend to cancel, especially as the distance from the wires becomes great and the opposing fields become nearly equal.

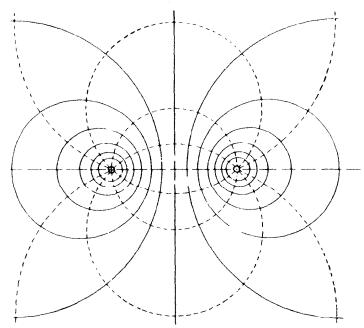


Figure 2.

Simple Winding. With multiple turns of wire in a helical array or single layer solenoid as shown in Figure 3, the field in the center of the winding becomes more concentrated and relatively linear. Assuming 8 turns, with a current of 1 ampere, the total field integrated through the center of the winding using Equation 1 is 8 ampere-turns, the same as the single conductor carrying 8 amperes in Figure 1.

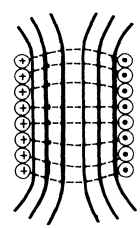


Figure 3.

Even though the field is more concentrated, there may still be more energy stored outside of the solenoid than within it. This is because the stray field outside the solenoid, although highly attenuated, extends to infinity. Magnetically, there is no such thing as insulation. The finite permeability of free space allows the magnetic field to propagate indefinitely.

Shielding. It is possible to provide magnetic shielding. This is accomplished in Figure 4 by surrounding the winding with a box of high permeability material such as ferrite, which shorts out the external magnetic field. Note that this also causes the field to become even more concentrated and more uniformly distributed, making it simple to calculate the energy in the field. The total flux within the ferrite is comparable to that within the winding, but the energy stored within the ferrite is negligible because with its high permeability the magnetic field is virtually zero.

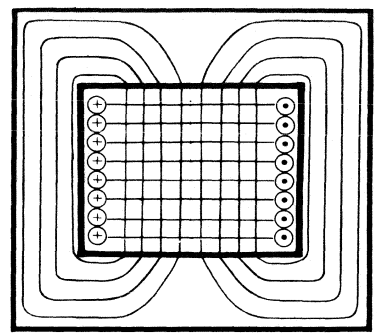
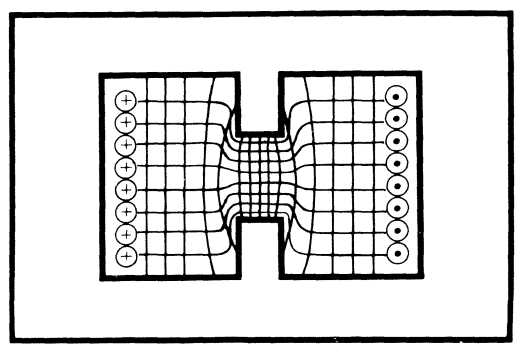


Figure 4.

Air Gap. In Figure 5, the field is concentrated further by adding ferrite pole pieces in the center of the winding, leaving a small gap, l_g. The total magnetic field remains the same if the ampere-turns are unchanged, but this field is all crowded into the small gap because of its low relative permeability of 1.0, compared to 3000 for the ferrite. From Equation 1: $H = NI/l_g$

Figure 5.



The energy density in the gap is easily calculated using Equation 4. Assuming that all of the energy in the system is stored in the gap, with uniform distribution, the total energy is found by multiplying the energy density by the volume of the gap (center-pole area, A_e, times the gap length, l_g) and further substituting Equations 3 and 1:

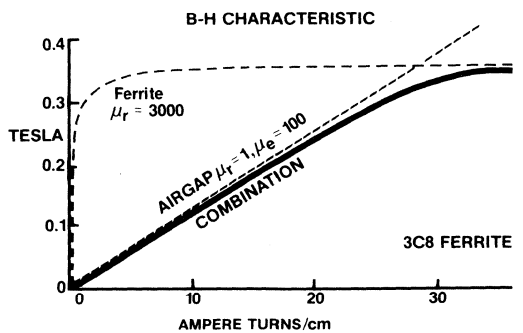
$$W = \frac{1}{2} B A_e H l_g = \frac{1}{2} \mu_o H^2 A_e l_g = \frac{1}{2} \mu_o N^2 I^2 \frac{A_e}{l_g} = \frac{1}{2} L I^2 \qquad (6)$$

$$L = \mu_o N^2 A_e / l_g \qquad (7)$$

As the first expression of Equation 6 shows, the total energy stored in the gap equals simply one-half the product of the total flux, BA_e, times the total magnetic field, Hl_e. The third expression of Equation 6 shows that the energy actually increases if the gap is made smaller with the same ampere-turns in the winding. This is because the total field is the same, so the field intensity, H, must increase. The flux density also increases proportional to H (Equation 3). The B-H product therefore changes inversely with the square of the gap size, so that even though the volume within the gap has decreased, the total energy is increased. Equation 7 shows this same relationship in terms of inductance increasing as the gap becomes smaller.

Referring again to Figure 5, the energy stored in the field outside the gap causes a few percent error in the calculation of stored energy and inductance. The error is small even though the volume of this field outside the gap is relatively large because the field is stretched out across the entire window. This reduces the field intensity and flux density, resulting in very low energy density in this region. Note that in practice, the gap is much smaller in relation to the window area than shown Figure 5.

Figure 6



B-H Characteristic. The composite B-H characteristic of a 3C8 power ferrite core with an air gap is depicted in Figure 6. The dash line on the left is the characteristic of the ferrite alone, with relative permeability of 3000 at 0.1 Tesla flux density. This characteristic is highly nonlinear, with saturation occuring at 0.35 Tesla at 100C. The dash line sloping linearly to the right is the air gap characteristic, with an actual relative permeability of 1.0 but an effective permeability of 100. The effective permeability is the average value that would be obtained as if the air gap was spread out over the entire length of the magnetic path through the core. In this case, the total magnetic path length is 100 times greater than the gap length, resulting in an effective permeability of 100.

The solid line represents the overall characteristic which is the sum of the magnetic fields in the ferrite and in the gap. Even though the distance through the ferrite is 100 times longer, its permeability is so large the composite characteristic is dominated by the gap. The effective permeability of the composite is

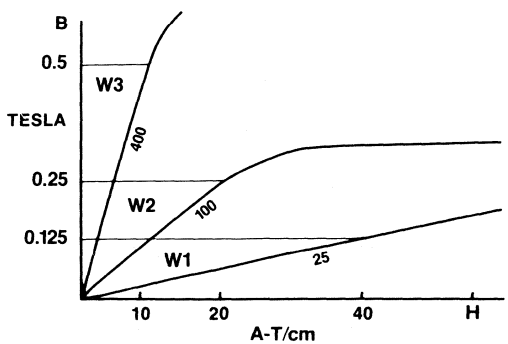
approximately 100, averaging the actual permeabilities of 1.0 in the gap and 3000 in the ferrite over the entire path length.

The energy storage at any operating point is the area to the left of the curve from the origin up to the operating point, equal to the integral HdB, which simplifies to BH/2 (Equation 4). The straightness of the composite characteristic validates the simplified approximation. The curves also show that the area to the left of the ferrite characteristic alone is very small, indicating that it is not possible to store significant energy in the ferrite because its high permeability results in a very small magnetic field component. This is ideal for a transformer, where energy storage is undesireable, but not for an inductor, whose main function is to store energy.

When it is necessary to store a significant amount of energy, this is usually accomplished by introducing a gap (air or other non-magnetic material) in series with the magnetic core. An apparently homogeneous moly-permalloy powder core actually stores its energy in a series of microscopic "gaps" in the binder which holds the moly-permalloy particles together. Since this distributed gap cannot actually be measured, the manufacturer measures and specifies the effective permeability of the gap averaged around the length of the core.

Alternative Characteristics. Assuming a specific energy storage design requirement for a flyback "transformer" (actually a coupled inductor) or filter inductor, Figure 7 shows several composite B-H characteristics, any of which could satisfy the inductor requirements. Each characteristic shown can provide the same energy storage as shown by the equal areas of the triangles at their respective operating points, assuming the same size cores.

Figure 7.



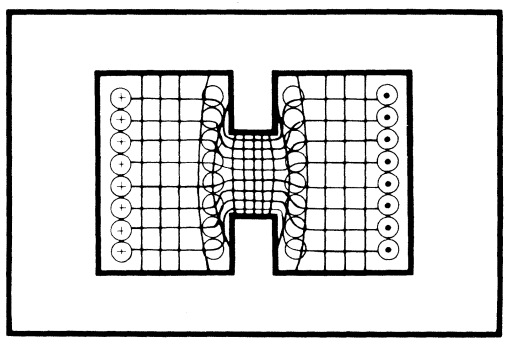
Core #1 is a ferrite core whose gap is 1/25 of the total magnetic path through the core, resulting in an effective permeability of 25. This core is underutilized, since it is operating at a flux density well below saturation. It could store much more energy, but that will never be required in this application. The magnetic field is much larger than necessary, resulting in excessive stray fields and leakage inductance. The winding must have many turns in order to generate this large field, resulting in smaller wire size and large DC copper losses.

Core #2 is <u>much</u> better. This is the same ferrite core as #1 with a much smaller gap (1/100 of the total path) for an effective permeability of 100. To store the same energy, field intensity is halved and flux density doubled. Stray energy and leakage inductance will be 1/4 as much as core #1, the number of turns is halved, the wire area can therefore double, and the DC losses are 1/4 of core #1. This core is almost fully utilized magnetically since it is operating close to saturation flux density.

Core #3 is the best of the three shown, because it is operating at twice the flux density of #2 and half the magnetic field intensity. This is a moly-permalloy powder core which saturates at 0.65 Tesla and has an effective relative permeability of 400. This provides another factor of four improvement in stray field, leakage inductance and DC winding losses.

<u>Coupled Inductors.</u> In Figure 8, an inner winding is added to the inductor of Figure 5. The inner winding is not carrying current, so the magnetic field is the same as Figure 5. Note that the flux lines associated with the energy in the field within the gap are linked 100% to both windings. This energy is therefore 100% coupled to both windings and represents mutual inductance. However, the flux lines associated with the relatively small energy stored <u>between</u> the two windings are linked only to the outer winding, and not at all to the inner winding. This energy represents leakage inductance, entirely in series with the outer winding. This can be confirmed by measuring the inductance of both windings independently. The outer winding will have the greater inductance by an amount equal to the leakage inductance.

Figure 8.

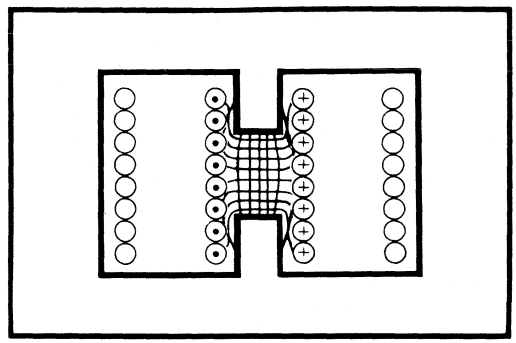


In a flyback type of switching power supply, current is built up in one of the two windings to store energy in the magnetic field. When this current is switched off, the mutual inductance causes the current to transfer to the other winding (and to the load). The same ampere-turns must continue to flow in order to maintain the energy in the mutual field.

In Figure 9, current has been transferred from the outer to the inner winding, with the same ampere-turns flowing. The field inside the inner winding is the same as in Figure 8, but the leakage inductance field between the two windings no longer exists. This energy does not just disappear when current transfers

from the outer to the inner winding. The leakage inductance tries to maintain the current in the outer winding. This causes a large reverse voltage swing which forces the leakage inductance energy to be absorbed by the external circuit. Usually the energy is dissipated in snubber or clamp circuits, causing increased losses. In addition, using a low clamp voltage (in order to protect the switching devices) will limit the reverse voltage swing and delay the transfer of current to the inner winding. This will hurt the regulation and efficiency of the switching power supply.

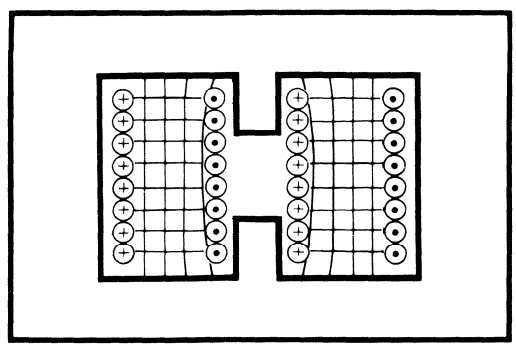
Figure 9.



When current is transferred from the inner winding back to the outer winding, the leakage inductance again opposes and delays the transfer. This time the circuit does not absorb energy, it must provide the energy required by the leakage inductance field between the windings.

If current is applied to both windings with equal and opposite ampere-turns as in Figure 10, the fields in the gap cancel. The only energy stored is in the leakage inductance field between the two windings. The leakage inductance can be measured directly by applying AC current to one winding and shorting the other. Equal and opposite ampere-turns are induced in the shorted winding, cancelling the mutual inductance field.

Figure 10.



Note that the leakage inductance field is determined by the number of turns and the dimensions of the volume between the two windings. The magnetic structure outside of these windings has very little influence on the leakage inductance. In fact the

leakage inductance is independent of the gap length, and it will decrease only slighly if the entire core is removed!

The leakage inductance can be approximated using Equation 7, substituting l_e, the length of the window that the winding is stretched across, for l_g. A_e is now the area of the cylindrical volume between the centers of the windings. From Equation 7, it is obvious how to decrease the leakage inductance:

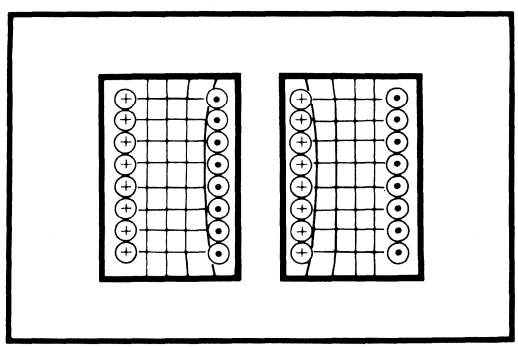
1. Increase l_e by stretching out the winding by using a core with a longer window. With the same total field (Hl = NI), this causes both the field intensity and flux density to decrease, dramatically reducing the leakage inductance energy while maintaining the same field and mutual inductance in the gap.

2. Reduce A_e. Use the thinnest possible insulation between windings. Since A_e includes approximately one-half of each winding, making the winding slimmer also helps significantly. Use the smallest possible wire size. Stretching out the windings (1. above) has the added benefit of making the winding slimmer.

3. Reduce the number of turns. With the same current, this must reduce the total field (Hl = NI). A smaller gap is required increasing H and B in the gap so as to maintain the desired mutual inductance energy. This approach is limited by B reaching saturation flux density. The smaller total field also results in less stray flux and EMI. Fewer turns also permit a slimmer winding, reducing the center-to-center area, A_e. DC losses are reduced. For a homogeneous core such as moly-permalloy, this approach is equivalent to using the highest possible permeability.

Transformer. Figure 11 is identical to Figure 10 except there is no gap in the core centerpost. Referring back to Figure 6, without a gap very little energy can be stored in the core because its high permeability acts like a magnetic "short circuit." A very tiny field will produce high flux density, so a small magnetizing current can cause the core to saturate. This characteristic is ideal for a transformer, not an inductor.

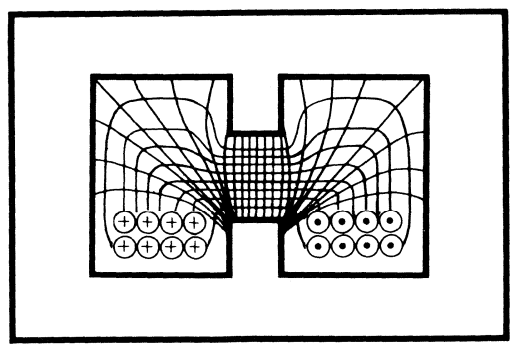
Figure 11.



In the transformer, the ampere-turns in all windings always sum up to zero (except for a relatively small magnetizing current which is a function of the integral of the volt-seconds applied to the windings according to Faraday's Law of Induction - Equation 5). The field caused by the ampere-turns of load current in the secondary windings is largely cancelled by the opposing field caused by primary winding current drawn from the power source. These two large opposing currents do create a significant field between the two windings as shown in Figure 11. The energy stored in this field represents leakage inductance, just as at did with the coupled inductor of Figure 10. For the same number of turns on the same size core, the leakage inductance value of the transformer of Figure 11 will be the same as the inductor of Figure 10 because the gap has no effect.

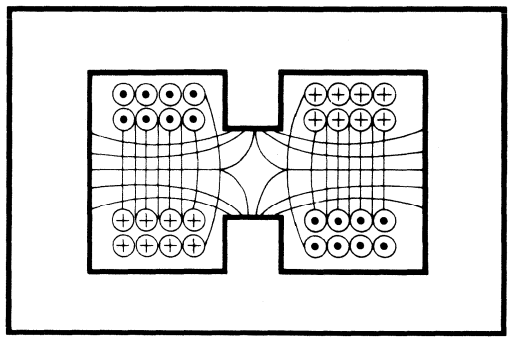
Bear in mind that for the transformer, the leakage inductance is effectively in series with the mutually coupled windings, and the energy stored in the leakage inductance is proportional to the square of the load currents. On the other hand, the magnetizing current represents a large value of inductance in parallel with the ideal mutually coupled windings. The small energy represented by this parallel inductance is stored in the core. This energy is a function of the volt-second integral of the voltage waveform applied to the windings and has absolutely no relation to load current.

Figure 12.



Side-by-Side Windings. Sometimes the windings are applied to the core in a side-by-side configuration, rather than one on top of the other. Figure 12 shows one winding of a side-by-side pair in a gapped core with the magnetic field caused by the same 8 ampere-turns. Note how the field in the gap is the same as before, and how the field extends through the entire volume of the window. This is neccessary so the flux lines can cross the window. (If the field did not extend across the window, the proportional flux lines would terminate, which they cannot - Flux Rule 2, page 2.)

Figure 13.



With the second winding added in Figure 13, and with opposing ampere turns in the two windings, the resulting field represents the leakge inductance energy. Compare this with Figure 10, the same situation with windings on top of each other.

In Figures 12 and 13, the fields of each winding conducting individually are symmetrical and equal. The total inductances of each winding (assuming equal turns) are identical. Exactly half the leakage inductance is in series with each winding, unlike Figures 9 and 10, becaused the windings are placed symmetrically with respect to the gap.

However, the amount of energy stored in the field of Figure 13 is very much greater than in Figure 10. This very undesirable result is because the same magnetic field is across the short dimension of the window rather than the long dimension as in Figure 10. This compresses the leakage inductance field, increasing the field intensity and flux density, and therefore increasing the stored energy. The leakage inductance in this winding configuration could easily be 10 or 15 times larger than in Figure 10.

Conclusion. A good understanding of the behavior of magnetic fields and their energy content, and their linkage to the windings that create the magnetic field, is essential to understanding the complete nature of inductors and transformers used in switching power supplies. Practical examples of transformer and inductor design are given in Sections M5 and M6.

POWER TRANSFORMER DESIGN

FOR SWITCHING POWER SUPPLIES Rev. 7/86

This design procedure applies to transformers used for coupling and isolation, in which energy storage is undesired. The 'transformers' used in Flyback circuits are actually coupled inductors used primarily to store energy and whose design procedure is covered in Section M6 of this manual.

Symbols, definitions, equations and various core and wire data used in this section are defined in Reference Sections M1, M2, and M3.

1. Determine the Flux Density Excursion: The first step in this design procedure is to define the flux density swing, ΔB, that will occur with normal steady-state operation. The transformer should be designed to operate with ΔB as large as possible, resulting in fewer turns in the winding, increased power rating and lower leakage inductance. In practice, ΔB is limited either by core saturation, B_{sat}, or core losses.

In most bridge, half-bridge and full-wave center-tap circuits, the transformer is symmetrically driven so that the flux swing is symmetrical around zero on the B-H characteristic. This allows a theoretical maximum ΔB of 2 times B_{sat}. In most single-ended circuits, such as the forward converter, the flux excursion is entirely within the first quadrant of the B-H characteristic, from B_r toward B_{sat}, limiting the theoretical maximum ΔB to ($B_{sat} - B_r$). This means that a larger transformer size is required for a given power output in single ended applications when ΔB is not limited by core losses (usually at frequencies below 50 - 100 kHz).

In voltage-fed circuits (which includes all of the commonly used buck regulator topologies), ΔB is determined by the volt-seconds applied to the primary, in accordance with Faraday's Law. With normal steady state operating conditions, the primary volt-seconds are constant, equal to $V_{in(min)}t_{on(max)}$ or $V_{in(max)}t_{on(min)}$, and the flux swing is also constant.

However, with simple duty cycle control method used by most control ICs, $V_{in(max)}$ may occur simultaneously with $t_{on(max)}$ during startup or after a sudden increase in load current. Under these transient conditions, if $V_{in(max)}$ is double $V_{in(min)}$, ΔB can be twice the steady-state value. This means the steady-state ΔB can only be half the theoretical maximum or the core will saturate under transient conditions. With volt-second control (voltage feed-forward) available in the UC1840 control IC, the maximum volt-seconds can be clamped to a level only slightly greater than normal. This permits larger flux swings and improves transformer performance.

B_{sat} for most power ferrites such as 3C8 material is above 0.3 Tesla (3000 Gauss). In push-pull voltage-fed applications ΔB is usually limited to 0.3 T. Core losses at 50 kHz will approach copper losses. Above 50 kHz, increased core losses will necessitate further reduction of ΔB.

In single-ended circuits without volt-second clamping, ($B_{sat} - B_r$) of 0.2 T under transient conditions permits a normal ΔB of only 0.1 T. Core losses at 50 kHz will be almost negligible with this small flux swing. With volt-second clamping, possible with the UC1840 control IC, a ΔB of nearly 0.2 T is acceptable, significantly reducing transformer size.

In current-fed circuits (all boost topologies and the Coupled Inductor, Current Driven Buck regulator), ΔB is governed by the volt-seconds on the secondary windings which are clamped to the output voltages. Since the volt-seconds are thus independent of input voltage variations, current-fed circuits can operate with ΔB close to theoretical maximum (except for core loss considerations) without the need for volt-second clamping.

At frequencies above 50 - 100 kHz, ΔB is usually limited by core losses.

2. Select the Core: The second step is to select a specific core that is able to support the required volt-seconds without saturating and with acceptable core losses and winding losses. This can be accomplished by an iterative process with trial solutions. However, equations (1A) and (1B) provide an approximation of the core area product, AP, required for the application. (AP = core window area A_W, times magnetic cross section A_e.) Equation (1A) applies when ΔB is limited by saturation and (1B) when limited by core losses. If uncertain which applies, solve both equations and use the largest resulting AP. From core catalog data or the core data given in Section M3, select a core whose AP exceeds the calculated value.

$$AP = A_W A_e = \left(\frac{P_{in}\, 10^4}{K_t\, K_u\, K_p\, 420\, \Delta B\, 2\, f_t} \right)^{1.31} = \frac{11.1\, P_{in}}{K\, \Delta B\, f_t}^{1.31} \quad cm^4 \qquad (1A)$$

$$AP = A_W A_e = \left(\frac{P_{in} \cdot 10^4}{120\, K\, 2 f_t} \right)^{1.58} \cdot (k_H f + k_E f^2)^{.660} \quad cm^4 \qquad (1B)$$

where $P_{in} = P_o/\eta$ = Power Output/Efficiency
$K_t = I_{in(DC)}/I_{p(rms)}$, Topology Factor
$K_u = A_W'/A_W$, Window Utilization Factor (0.40)
$K_p = A_p/A_W'$, Primary Area Factor
$K = K_t K_u K_c$
J = Current Density (420 A/cm²)
f_t = Transformer operating frequency
see Table I below and Section M2, page 2.

For most power ferrites, hysteresis coefficient $k_H = 4 \cdot 10^{-5}$, eddy current coefficient, $k_E = 4 \cdot 10^{-10}$.
Equations (1A) and (1B) assume that the windings occupy 40% of the window area, the primary and secondary winding areas are proportioned for equal power density and that winding and core losses result in a 30°C hot spot temperature rise with natural convection cooling.

TABLE I -- K Factors

		K	Kt	Ku	Kp
Forward Converter	SE/SE	0.141	0.71	0.40	0.50
Bridge/Half Bridge	SE/CT	0.165	1.0	0.40	0.41
Full Wave Center-Tap	CT/CT	0.141	1.41	0.40	0.25

NOTE: Throughout the following calculations:

Half-bridge -- V_{in} equals 1/2 the rail-to-rail input voltage.
C.T. Primary -- All primary references are to 1/2 the total primary.

3. Design the Windings: First, calculate the maximum total transformer loss using the core tentatively selected from its thermal resistance, R_T, and the maximum hot spot temperature rise, ΔT.

$$P_t = \Delta T / R_T \quad W \tag{2}$$

If the thermal resistance for the core used is not published, it may be calculated from the approximation:

$$R_T = 23\,AP^{-.37} \quad °C/W \qquad \text{(not for toroids)} \tag{3}$$

If the Area Product calculated by Eq. (1A) is greater than (1B), the flux swing is saturation limited. ΔB is the known value used in Eq. (1A).

If the flux swing is core loss limited, the design is optimized by assigning half the total loss to the windings and half to the core loss ($P_W = P_C = P_t/2$). ΔB is not yet known, but can be found by dividing the allowed core loss, P_C, by the core volume, V_e, and using this value to enter the core manufacturer's core loss curves. The resulting flux density is usually given as a peak value and must be doubled to obtain ΔB.

Calculate the minimum number of primary turns, N_p, required to support the normal volt-seconds.

$$t_{on(max)} = D_{max}/f_S = 0.5/f_t \quad \text{sec}$$

$$N_p > \frac{V_{in(min)}\, t_{on(max)}}{\Delta B\, A_e} \times 10^4 = \frac{5000\, V_{in(min)}}{\Delta B\, A_e\, f_t} \tag{4}$$

The primary to secondary turns ratio, n, is calculated for the lowest voltage secondary at min. V_{in} and max. duty cycle. V_f is the rectifier forward drop. The factor 0.9 allows for transistor storage/fall times:

$$n = \frac{N_p}{N_S} = \frac{0.9\,[V_{in(min)} - V_{CE(sat)}]\,D}{V_O + V_F} \tag{5}$$

Calculate the number of turns required for the lowest voltage secondary, and round up to the next larger integral number of turns:

$$N_S = \text{Integer}(N_p/n) \tag{6}$$

Recalculate the actual primary turns. If the new value of N_p is significantly larger than the minimum value in Eq. (4), a larger core may be required:

$$N_p = n\,N_S \tag{7}$$

Substitute the new value of actual primary turns into Eq. (4) and solve for the actual ΔB. Use this to find the core loss/cm³ from the core manufacturers' core loss curves. (ΔB is the peak-peak flux density swing which usually must be halved to obtain the peak flux density value used in most core loss curves.) Multiply by the core volume, V_e, to obtain the actual core loss, P_C.

Subtract the actual core loss, P_C, from the total transformer loss, P_t, to define the max. winding losses. Then multiply by primary area factor, K_p,

to obtain the max. allowed primary losses (half C.T. primary), P_p :

$$P_p = K_p(P_t - P_c) \quad \text{Watts} \tag{8}$$

The full load max. RMS primary current (half of C.T. primary) is:

$$I_{p(max)} = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(min)}\,K_t} \quad A \tag{9}$$

Calculate the maximum primary resistance (half of C.T. primary):

$$R_p = P_p/I_{p(max)}^2 \quad \Omega \tag{10}$$

Look up the mean length of each turn, ℓ_t, for the selected core, and using N_p from Eq.(7), calculate the resistance/cm of the (1/2) primary.

$$R_p/cm = R_p/(N_p\ell_t) \tag{11}$$

Enter the wire tables (Section M2) with this R_p/cm value and find the minimum required size and its copper area, A_X. Multiply by N_p to obtain the total primary copper cross-section area (half of C.T. primary). Compare with the area actually available for primary copper in the window.

$$A_p = N_pA_X \leq K_UK_pA_W \tag{12}$$

If A_p is larger than the available window area, then a larger core must be used and the procedure repeated from Eq. (2) (or a larger temperature rise must be accepted). If A_p is considerably smaller, it may be desireable to use a smaller core.

All windings should be operated at the same current density. This results in uniform power density throughout the windings for best utilization of the window area. Proportion the areas of each secondary conductor to the primary conductor area, A_X, according to the rms currents in each winding.

To avoid severe eddy current losses and to make winding easier, it may be necessary to use multiple paralleled turns of finer wire with equivalent total cross-section area. For high current secondaries, thin copper strip is often used. Refer to Section M2.

TRANSFORMER CORE AREA PRODUCT DERIVATION

The DC (average) component of the switching regulator input current, I_{in}:

$$I_{in} = P_{in}/V_{in}\ , \qquad P_{in} = P_o/\eta$$

Maximum RMS primary current, $I_{p(max)}$, occurs with minimum V_{in}. Topology Factor K_t relates the RMS primary winding current to the DC input current:

$$I_{p(max)} = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(min)}\,K_t} \qquad (A1)$$

The number of turns that will fill the available primary window area when operated at current density J depends upon the Window Utilization Factor, K_u, and the Primary Area Factor, K_p:

$$N_pI_p = A_pJ = K_uK_pA_wJ, \qquad N_p = K_uK_pA_wJ/I_p$$

Substituting for I_p from Equation (1):

$$N_p = V_{in(min)}\,K_t\,K_u\,K_p\,A_w\,J/P_{in(max)}, \qquad A_w = \frac{N_p\,P_{in(max)}}{V_{in(min)}\,K_t\,K_u\,K_p\,J} \qquad (A2)$$

From Faraday's Law:

$$E\,dt = N\,d\Phi$$

$$V_{in}\,t_{on} = N_p\,\Delta B\,A_e, \qquad A_e = \frac{V_{in(min)}\,t_{on(max)}}{N_p\,\Delta B}$$

Forward Converter: $t_{on(max)} = D_{max}/f_s = 0.5/f_s = 1/2f_t$
Bridge, Half Bridge, C.T.: $t_{on(max)} = D_{max}/f_s \simeq 1/f_s \simeq 1/2f_t$
ΔB is the total flux density swing during normal operation.

$$A_e = \frac{V_{in(min)}}{N_p\,\Delta B\,2\,f_t} \qquad (A3)$$

Combining (2) and (3):

$$AP = A_wA_e = \frac{P_{in(max)}}{K_t\,K_u\,K_p\,J_{max}\,\Delta B\,2\,f_t} \quad m^4 \qquad (A4)$$

To obtain Area Product in cm^4, use J in A/cm^2 and multiply result by 10^4.

For the case when the flux swing is saturation (not core loss) limited, it is assumed that core losses are negligible and all losses are in the windings. A maximum current density, J_{max}, of 420 A/cm^2 (2700 A/in^2) will cause a 30°C hot spot temperature rise with natural convection cooling for a core with area product of 1 cm^4. Maximum current density decreases as core size increases because the heat dissipating surface area increases less than the heat producing volume. Empirically:

$$J_{30} = 420\,AP^{-.240} \qquad A/cm^2 \qquad (A5)$$

Substituting (A5) into (A4), the saturation limited area product is:

$$AP = A_w A_e = \left(\frac{P_{in}\ 10^4}{K_t\ K_u\ K_p\ 420\ \Delta B\ 2\ f_t} \right)^{1.31} \quad cm^4 \qquad (A6)$$

In the core loss limited case, start with Equation (A4). Again, a 30°C hot spot temperature rise is assumed, but half the losses are apportioned to the core, half to the windings. Assume 15°C rise from core losses, 15°C from the windings operating at a current density of:

$$J_{15} = 297\ AP^{-.240} \quad A/cm^2 \qquad (A7)$$

J_{15} will be substituted for J_{max} in (A4). First, find ΔB value that will result in 15°C rise from core losses. Core losses/cm³ can be calculated from the following empirical formula:

$$P_C/cm^3 = \Delta B_m^{2.4}(k_H f + k_E f^2) \qquad (A8)$$

Temperature rise depends upon the core losses/cm³ as well as the core volume and thermal resistance:

$$\Delta T = 15°C = R_T V_e (P_C/cm^3) \qquad (A9)$$

Thermal resistance and core volume relate empirically to area product:

$$R_T \cong 23\ AP^{-.37} \quad °C/W \qquad (A10)$$

$$V_e \cong 5.7\ AP^{.68} \quad cm^3 \qquad (A11)$$

Substitute (A8), (A10), and (A11) into (A9) and solve for ΔB_m:

$$\Delta B_m = \frac{0.405 \cdot AP^{-.129}}{(K_H f + K_E f^2)^{.417}} \qquad (A12)$$

Finally, substitute (A7) and (A12) into (A4) and solve for the core loss limited Area Product requirement;

$$AP = A_w A_e = \left(\frac{P_{in} \cdot 10^4}{120\ K\ 2 f_t} \right)^{1.58} \cdot (k_H f + k_E f^2)^{.660} \quad cm^4 \qquad (A13)$$

APPORTIONMENT OF TRANSFORMER WINDINGS:

I = RMS primary or secondary current in single-ended winding.
I' = I/1.414 = RMS current in one side of center-tap winding.

A_w = Total Window Area in core for conductors and insulation.
A_wK_u = Window area utilized by actual conductors. Typical K_u = .35
$A_wK_uK_p$ = Area of primary (1/2 C.T.)

Total conductor area equals the sum of the individual windings:

$$A_wK_u = A_1 + A_2 + \ldots A_n$$

The conductor areas, A_n, required for all windings to operate at the same current density, J, (to obtain uniform power density) are:

$$A_n = N_nI_n/J \quad \text{(single ended winding)}$$

$$A_n = N_nI_n'/J = N_nI_n/1.414J \quad \text{(each side of C.T. winding)}$$

Primary and Secondaries both Single-Ended (Forward Converter):

$N_pI_p = N_sI_s$, $\quad N_pI_p/J = N_sI_s/J$, $\quad A_p = A_s$

$A_wK_u = A_p+A_s = 2A_p$, $\quad A_p = A_s = 0.5A_wK_u$, $\quad K_p = 0.5$

Primary Single-Ended, Secondaries C.T. (Bridge, Half-bridge):

$N_pI_p = N_{s1}I_s = N_{s2}I_s$

$A_p = N_pI_p/J$, $\quad A_{s1} = A_{s2} = N_sI_s'/J = N_sI_s/1.414J = N_pI_p/1.414J = A_p/1.414$

$A_wK_u = A_p+A_{s1}+A_{s2} = A_p + 2A_p/1.414 = A_p(1+1.414)$

$A_p = .414A_wK_u$, $\quad A_{s1} = A_{s2} = .293A_wK_u$, $\quad K_p = .414$

Primary and Secondaries both Center-Tap:

$N_{p1}I_p = N_{p2}I_p = N_{s1}I_s = N_{s2}I_s$

$A_{p1} = A_{p2} = N_pI_p'/J = N_pI_p/1.414J$

$A_{s1} = A_{s2} = N_sI_s'/J = N_sI_s/1.414J = N_pI_p/1.414J$

$A_wK_u = 2A_p+2A_s = 4A_p$

$A_{p1} = A_{p2} = A_{s1} = A_{s2} = .25A_wK_u$, $\quad K_p = .25$

FILTER INDUCTOR AND FLYBACK TRANSFORMER DESIGN FOR SWITCHING POWER SUPPLIES

Lloyd H. Dixon, Jr.

This design procedure applies to magnetic devices used primarily to store energy. This includes inductors used for filtering in Buck regulators and for energy storage in Boost circuits, and "flyback transformers" (actually inductors with multiple windings) which provide energy storage, coupling and isolation in Flyback regulators. The design of true transformers used for coupling and isolation in circuits of the Buck and Boost families (in which energy storage is undesired) is covered in Section M5 of this manual.

Symbols, definitions, basic magnetic design equations and various core and wire data used in this section are defined in Reference Sections M1, M2, and M3, and in Appendix A at the end of this section. The specific equations used in this design procedure are derived in Appendix B. The Standard International system of units (rationalized MKS) is used in developing the equations, but dimensions have been converted from meters to centimeters.

All circuit values such as inductance, peak and rms currents and turns ratios must be defined before beginning the magnetics design procedure.

A practical design example of a flyback transformer design using this procedure is in the paper: "150 Watt Flyback Regulator".

Step 1. Select the Core Material and Configuration

Ferrite is the most widely used core material for commercial applications (see Section M3). Molybdenum-permalloy powder toroidal cores have higher losses, but they are often used at switching frequencies below 100 kHz when the flux swing is small -- in filter inductors and flyback transformers operated in the continuous mode. Powdered iron cores are sometimes used, but they are generally either too low in permeability or too lossy for practical use in switching power supply applications above 20 kHz.

The basic magnetic materials above all have very high permeabilities (μ_r = 3000 - 100,000) and cannot therefore store much energy. This is good for a true transformer, but not for an inductor. The large amount of energy that must be stored in a filter inductor or flyback transformer is in fact stored in an air gap (or other non-magnetic material with $\mu_r = 1$) in series with the high permeability core material. In moly-permalloy and powdered iron cores the energy storage gap is actually in the non-magnetic binder holding the magnetic particles together. This distributed gap cannot be measured or specified directly, so the equivalent permeability of the overall composite core is specified instead.

Step 2. Determine the Peak Flux Density

In the following procedure, inductance and current values are referred to the primary. (The single winding of a simple inductor will also be called the primary.) The inductance, L, required and the peak short-circuit

inductor current, I_{pk}, are dictated by the circuit application. I_{pk} is set by the current limiting circuit. Together, these define the absolute maximum inductor energy, $(LI_{pk}^2)/2$, that the inductor must be designed to store (in the gap) without saturating the core and with acceptable core losses and copper losses.

The maximum peak flux density, B_{max}, that will occur at I_{pk} must be defined. The inductor should be operated at B_{max} as large as possible to achieve the smallest possible gap capable of storing the required energy. This minimizes the winding turns, eddy current losses, and inductor size and cost.

In practice, B_{max} is limited either by core saturation, B_{sat}, or by core losses. Core losses in ferrite are proportional to frequency and to the approximate 2.4th power of the peak-to-peak flux density swing, ΔB, during each switching cycle. In an inductor designed to operate in the continuous current mode (such as a buck regulator filter inductor or a continuous mode flyback transformer), core losses are usually negligible at frequencies below 500 kHz because ΔB_m is a small fraction of the DC flux level. In these cases, B_{max} can be almost equal to B_{sat}, with a small safety margin. B_{sat} for most power ferrites such as 3C8 material is above 0.3 Tesla (3000 Gauss), and B_{max} of 0.28 - 0.3 Tesla may be tentatively chosen.

In an inductor designed to operate in the discontinuous mode, flux density swings all the way from zero to B_{max} (flux remnance is negligible because of the gap). Thus the maximum flux density swing, ΔB_m, equals B_{max}. In the discontinuous mode, especially at high frequencies, ΔB_m (and B_{max}) will usually be limited by core losses so that B_{max} will be much less than B_{sat}.

Step 3. Determine Core Size

The core used must be able to store the required peak energy in a small gap without saturating and with acceptable core losses. It must contain the required turns with acceptable winding losses. Core selection can be made through an iterative process involving trial solutions, but Equations 1A and 1B provide an approximation of the core area product, AP, required for the application. (AP = window area A_W, times magnetic cross section A_e). Select the smallest core available from catalog data whose area product exceeds the calculated value.

Equation 1A applies when B_{max} is limited by saturation and Equation 1B when limited by core losses. It may be necessary to try both equations, using the largest resulting AP value. First, the saturation limited case. (Refer to Appendix A for symbol definitions):

(1A) $$AP = A_W A_e = \left(\frac{L\, I_{pk}\, I_{FL} \cdot 10^4}{420\, K\, B_{max}} \right)^{1.31} \quad \text{cm}^4$$

With L in Henries, B in Tesla, K = see Table I

Equation 1A is based on copper losses at current density J_{max} resulting in a hot spot temperature rise (at the middle of the center-post) of 30°C. J_{max} is a function of core size:

(2A) $$J_{30} = 420\, AP^{-.240} \quad \text{A/cm}^2$$

For the core loss limited case, Equation 1B is also based on a hot spot temperature rise of 30°C, but only half due to copper losses and half core losses.

(1B) $$AP = A_W A_e = \left(\frac{L\,\Delta I_m\, I_{FL}\cdot 10^4}{130\,K}\right)^{1.58} \cdot (k_H f + k_E f^2)^{.660} \qquad cm^4$$

For most power ferrites, hysteresis coefficient $k_H = 4\cdot 10^{-5}$, eddy current coefficient, $k_E = 4\cdot 10^{-10}$. Equation 1B is based on operating at a current density, J_{max}, contributing 15°C to the hot spot temperature rise:

(2B) $$J_{15} = 297\,AP^{-.240} \qquad A/cm^2$$

Multiple windings, if any, should be proportioned to operate at the same rms current density to assure uniform power distribution in the windings.

TABLE I -- K Factors

	K_u	K_p	$K=K_u\cdot K_p$
Continuous Buck, Boost Inductor:	0.7	1.0	0.7
Discontinuous Boost Inductor:	0.7	1.0	0.7
Continuous Flyback Transformer:	0.4	0.5	0.2
Discontinuous Flyback Transformer:	0.4	0.5	0.2

Window utilization factor K_u of 0.4 for the flyback transformers in Table I includes insulation to meet VDE line isolation requirements, but does not include a bobbin. K_u should be halved for toriodal cores. The primary area factor K_p of 0.5 is for half of the copper area apportioned to the primary, half to the secondary.

4. Define N

The minimum number of turns is next calculated:

(3A) $$N_{min} = \frac{L\,I_{pk}}{B_{max}A_e}\cdot 10^4$$ when B_{sat} limited

(3B) $$N_{min} = \frac{L\,\Delta I_m}{\Delta B_m A_e}\cdot 10^4$$ when core loss limited

The actual number of turns is the next possible integer value greater than N_{min}. In a flyback transformer with multiple windings, the primary turns may be constrained to specific multiples such as 22, 44, 66, 88 etc. because of turns ratio considerations. In this case if N_{min} is 36 turns, the smallest possible N is 44 turns. It may be that these additional turns above the minimum will not fit the core unless the actual core area product is sufficiently greater than the minimum AP calculated in Equation 1. For the same inductance, the larger N also results in a B_{max} or ΔB_m less than the original limit, and the core losses will be less. Using Equation 3B with the larger value of N and the actual ΔI_m of the application, calculate the smaller value of ΔB_m and use this to find the actual core losses, P_C, from the core manufacturers core loss tables.

5. Calculate the Gap

The gap length is calculated using the classic inductance formula:

(4A) $$\ell_g = \frac{\mu_o \mu_r N^2 A_e}{L} \cdot 10^{-2} \qquad \text{cm } \mu_r = 1$$

With Ferrite E-E or pot cores, the gap should be in the center-post only, which requires grinding it to size if not available as a standard part. The grinding operation may be avoided by shimming the core halves apart by approximately half the calculated gap length. This puts half the gap in the center-post, with the other half in the outer legs of the core, assuming the cross section area of the combined outer legs equals the centerpost area. The shimming technique results in considerable external magnetic field -- a possible source of EMI. The effective gap is difficult to calculate and it must be adjusted empirically.

In toroidal cores, the gap is distributed between magnetic particles around the entire core, and is inaccessible. Instead of gap length, the core manufacturer specifies the *equivalent* relative permeability as though the core were made entirely of a homogeneous magnetic material. ℓ_e is the effective magnetic path length around the entire core:

(4B) $$\text{Max } \mu_r = \frac{L\, \ell_e}{\mu_o N^2 A_e} \cdot 10^2$$

3. Design the Windings

Calculate the maximum total power dissipation, P_{max}, based on the maximum hot spot temperature rise, ΔT, and core thermal resistance, R_T. Subtract the previously calculated core losses, P_C, to determine the maximum winding losses, P_{Cu}:

(5) $$P_{Cu} = \Delta T / R_T - P_C \quad \text{W}$$

If thermal resistance of the core used is not known, calculate it from the approximation:

$$R_T = 23\, AP^{-.37} \quad ^\circ\text{C/W}$$

Primary winding loss, P_p, obviously equals P_{Cu} in single winding inductors, but P_p equals $P_W/2$ with multiple windings. Calculate the maximum primary resistance, using the maximum rms primary current:

(6) $$R_p = P_p / I_F L^2 \quad \Omega$$

Divide R_p by the total length of the primary winding to obtain the maximum resistance/cm of the primary conductor:

(7) $$R_{p/cm} = R_p / (N\, \ell t)$$

Enter the wire tables with this $R_{p/cm}$ value and find the minimum required wire size and its copper area, A_x. Check the total primary conductor area

with N wires to make sure it will fit the area available in the core window:

(8) $$A_P = N A_X \leq K_U K_P A_W$$

If A_P is too large, then a larger core must be used and the procedure repeated from Equation 3A or 3B (or a larger temperature rise must be accepted). If A_P is considerably smaller, it may be desirable to use a smaller core. In multiple winding inductors, do *not* use a wire size larger than Equation 7 requires, or leakage inductance and eddy current losses will increase.

The secondary conductor areas are proportioned to the primary conductor area according to the rms currents in each winding, so that the current densities are the same in all windings.

To obtain good coupling between multiple windings, *each winding* must stretch across the entire breadth of the window (the longer dimension), allowing suitable creepage distance at each end. If the turns in any winding, closely wound, do not extend across the entire available winding breadth, they should be spread out. However, this poorly utilizes the window area and results in high eddy current losses if the wire diameter approaches twice the penetration depth. It is much better to replace a single large diameter conductor with several paralleled conductors which can occupy the available area much more compactly and also reduce eddy current losses.

For example, suppose a tightly wound winding of N turns of diameter D and area A occupies only half the available winding breadth. The height of the winding layer equals D. If this winding is spread out, the coupling to other windings will greatly improve, but the height is still D and it occupies twice the volume that it should. If the single wire is replaced by four wires paralleled, each with area $A/4$, diameter $D/2$ and N turns (close wound adjacent to one another as though they were one wire), they will extend exactly across the winding breadth, with a winding height of only $D/2$, and the eddy current losses and leakage inductance will be greatly reduced. The ultimate of this technique is to use thin copper strip for high current windings that have only one or two turns.

The total rms current, I, in any winding usually has a DC component and an AC component according to the relationship:

(9) $$I^2 = I_{DC}^2 + I_{AC}^2$$

The losses in any winding as calculated earlier are caused by the total rms current flowing through the DC resistance of the winding. However, the AC resistance may be much greater than the DC resistance because skin effect and proximity effect cause the AC current component to flow in only a small portion of the total wire area. The ratio R_{AC}/R_{DC} is the resistance factor, F_R. Eddy current losses result from the *rms AC current component only*, I_{AC}, flowing through the higher effective AC resistance of the wire.

In filter inductors used in buck regulators, Eddy current losses are seldom a problem because the AC current component is so small. I_{AC}^2 is typically 1/200 of I_{DC}^2, so F_R would have to be 200 for the eddy current losses to equal the low frequency losses. In continuous mode flyback transformers,

the AC component of total inductor current is small and the core losses are therefore small. However, the AC component in each winding is quite large because the current switches back and forth from primary to secondaries, and eddy current losses are usually significant.

The proximity effect is caused by the AC component of the magnetic field that exists between primary and secondary windings. This AC field induces circulating AC currents within each conductor, adding to the DC current in some areas and subtracting in others and greatly increasing the losses. This effect is combated by using paralleled fine wires or thin copper strips which reduce the circulating currents, and by reducing the magnetic field strength. The latter is accomplished by using a wider window to stretch the windings out, by reducing the number of layers in the windings, and by interleaving -- putting half the primary turns inside and half outside the secondaries. The paper "150 Watt Flyback Regulator" gives a practical example of handling these problems.

The thermal resistance with natural convection cooling, R_T, upon which the hot spot temperature rise depends is probably the weakest approximation used in this procedure. R_T is strongly influenced by the shape of the enclosure in which the transformer is mounted, size and location of cooling vents, horizontal vs. vertical mounting surfaces (chimney effect), and obviously by forced air. As a final check, it is a good idea to attach a fine wire thermocouple to the middle of the centerpost and check the temperature rise under conditions approximating the application.

APPENDIX A. SYMBOL DEFINITIONS

International Standard (SI) units are used except dimensions are converted from meters to centimeters. In flyback transformers or multiple winding inductors, symbols refer to primary winding values.

General:

I_{FL}	total rms primary current at full load
I_{pk}	peak short circuit primary current
I_m	maximum continuous peak-to-peak primary current swing
L	primary winding inductance, Henries
P_{MAX}	total power dissipation
R_T	hot spot thermal resistance, natural convection
ΔT	hot spot temperature rise
AP	core area product = $A_w A_e$, cm^4

Winding Parameters:

A_w	total winding window area in core, cm^2
A_{cu}	total conductor area - all windings
A_p	conductor area of primary winding = $N A_X$
A_X	conductor area of one primary turn
J_{max}	maximum flux density, A/cm^2
K_u	window utilization factor = A_{cu}/A_w
K_p	primary factor = A_p/A_{cu}
K	winding factor = $K_u K_p$
ℓt	avg. length of 1 turn (MLT), cm
n	turns ratio
N	number of turns
P_{cu}	winding losses

Core Parameters:

A_p	Conductor area of primary winding, cm^2
A_e	effective center-post area
B_{sat}	saturation flux density, Tesla
B_{max}	maximum peak flux density
ΔB_m	maximum peak-to-peak flux density swing
k_H	core hysteresis loss coefficient
k_E	core eddy current loss coefficient
ℓg	gap length, cm
μ_o	permeability of free space = $4\pi \cdot 10^{-7}$ (SI units)
μ_r	relative permeability
P_C	core losses
V_e	core volume

APPENDIX B. DERIVATION OF EQUATIONS

International Standard (SI) units are used in the initial development of these equations, but dimensions are later changed from meters to centimeters. All values are referred to the primary winding.

Circuit energy equals magnetic energy stored in the gap:

(B1) $$\frac{1}{2} L I^2 = \frac{1}{2} B H A_e \ell_g$$

Ampere's Law applied to the nearly linear field within the gap:

(B2) $$N I = H \ell_g$$

Substitute $H\ell_g$ into (B1) and simplifying:

(B3) $$L I = B A_e N$$

Solve for N:

(B3A) $$N = \frac{L I}{B A_e} = \frac{L I_{pk}}{B_{max} A_e}$$ when B_{sat} limited

(B3B) $$N = \frac{L \Delta I}{\Delta B A_e} = \frac{L \Delta I_m}{\Delta B_m A_e}$$ when core loss limited

The primary ampere-turns equals the current density times the total primary conductor area:

$$N I = A_p J = J A_w K$$

(B4) $$N = \frac{A_w J K}{I} = \frac{A_w J_{max} K}{I_{FL}}$$

For the saturation limited case, equating N in (B3A) and (B4):

$$\frac{A_w J_{max} K}{I_{FL}} = \frac{L I_{pk}}{B_{max} A_e}$$

Solve for Area Product and convert dimensions (only) to centimeters:

(B5) $$AP = A_w A_e = \frac{L I_{pk} I_{FL} \cdot 10^4}{J_{max} K B_{max}} \quad cm^4$$

In the case where core operation is saturation limited, core losses are not dominant and the windings are operated at a current density that will produce a 30°C rise with natural convection cooling, from practice:

(B6) $$J_{30} = 420\, AP^{-.240} \quad A/cm^2$$

Substitute (B6) into (B5) and solve for Area Product:

(B7) $$AP = A_W A_e = \left(\frac{L\, I_{pk}\, I_{FL} \cdot 10^4}{420\, K\, B_{max}}\right)^{1.31} \quad cm^4$$

In the core loss limited case, equate (B3B) and (B4) and convert dimensions to centimeters:

(B8) $$AP = A_W A_e = \frac{L\, \Delta I_m I_{FL} \cdot 10^4}{J_{max} K\, \Delta B_m} \quad cm^4$$

Assume 15°C temperature rise contribution from core losses, 15°C from the windings operating at a current density of:

(B9) $$J_{15} = 297\, AP^{-.240} \quad A/cm^2$$

J_{15} will be substituted for J_{max} in (B8). First, find ΔB_m value that will result in 15°C rise from core losses. Core losses/cm³ can be calculated from the following empirical formula:

(B10) $$P_C/cm^3 = \Delta B_m^{2.4}(k_H f + k_E f^2)$$

Temperature rise depends upon the core losses/cm³ as well as the core volume and thermal resistance:

(B11) $$\Delta T = 15°C = R_T V_e (P_C/cm^3)$$

Thermal resistance and core volume are related empirically to area product:

(B12) $$R_T \cong 23\, AP^{-.37} \quad °C/W$$

(B13) $$V_e \cong 5.7\, AP^{.68} \quad cm^3$$

Substitute (B10), (B12), and (B13) into (B11) and solve for ΔB_m:

(B14) $$\Delta B_m = \frac{0.405 \cdot AP^{-.129}}{(K_H f + K_E f^2)^{.417}}$$

Finally, substitute (B9) and (B14) into (B8) and solve for the core loss limited Area Product requirement;

(B15) $$AP = A_W A_e = \left(\frac{L\, \Delta I_m\, I_{FL} \cdot 10^4}{120\, K}\right)^{1.58} \cdot (k_H f + k_E f^2)^{.660} \quad cm^4$$

COUPLED FILTER INDUCTORS IN MULTIPLE OUTPUT BUCK REGULATORS

PROVIDE DRAMATIC PERFORMANCE IMPROVEMENT

Introduction: When switching power supplies of the buck family (forward converter, full and half bridge, etc.) have more than one output as shown in Figure 1, separate filter inductors (L1,L2) are normally used in each output. These independent inductors hurt performance by decoupling and isolating the outputs from each other. Dynamic cross regulation is very poor and several other major problems are created because of the independent inductors. These problems are virtually eliminated if the inductors are coupled to each other by winding their separate coils on a single, common core [1].

Coupled filter inductors can provide additional benefits. Dramatic reduction in filter capacitance can be achieved by ripple current steering. Also, minimum load requirements can be reduced or even eliminated.

The coupled inductor technique is almost a panacea -- designers who have mastered it are nearly unanimous in their acclaim. Its benefits far outweigh the few difficulties involved.

Circuit Analysis with Independent Inductors: The 180 Watt forward converter of Figure 1 has a 5V output and a 15V output (actually 15.8V intended to be post-regulated to 15V). A buck-derived regulator operated in the continuous inductor current mode, the DC output voltages must equal the time averaged voltages on the input side of their respective filter inductors. Using output #1 for example, with duty cycle D and with $V_{D1A} = V_{D1B} = V_{D1}$:

$$V_{o1} = (V_{in1}-V_{D1A})\cdot D - V_{D1B}\cdot(1-D) = V_{in1}\cdot D - V_{D1} \qquad (1)$$

Note that there is always one rectifier in series with each inductor winding. As shown in (1), this results in a one-diode drop offset voltage from the ideal buck regulator relationship: $V_o = V_{in}\cdot D$. This has the same effect as single rectifier located in series with the output side of the inductor. Considering both outputs, the diode drop offset will be a larger proportion of the 5V output than the offset in the nominal 15V output. To correct for this offset error, the transformer turns ratio must differ slightly from the desired output voltage ratio.

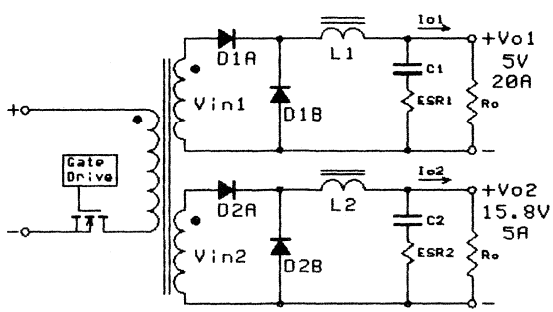


Figure 1. Forward Converter with Two Outputs

A well-designed control loop taken from the 5V output will provide good line regulation for both outputs and good load regulation for the controlled 5V output. The DC cross-regulation between the 5V and 15V outputs with load changes will be reasonably good if the transformer secondaries are tightly coupled and wiring inductance is minimized. Rectifier dynamic resistances and temperature coefficients are also significant factors in DC cross-regulation.

Disadvantages of Independent Inductors:

1. Dynamic cross-regulation is very poor. Output voltages will temporarily diverge from their DC levels when transient load changes occur. For example, a sudden load increase on the 15V output will cause its voltage to drop. This deviation must propagate through the high series impedance of inductor L2, the low shunt impedance of the input voltage source or free-wheeling rectifiers, and the high impedance of L1 in order to reach the controlled 5V output. As a result, the control loop is dynamically insensitive to load changes at the 15V output. It will keep the 5V output constant, but with large changes in load current, the 15V output will drop as much as 4 or 5 volts and take tens or hundreds of milliseconds to recover.

2. Minimum load requirements. Buck regulators are almost always designed to operate in the continuous inductor current mode, where the output voltage equals the average value of the chopped input voltage waveform, and the average inductor current equals the load current. A critical minimum load current must be sustained on each output, amounting to 1/2 the peak-peak ripple current through its filter inductor. Otherwise the inductor current tries to become negative at each minimum peak of the ripple current waveform, but it cannot because of the series rectifiers. The mode of operation becomes discontinuous and DC cross-regulation becomes very poor -- output voltages may diverge as much as 200-300%.

3. Each output should have independent current limiting to prevent saturation of the independent filter inductors under overload conditions.

4. Loop gain irregularities will occur because of interaction between the multiple outputs. With the transformer secondaries normally closely coupled, all outputs in the small-signal loop gain model are driven in parallel at the input of their respective filter inductors. One output is sensed for closed loop control. This controlled output is shunted by all the other outputs at the common driving point. The LC filters of these shunt outputs soak up much of the source current at their respective series resonant frequencies, causing reduced gain and significant phase shifts in the controlled output at these frequencies. This effect is especially severe with current mode control because of its characteristic high impedance at the driving point.

The Coupled Filter Inductor Circuit Approach: Refer again to the circuit of Figure 1, but consider that windings L1 and L2 are tightly coupled together on the same core. It is also vital that inductor windings L1 and L2 have exactly the same turns ratio as transformer secondary windings 1 and 2. This will be explained shortly.

From a DC standpoint, performance is identical to that described on the first page for independent inductors. Equation (1) applies, and the diode offset voltage problem and DC cross-regulation considerations are exactly the same.

For a specific example, assume:

$V_{D1A} = V_{D1B} = V_{D1} = 0.6V$ (Schottky); $V_{D2A} = V_{D2B} = V_{D2} = 1.0V$ (UES)

Duty cycle, D = 0.4; $V_{o1} = 5V$; Turns ratio, n = N2/N1 = 3:1

The resulting circuit values apply with either independent or coupled inductors. Note how the disproportionate effect of the diode drops pushes the 15V output to 15.8 V:

$V_{in1} = (V_{o1}+V_{D1})/D = 5.6V/0.4 = 14Vpk$; $V_{in2} = V_{in1} \cdot n = 14 \cdot 3 = 42Vpk$

$V_{o2} = V_{in2} \cdot D - V_{D2} = 42 \cdot 0.4 - 1.0 = 15.8V$ (for post regulation to 15V)

During the time when the power MOS switch is ON:

$V_{L1} = V_{in1}-V_{D1}-V_{o1} = 14-0.6-5 = 8.4V$; $V_{L2} = 42-1-15.8 = 25.2V$

While the switch is OFF, the "B" rectifiers freewheel the inductor current:

$V_{L1} = -V_{D1}-V_{o1} = -0.6-5 = -5.6V$; $V_{L2} = -1-15.8 = -16.8V$

Note that during both the ON and OFF times, V_{L2} is always exactly 3 times V_{L1} (because the transformer turns ratio is 3:1 and $(V_{o2}+V_{D2})/(V_{o1}+V_{D1})$ is also 3:1). Therefore, the coupled inductor windings must also have the same 3:1 turns ratio or there will be a conflict between V_{L1} and V_{L2}, which will cause a very large ripple current to circulate back and forth between the two output circuits. This will show up as a large ripple voltage across the highest impedance element in the circuit -- usually the output capacitor ESR, resulting in output ripple voltage much greater than expected. To prevent this from occurring, the transformer secondaries and corresponding inductor windings must have identical turns ratios.

Additional Problems and Limitations with the Coupled Inductor: If the "A" and "B" rectifiers in any output do not have identical forward drops, a voltage conflict is created similar to that caused by turns ratio inequality but much less severe. With tightly coupled inductor windings, output ripple voltage will increase by the amount of the rectifier mismatch. To solve this problem, it is not necessary to match each rectifier pair. A small amount of uncoupled leakage inductance or wiring inductance will provide enough series impedance to limit the mismatch induced ripple current. The corresponding ripple voltage will appear across the leakage inductance rather than at the output. As little as 2% leakage inductance will accomplish this purpose (it's hard to get much less than this). Try not to exceed 10% leakage inductance or dynamic cross-regulation will be impaired and spurious resonant conditions will be created.

Note that it is not necessary for the rectifier forward drops in one output to equal those in other outputs. Rectifier inequality between outputs causes a DC output voltage offset error, but does not increase ripple.

In addition, the timing of the waveforms across the transformer and coupled inductor windings must be identical in all outputs. Otherwise, voltage conflicts will occur during the times that the waveforms differ, causing very large current spikes to circulate between the outputs at these times. This means that independent secondary-side pulse width modulation cannot be used with coupled output inductors, ruling out the use of magnetic amplifier or Bisyn® PWM synchronous rectifier techniques for independent output regulation.

Advantages of the Coupled Filter Inductor:

1. AC cross-regulation is excellent because all outputs are dynamically coupled.

2. Large signal overshoot/undershoot is reduced because all outputs absorb or provide energy as necessary to support any output load change.

3. Although each output still requires a minimum load current greater than 1/2 the ripple current, the consequences of violating the critical minimum load current are less severe than with uncoupled inductors -- a 10 to 30% output voltage divergence vs. 200 to 300%

4. Simplified current limiting. A single primary side current limit will prevent inductor saturation, regardless of which output is overloaded.

5. Loop gain irregularities are eliminated because the coupled inductor is dynamically in common with all outputs combining them into a single circuit with one resonant frequency (unless leakage inductance is too large).

6. The single filter inductor is lower in cost and has smaller volume and mounting area compared with independent inductors.

Some Important Additional Advantages:

7. The critical minimum load current required for each output can be adapted to suit the application. Most of the ripple current can be steered to the output with the most minimum load power, thereby reducing minimum load requirements on the other outputs.

8. Output filter capacitor size and cost can be reduced considerably by steering most of the ripple current to the highest voltage output, where capacitors are much more effective. This is because at a given frequency and power level, the filter capacitor impedance needed for a given % output ripple voltage increases with the output voltage squared. (How to steer the ripple current will be explained shortly.)

For example, if the filtering burden is placed on the 15V output by steering the ripple current there, filter capacitor impedance can be 3^2 or 9 times larger than needed at the 5V level -- for an electrolytic capacitor, ESR can be 9 times larger, and ESR is inversely proportional to volume, regardless of voltage rating. For a ceramic or film capacitor, 1/9 the C value is required, and C is proportional to volume and independent of voltage below 50-100V. In either case, by steering the ripple current to the 15V output instead of the 5V, the filter capacitor volume is reduced by a factor of 9, and cost by a comparable amount! The 5V output will still require a relatively small filter capacitor because of the small ripple current and switching noise spikes remaining in that output.

However, when the ripple current is steered to the highest voltage output, it may not have sufficient minimum load power to satisfy the critical minimum current requirement. This problem can be solved by sensing the load current in this output and if it drops to the critical level, switching in an additional dummy load. This takes care of the minimum load requirements of the entire supply. Another way to solve the minimum load problem is to use synchronous bi-directional switches instead of conventional rectifiers in this

output. When the load current is less than 1/2 the peak-peak ripple current, the bi-directional switches will allow the inductor current to be negative at times during the switching cycle so that output voltage averaging and continuous mode operation is maintained even with no load.

9. With bi-directional switches instead of rectifiers, performance can be further optimized by steering most of the ripple current to a special high voltage "output" (really not an output in the normal sense) whose sole purpose is to provide the ultimate in cost-effective filtering. At the high voltage level (50V?), the capacitor required to handle the filtering task is much smaller (1/100?) and lower in cost. No minimum load is available at the high voltage level, but the bi-directional switches eliminate that requirement.

The Normalized Equivalent Circuit: These additional advantages of the coupled filter inductor and the principles of ripple current steering are more easily explained using a normalized equivalent circuit which reduces transformer and inductor windings to a 1:1 turns ratio and then combines all mutual elements. This equivalent circuit is intended to provide insight into instantaneous circuit behavior within the switching cycle. It is not comparable to the small signal state-space averaged models used for loop gain analysis at frequencies well below the switching frequency.

In the transformer driven circuit of Figure 1, secondary voltages V_{in1} and V_{in2} are positive values during the time the primary MOS switch is ON. During the OFF time, the voltages on all the transformer windings must be allowed to swing negative in order to reset the flux in the transformer core. Rectifiers D1A and D2A allow this negative swing to occur while the inductor freewheels its current through D1B and D2B.

Assuming D1A and D1B are matched and D2A and D2B are matched, the circuit of Figure 1 can be replaced by Figure 2. The transformer has been replaced by two pulse voltage sources whose voltages are identical to the transformer secondary voltages during the ON time, but are at zero during the OFF time instead of swinging negative. This permits the two rectifiers in each output to be replaced the single rectifiers D1 and D2. The two circuits function the same -- the voltage and current waveforms at the inductor inputs are identical and each inductor always has a series rectifier.

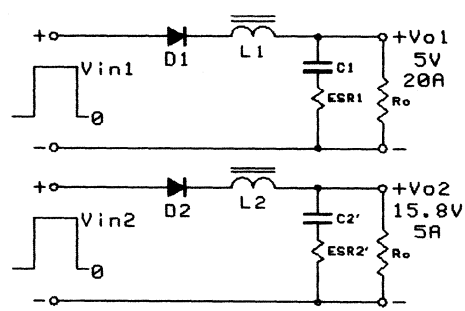


Fig. 2 Equivalent Sources

The next step is to normalize the 15V output to the same impedance level as the 5V output. The actual transformer and inductor turns ratio, n, is 3:1. The 15V output is normalized to 5V by dividing its transformer and inductor turns by n, adjusting its voltages and current by n and impedances by n^2:

$N2' = N2/n = N1$

$V_{in2}' = V_{in2}/n$; $V_{D2}' = V_{D2}/n = 1/3 = .33V$; $V_{o2}' = V_{o2} = 15.8/3 = 5.27V$

$I_{o2}' = I_{o2} \cdot n = 5 \cdot 3 = 15A$; $L2' = L2/n^2$; $C2' = C2 \cdot n^2$; $ESR2' = ESR2/n^2$

$V_{in2'}$ is now identical to V_{in1}, and can therefore be combined with it into the single source V_{in1} as shown in Figure 3. Note how small $V_{D2'}$ is, reflecting its small proportionate effect on the 15V output. Note also that the power level of output #2 is the same as before. We can in fact think of output #2 as being at either the 15V level or the 5V level and translate back and forth according to the relationships established by the actual turns ratio. It doesn't matter to the inductor if the winding has 1/3 the turns at 3 times the current and 1/3 the voltage swings and 1/9 the circuit value of inductance.

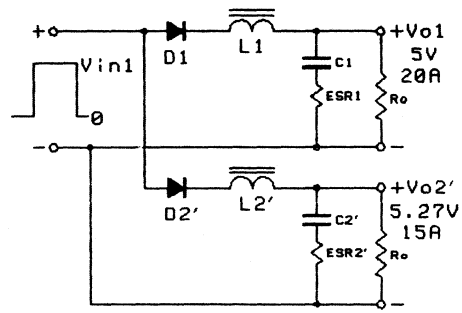


Fig. 3 Normalized

In Figure 4, rectifiers D1 and D2' are moved to the output side of their respective inductor windings. This makes it clearer that the rectifiers simply act as DC offsets to the output voltage levels.

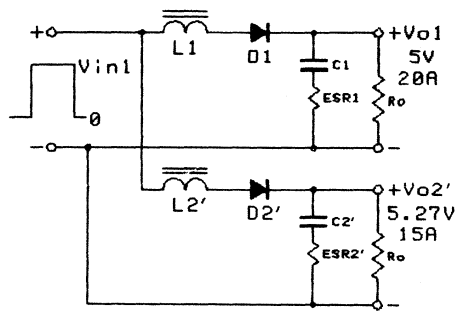


Fig. 4 Relocate Diodes

Figures 1 to 4 apply with either independent or coupled inductors. With independent inductors, Figure 4 is the final step in circuit simplification. However, if the inductors are coupled it is possible to go an important step further. In Figure 4, L1 and L2' have exactly the same normalized number of turns on the same core. Therefore they must have the same normalized mutual inductance values and the same induced volts/turn. Since they are directly connected on their input side, L1 and L2' can be combined into the single inductor Lm as shown in Figure 5. But the coupling between the two outputs is never perfect because of leakage inductance between the windings and external circuit wiring inductance. Lℓ1 and Lℓ2' represent the combined leakage and wiring inductance in each output, normalized to the 5V output level.

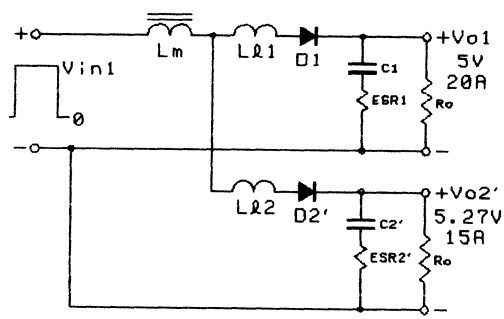


Fig. 5 Combined Mutual Inductance

Ripple Current Steering: In a practical, well-designed multi-output buck regulator as shown in Fig. 5, mutual inductance Lm is much greater than uncoupled inductances Lℓ1 and Lℓ2'. These in turn have much higher impedance than the output capacitors (including ESR) at the switching frequency. So the total normalized ripple current to all outputs is determined almost entirely by Lm. The total ripple current is apportioned between the normalized outputs by the uncoupled inductances Lℓ1 and Lℓ2'. In other words, the ripple current can be steered to one output or the other or apportioned in any desired way according to the relative normalized values of the uncoupled inductances.

If it is desired to steer most of the ripple current to the high voltage output, Lℓ2 must be much smaller than Lℓ1. Figure 6 gives a better view of this situation. The inductor should be designed to put the leakage inductance in series with the low voltage winding. This is accomplished by placing the high voltage inductor winding closest to the centerleg, with the low voltage winding immediately on top of it. In a well-designed inductor using ferrite E-E cores, the leakage inductance is usually less than 10% of the mutual inductance, and may be as low as 2% if the windings are interleaved. It will be greater than this with pot cores because of the poor window aspect ratio, and can be considerably less on a toroidal core.

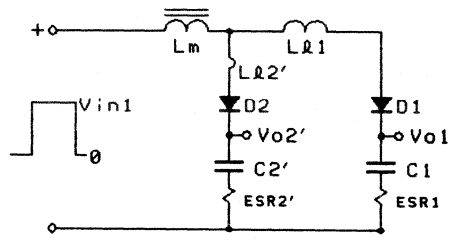


Fig 6 Ripple sent to #2

Effective ripple current steering and control can be achieved with uncoupled inductance values that are a very small fraction of the total inductance. In fact, uncoupled inductance should be kept as small as possible to avoid spurious resonances which can result in excessive phase shift and other closed loop problems. This means paying strict attention to minimizing wiring inductance as well as proper inductor design.

At frequencies above 100kHz, wiring inductance becomes a significant portion of the total uncoupled inductance and may in fact be larger than the leakage inductance in low voltage outputs. A comparable amount of wiring inductance in a high voltage output is much less significant than in a low voltage output. This is evident when the high voltage output is normalized to the low voltage level -- the wiring inductance is reduced by the square of the turns ratio. This makes it naturally easier to steer most of the ripple current to a high voltage output. Fortunately, this is where it is usually desired.

Design Example -- 180 Watt Forward Converter:

Output #1:	5 Volt,	20 Amp	--	100 Watts
Output #2:	15.8 Volt,	5 Amp	--	80 Watts
(Normalized Output #2:	5.27 Volt,	15 Amp	--	80 W)

First, define the turns ratio for the transformer and coupled filter inductor. The number of turns should be proportional to the output voltages plus rectifier drops:

$$N2:N1 = (15.8+1):(5+0.6) = 16.8:5.6 = 3:1$$

The inductor windings are not required to have the same number of turns as the transformer secondaries, but they must have identical turns ratios.

Then, making the temporary assumption that the entire power output of the supply is concentrated in a single output (#1 - 5 Volts, 35 Amps, 180 Watts), the L and C values that would be required for this output are calculated.

The L value is calculated during the OFF time, when the inductor freewheels across the 5 volt output + 0.6 V rectifier drop. Assuming a maximum inductor

ripple current of 6A p-p (17% of full load output current) at maximum OFF time of 7.5 µs (T=10 µs, Dmin = .25 at max. V_{in}):

$$Lm = E\,\Delta t/\Delta I = 5.6x7.5/6 = 7\ \mu H$$

Design the inductor with winding #1 outside #2. Leakage L in the 5V output #1 will approximate 700nH (10% of 7 µH) plus 100 nH wiring inductance for a total uncoupled inductance, L&1 = 800 nH. In output #2, leakage L is 0. Wiring L of 100 nH is divided by turns ratio 3:1 squared, so L&2' is only 11 nH.

I_L distribution:
#1 = 6A•11/(800+11) = .08 A p-p
Normalized - #2 = 6A•800/(800+11) = 5.9 A p-p
Actual - #2 = 5.9A/3 = 2 A p-p

Critical min. load on #1 output: .08/2 = .04 A; on #1 output: 2A/2 = 1 A

Max. output voltage ripple = 1% p-p = .05V @ 5V ; .15V @ 15V

Capacitor requirements for 15V output #2:

$$C = \frac{\Delta I}{8f\Delta V} = \frac{2}{8\bullet 0.1\bullet .15} = 16.7\ \mu F; \quad ESR = \Delta V/\Delta I = .15/2 = .075\ \Omega$$

Capacitor requirements for 5V output #1 (Assume 0.5A p-p for safety margin):

$$C = \frac{\Delta I}{8f\Delta V} = \frac{0.5}{8\bullet 0.1\bullet .05} = 12.5\ \mu F; \quad ESR = \Delta V/\Delta I = .05/0.5 = 0.1\ \Omega$$

Using aluminum electrolytics, ESR requirements dominate. Capacitors used:

#2 Output:	Panasonic HF 470µF, 25V, .07Ω, 1.7 cm dia. x 2.9 cm,	$.63
#1 Output:	Panasonic HF 1000µF, 10V, 0.1Ω, 1.3 cm dia. x 2.9 cm,	$.44

If all ripple 6A p-p was in Output #1, 4 capacitors would be required:

Panasonic HF 2200 @ 16V, .008 Ω, (1.9 cm dia. x 3.6 cm)x4, Total cost $3.50

Refer to Design Reference Section M6 for the actual design of the coupled inductor. Start with the earlier temporary assumption and design a single winding inductor of 7 µH with a conductor area appropriate for 35 Amps. Then provide for the additional outputs by assigning part of the conductor and winding area to the other outputs in proportion to their relative power outputs. This will result in operation of all windings at the same current density and uniform distribution of power dissipated within the windings.

The #1 winding is actually only 20A, not 35A. Reduce its conductor area in proportion to this reduction in current. Its winding area will be reduced by the same proportion. The window area thus made available will exactly accommodate the #2 winding which has the same number of turns carrying 15A at the normalized 5V level. But with the 3:1 turns ratio, the actual 15V #2 winding will have 3 times the turns with 1/3 the conductor area for the same current density and same winding area. The measured inductance values of the windings will of course be proportional to the turns squared. In building the

inductor, the winding which will receive most of the ripple current (in this case #2) must be the innermost winding so as to have the least leakage inductance.

Closing the Feedback Loop: To avoid confusion, it is best to normalize all outputs to the one sensed for closed loop control, and draw the equivalent normalized circuit as shown in Figure 7. Lℓ2' is so small it is omitted. Note that mutual inductance Lm with capacitor C2' is the main LC filter, but there are additional resonant LC circuits involved in the "downstream" lower voltage outputs such as Lℓ1 and C1. These spurious resonant circuits can cause ringing and instability unless their Q is less than 1. There are two cases to be considered:

If the first sequential output (in this case #2, 15V) is sensed for control, loop gain considerations are similar to a single output. The control loop will dampen the resonant circuit Q. This 15V output will be well controlled and regulated, but if downstream resonant circuit Lℓ1-C1 is underdamped under any load condition, the 5V output will exhibit shock-excited ringing at the Lℓ1-C1 resonant frequency. Make certain the downstream output is critically damped under all conditions.

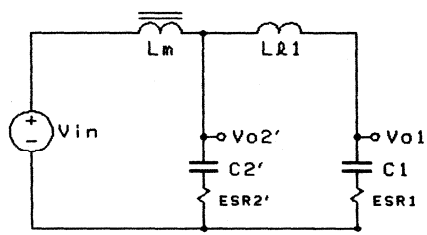


Fig. 7 Small Signal Model

If a downstream output such as #1, 5V is chosen to close the loop, there will be two (or more) LC circuits in cascade with two 180° phase lags which makes loop closing difficult, to say the least. Using current mode control eliminates inductor Lm1 and its 90° phase lag which helps a lot. In addition, the downstream resonant circuit frequencies must be well above the loop gain crossover frequency and they must still be critically damped or their ringing will reflect into the upstream (#2, 15V) output.

In the design example, Lm of 7 µH and C2' of $470 \cdot 3^2$ = 4200 µF resonate at 925 Hz, and the resonant impedances of L and C are .041 Ω. Max. ESR2' is $.07/3^2$ = .008 Ω, for a Q of .041/.008 = 5, which will be reduced further by shunt load resistance and series rectifier dynamic resistance. If current mode control is employed, Lm is absorbed in the equivalent current source and there is no longer a resonant condition. Then, if the loop gain crossover frequency is 10-20 kHz, the Lm-C2' phase shift will approach 90°.

In the downstream section, Lℓ1 of 0.8 µH and C1 of 1000 µF resonate at 5600 Hz with resonant impedances of .028 Ω. Series ESR1 of 0.1 Ω causes a heavily overdamped situation. Essentially, the capacitor ESR zero frequency of 1600 Hz is well below the resonant frequency and so this section behaves more like an L-R section, with 45° phase shift at 20 kHz, the Lℓ1-ESR1 pole frequency. This means the total phase shift is less than 135° up to 20 kHz, allowing the crossover frequency to be as high as 20 kHz if desired.

If it is necessary or desireable to raise the frequency and lower the Q of the downstream outputs, try hard to reduce the leakage and wiring inductances. (Large uncoupled inductance values are not needed to steer ripple currents and correct for rectifier mismatch.) A long stretched-out winding provides the lowest leakage inductance. For this reason, pot cores are poor, and toroidal

cores are best of all. Leakage inductance may also be reduced by a factor of 3 or 4 by interleaving the coupled inductor windings. Split the high voltage winding into two series connected portions, each with half the total turns. Sandwich the entire low voltage winding between the two halves of the high voltage winding. The leakage inductance will be only 1/3 of the equivalent non–interleaved structure and it will appear in series with the low voltage (central) winding. In addition to the more leveraged wiring inductance of the low voltage output, this will steer most of the ripple current to the high voltage output where it is more easily and effectively filtered.

When the ripple current is steered to a high voltage output and/or at high frequencies, ceramic or film capacitors often become cost–effective in place of electrolytic capacitors, with ceramics offering considerable reduction in size. However, with an electrolytic capacitor, the ESR requirement dictates the capacitor size and the resulting C value is huge compared to the actual C requirement. This has one big advantage. The large C value results in a low L/C ratio and output surge impedance, making the output much stiffer when loop bandwidth is low. Even with high loop gain–bandwidth, under large signal conditions which inevitably occur at start–up and with large, rapid load changes, considerable output voltage over/undershoot will occur because of the much smaller C values of the ceramic or film capacitors.

In addition, if ceramic or film capacitors are used in the downstream outputs (which may be feasible and desirable because ripple current is much less than with independent inductors), the smaller C values with almost zero ESR will substantially raise the Q and resonant frequency and of these "downstream" resonant circuits. This worsens the output and loop gain stability problems mentioned earlier (lowering uncoupled inductance helps, but lowering C and eliminating ESR hurts).

In the design example, C1 could have been a 12.5 μF ceramic or film capacitor. The Lm–C1 resonant frequency would then be 50 kHz, with a resonant impedances of 0.25 Ω and no ESR to lower the Q. With minimum shunt load R of 0.25 Ω, this section is critically damped only under full load conditions, and Q will become quite large with light load. This is not acceptable. Although the resonant frequency is well above the highest possible loop gain crossover frequency, this Ll1–C1 section will cause shock–excited ringing at 50 kHz between the two outputs, no matter which is controlled. One solution to this problem might be to shunt the 12.5 μF capacitor with a 220 μF, 10 V electrolytic whose ESR of 0.22 Ω will keep the Q less than 1.

REFERENCE:

1. H. Matsuo and K. Harada, "New Energy Storage DC–DC Converter with Multiple Outputs," Solid State Power Conversion, Nov. 1978, pp 54–56.

ADDENDUM 9/88 – Positive and Negative Outputs. In Figure 1 with windings L1 and L2 coupled, suppose diodes D2A and D2B are reversed to provide –15.8 V output. The polarity of L1 must be opposite L2, otherwise the voltage waveforms across the windings will conflict catastrophically. The polarities may be reversed by driving the two coils from opposite ends, but this will generate considerable noise spikes in the outputs because the noisy end of each winding is physically close to — and therefore capacitively coupled to — the output end of the other winding. This problem can be eliminated by driving all windings from the same end, but reversing the rotational direction of the negative current windings vs. those with positive current, i.e., plus current windings could be "right–handed", while minus current windings are wound "left–handed". This is the approach to use when plus and minus outputs are taken from the same transformer secondary.

Referring again to Figure 1 (original diode polarities) with two positive outputs, the two windings are driven from the same end and there is no output noise problem. However, because the two transformer secondaries are independent, the 15.8 V output can be made negative simply by grounding the plus output terminal rather than the minus terminal. Thus, the coupled inductor sees "positive" current in the negative output and all windings are polarized the same.

HOW TO DESIGN A TRANSFORMER WITH FRACTIONAL TURNS

Lloyd H. Dixon, Jr.

Fractional turns used in high frequency switching power supply transformers can reduce the number of turns otherwise needed to provide low voltage outputs and to obtain desired voltage resolution between several outputs. With fractional turns, half the number of turns or less may be required in all windings, significantly decreasing transformer size and cost. Unfortunately, fractional turns have inherently high leakage inductance, making their use impractical unless special techniques are employed. Several methods of accomplishing this are described.

The Need for Fractional Turns: The optimum number of turns in a transformer winding depends upon the maximum allowable flux swing and the operating frequency according to Faraday's Law (in SI units with dimensions in cm):

$$N_{(optimum)} = (V_N \Delta t / A_e \Delta B) \cdot 10^4$$

where ΔB is the flux swing (Tesla), A_e is the centerleg area (cm^2), and Δt is the time (approaching 1/2 the period) that voltage V_N is across the winding.

In switching power supplies designed to operate at frequencies below 50 kHz, the optimum numbers of turns are so large that there is little need to use fractional turns. At higher frequencies, fractional turns become attractive for the following two reasons:

1. Optimum transformer design may call for less than one full turn for the lowest voltage secondary. This is likely to happen at high frequencies, high power levels, and especially with the 2 to 3 volt outputs required by the newer logic families.

2. With multiple secondaries, to obtain the desired output voltages with sufficient accuracy using integral turns may require several times the optimum number of turns. For example, with a 12 V and 5 V output, a turns ratio of 2.5:1 or 2.25:1 may be desired. If 1 turn is optimum for the 5 Volt output, 3 turns will provide too much voltage for the 12 Volt output, causing excessive losses in a linear post-regulator. Otherwise, 5 and 2 turns or 9 and 4 turns are necessary to achieve the desired voltage resolution.

In these examples, the actual number of turns required in all windings may be 2, 3,or 4 times greater than optimum. Slightly larger wire sizes are required because the larger transformer must operate at lower current density. This means the winding window area will be 2, 3, or 4 times larger and the core and transformer volume will be 2.8, 5.2, or 8 times larger, with a corresponding increase in cost. This can be a powerful incentive to use fractional turns!

Implementing a Fractional Turn: A fractional turn is really a full turn around a fraction of the total centerleg flux. With an E-E core shape having two outer legs of equal areas, each outer leg has 1/2 the total flux. A single turn around either outer leg will have an induced voltage equal to 1/2 the primary volts/turn. Such a turn is therefore equivalent to 1/2 turn. In

Figure 1A, winding A is 1/2 turn and winding B is 1 1/2 turns. (The half turns are <u>both</u> linked to leg #3). In the cross core shown in Figure 1B, the total flux divides into four equal portions in the four equal area outer legs. Windings A, B, and C are effectively 1 1/4, 1 1/2, and 1 3/4 turns.

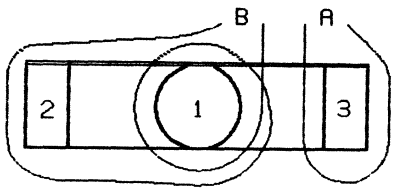


Figure 1A

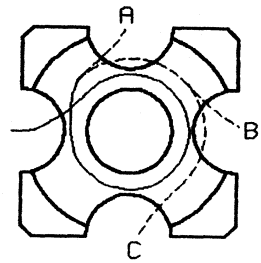


Figure 1B

Figures 2A and 2B show a transformer with multiple outer legs and its magnetic circuit equivalent. A single "fractional" turn is shown which encloses one or more (but not all) outer legs which are combined into leg #3 with magnetic cross-section area A_3 and permeance $P_3 = \mu A_3/\ell_3$. The remaining outer leg(s) are collectively leg #2 with area A_2 and permeance P_2.

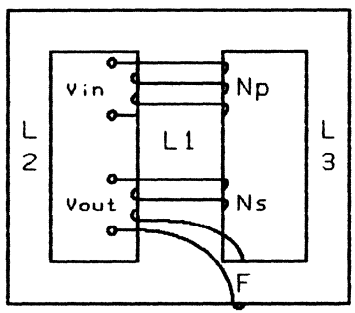


Figure 2A

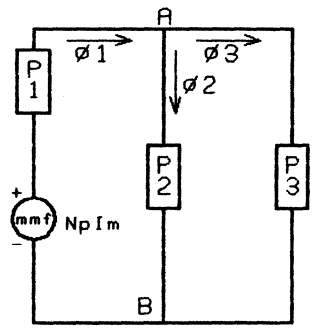


Figure 2B

With no secondary current, centerleg flux ϕ_1 divides between outer legs #2 and #3 in proportion to their permeances and their areas (assuming magnetic lengths ℓ_3 and ℓ_2 are the same). Let $F = P_3/(P_2+P_3) = A_3/(A_2+A_3)$, the fraction of the total outer leg area enclosed by the fractional turn. This turn encloses a corresponding fraction of the total flux, $\phi_3 = F \cdot \phi_1$, and $d\phi_3/dt = F \cdot d\phi_1/dt$. From Faraday's law, the induced volts/turn equals the rate of change of the enclosed flux, so the voltage induced in the fractional turn equals F times the primary volts/turn, V_{in}/N_p.

The full secondary turns around the centerleg and the primary turns link the same flux ϕ_1 so that their volts/turn are nearly identical: $V_s/N_s = V_{in}/N_p$. Thus:

$$V_{out}/V_{in} = (N_s+F)/N_p \qquad \text{(no load)}$$

Primary magnetizing ampere-turns N_pI_m provide the magnetic potential needed to support the flux level in the core.

The Leakage Inductance Problem: The full secondary turns are tightly coupled to the primary, although there is a small amount of leakage inductance in series with the full secondary turns due to stray flux between the windings. Unfortunately, the fractional turn has very high leakage inductance, and its induced voltage, $F \cdot V_{in}/N_p$, occurs only under no-load conditions.

When load current is drawn through the fractional turn, its voltage collapses. In fact, when a fractional turn is added to an otherwise stiff winding, the short-circuit current will probably be much less than the desired full load output current. Rather than helping matters, the performance of the winding is worsened by adding the fractional turn because of its leakage inductance.

As shown in Figure 3, secondary current through the full turns around the centerleg generates a magnetic potential, N_sI_s, which is cancelled by equal and opposite primary ampere-turns, N_pI_p. Magnetizing current, I_m, and centerleg flux, ϕ_1, do not change significantly. However, current through the fractional turn creates a magnetic potential in leg #3 which easily diverts flux ϕ_3 to leg #2. Because flux ϕ_3 is diminished, the voltage induced in the fractional turn is reduced. So the fractional turn voltage decreases rapidly with increasing load. At higher load current levels (usually well below desired full load), $d\phi_3/dt$ will reverse and the voltage induced in the fractional turn becomes negative. When this happens, the total secondary voltage is less than it would have been without the fractional turn.

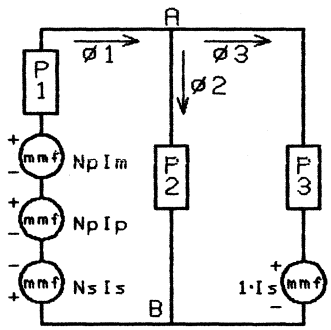


Figure 3

The leakage inductance of the fractional turn is:

$$L = F(1\text{-}F) \cdot P = F(1\text{-}F) \cdot \mu A/\ell \cdot 10^{-2} \qquad \text{Henrys}$$

ℓ (cm) - length of the outer legs
$A = A_2+A_3$ (cm^2) - combined areas of all outer legs
$F = A_3/A$ - fraction of total outer leg area linked to fractional turn
$\mu = \mu_o\mu_r = 4\pi \cdot 10^{-7} \cdot \mu_r$ - absolute permeability of the outer leg material
$P = P_2+P_3 = \mu A/\ell$ - permeance of all outer legs combined

This inductance of the fractional turn is equivalent to the inductance of a single turn wound on a core consisting of legs #2 and #3 in series. (Leg #1 has no effect.) The worst case is when the fractional turn links half the total outer leg area (effectively 1/2 turn). Whether the fractional turn is in series with one or more full turns around centerleg #1, or whether it is the entire secondary winding, it has the same leakage inductance. However, when the fractional turn is in series with several full turns, the power taken from it is only a small portion of the total transformer power. The adverse effect of the leakage inductance is then proportionately less, but it is more than enough to badly hurt cross-regulation in a multi-output supply.

The Solution to the Problem: The solution is simple -- maintain the flux in outer leg portions #2 and #3 in exactly the same ratio regardless of secondary current; in other words prevent the flux from escaping from leg #3 to leg #2 when the load current increases.

One technique used to keep the flux balanced in the two outer legs of an E-E core is to put one turn around each outer leg as shown in Figure 4. The two outer core legs have the same area (and permeance). Each of these turns links half the centerleg flux and acts like a half turn. If these turns were connected in series with the correct polarity, together they would become a full turn. But connected in parallel (with the same polarity) they act together like a single half-turn. Because of the parallel connection, the voltages induced across each turn must be identical, forcing equal flux in the two outer legs. This requires the opposing magnetic potentials in each outer leg to be the same ampere-turns which means the secondary current is shared equally by the two turns.

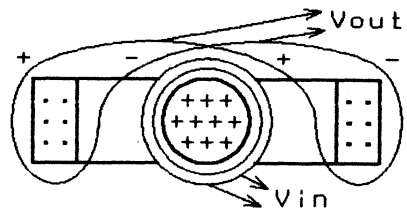


Figure 4

If the two outer legs had unequal flux, the voltages induced in the two paralleled turns would differ. This would cause a differential current to flow between these turns, applying magnetic potentials to each leg in a direction to eliminate the original flux inequality. Essentially, the cross-connection between the two turns forces the flux to divide equally between the two outer legs.

Note that even if the two outer legs have different areas, the flux in each leg is forced to be half the total flux, so that the paralleled turns still act like half turns.

While this technique eliminates the huge leakage inductance of a single half turn, it is far from ideal because there is much stray flux outside the core which is linked to the primary but not to the windings around the outer legs. This results in significant leakage inductance. Normally, to minimize leakage inductance caused by stray flux, good practice dictates the secondaries should be wound as intimately as possible with each other and with the primary.

Figure 5 shows a big improvement on the above technique which provides much better coupling to the primary, minimizing the leakage inductance of the half turn secondary. Two half cylinders of copper foil or strip are placed directly over the primary winding, separated only by the minimum insulation required for primary-secondary isolation. The half cylinders must not directly contact each other. They are paralleled by means of a pair of tabs off one end of each half cylinder, cross-connected over the outside end of the core. Output from the winding may be taken from across this pair of tabs.

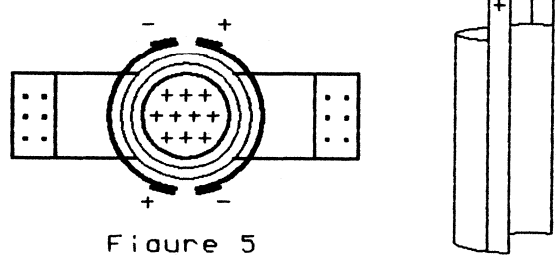


Figure 5

The series inductance of this half turn approach is not quite as good as one full turn of copper strip because of the inductance of the cross-connected tabs. Further reduction in series inductance may be obtained by putting cross-connected tabs at both ends. The ultimate improvement is to divide the primary into two portions and interleave the secondary structure between the two primary portions.

Because the cross-connected half turns in Figure 5 force equal flux division, the outer legs are "stiffened", so that a half turn added to any other secondary(s) will also have low leakage inductance.

Using a Separate Flux Balancing Winding: Any windings that cross-connect the two outer legs will force the flux to divide equally between the two outer legs. It is not even necessary for the flux balancing winding to be one of the output windings. As shown in Figure 6, it may be a completely separate winding dedicated to the sole purpose of flux equalization between the outer legs. This enables a single wire half-turn to be added to any secondary with minimal series inductance by forcing the total flux to remain equally divided between the two outer legs.

This technique is useful when fractional turns are added to more than one secondary, and especially with the center-tapped secondaries used in push-pull converters, where a fractional turn must be added each side of center-tap. These situations are difficult to implement by the method shown in Figure 5.

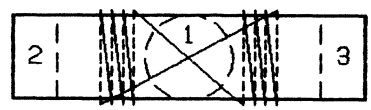


Figure 6

As shown in Figure 6, the flux balancing winding has two coils with equal numbers of turns cross-connecting the two outer legs at the point where they join the centerleg. Actually, this winding can be a single turn on each outer leg or many turns. It is better to use multiple turns because finer wire can then be used. By laying these fine wire turns side by side along the outer legs, interference with the bobbin is minimized, and eddy current problems are eliminated.

The ampere-turns of the flux balancing winding will be 1/2 the unbalanced amperes of the secondary half-turns. For example, assume two secondaries, 12 V, 3 A and 24 V, 2 A, each having a half turn in series with several other full turns. If the 3 A and 2 A half turns link the same outer leg, the worst case ampere-turns in the flux balancing winding will be (3+2)/2 = 2.5 A. With five turns on each outer leg, the current in each turn is 2.5/5 = 0.5 A. On the other hand, if the 2 A and 3 A half turns link to opposite legs, the worst case is with the 3 A secondary at full load and the 2 A secondary at no load. The maximum flux balancing ampere-turns will be half of 3, or 1.5 A-t, resulting in only 1.5/5 = 0.3 A in the five turn flux balance windings.

For this method of flux balancing to be the most effective in reducing leakage inductance, the flux balancing winding must have good coupling to the secondary half turn(s):

1. Wind the flux balancing coils on the outer legs as close as possible to where the flux divides - close to the centerleg. If they are located further out on the outer legs, coupling to the secondary half turns on the centerleg is reduced.

2. With a secondary half turn in series with several full turns wound helically along the centerleg, make sure this half turn is at the end of the centerleg adjacent to the flux balancing winding.

3. When the half turn is foil or strip along the length of the centerleg, put a flux balance winding at both ends of the centerleg.

4. When a secondary handles most of the total transformer power and has only 1/2 turn or 1 1/2 turns total, the method of Figure 5 works the best.

Diverse Fractional Turn Values: It is certainly possible to obtain fractional turn values other than 1/2. Referring back to Figure 1B, a cross core with four outer legs can provide 1/4, 1/2, or 3/4 turns. A slightly different technique is required to keep the flux divided equally among all four legs--a single flux balancing turn is put around each of the four legs and these four turns are paralleled. Because of the parallel connection, the voltages induced across each turn must be equal, which forces equal rates of flux change in each leg. Otherwise, current would flow in the flux balancing turns which would bring the flux changes back into equality.

In reference (1), the author cleverly provides the flux balancing winding by means of a double sided printed circuit board at one end of the centerleg where it interferes minimally with the transformer windings. Although this is a very simple and low cost method, the flux balancing turns are not close to the centerleg and the coupling to the secondary half turns is not as good as it might be. Also, cross cores are generally not optimally designed for high frequency power applications where a long narrow winding window is desirable to minimize leakage inductance and eddy current losses.

Obtaining Any Fractional Value with an E-E Core: It was stated earlier that the flux balancing winding would force equal flux in the outer legs even if they have unequal areas. Conversely, *it is easy to obtain any desired induced voltage in the fractional turn by forcing unequal flux division between the two outer legs*, even though their areas are equal. This makes it possible to take advantage of the better performance and cost available with modern E-E cores.

Unequal flux division between two outer legs of equal area is obtained by *using unequal turns in the flux balancing windings*. Suppose there are twice as many turns on leg #3 as on leg #2. The induced voltage across both windings must be equal because they are in parallel. This means the volts/turn and $d\phi_3/dt$ of leg #3 must be 1/2 of leg #2. Therefore 1/3 of the total flux goes to leg #3 with twice the turns, while 2/3 goes to leg #2.

Any secondary fractional turn linked to leg #3 will have only 1/3 of the primary volts/turn induced, while a fractional turn linked to leg #2 will have 2/3 of the primary volts/turn. Similarly, a 1:3 turns ratio in the flux balancing winding will result in a 1/4 : 3/4 flux division and corresponding fraction of the primary volts/turn induced in a fractional turn. Depending upon which leg is linked by the fractional turn, 1/4 turn or 3/4 turn is obtained. It is possible to obtain 1/2 turn in this configuration by putting one additional turn around the 1/4 turn leg!

When the flux division is made unequal between two outer legs of equal area, obviously one outer leg has greater flux density (and flux swing) than the other, and probably greater flux density than the centerleg, as well. This could theoretically force a reduction in the operating flux level and reduce the core utilization to avoid saturating the high flux density leg. However, fractional turns will normally be used above 50-100 kHz, where the flux density swing is limited by core losses, not saturation. The only adverse result is that one outer leg will have greater core loss, the other leg less, for a net small increase in core loss.

Experimental Results: The data given in Table I was taken with a 20 turn primary winding over the centerleg of an EC41 ferrite core. Secondaries were placed directly over the primary (not interleaved) with 5 mil insulation in between. Leakage inductance was measured on the primary side with the various secondary configurations shorted because it is difficult to obtaining accurate measurements on the 1/2 turn low impedance secondary side. Equivalent secondary leakage inductance with the primary shorted was calculated from the measured primary values.

TABLE I

Description	Measured Primary	Calculated Secondary	
(1) Primary only (20 turns) -- no secondary	1480 µH	--	
(2) 1 Full turn copper strip secondary	1.6 µH	1 nH	(Ideal)
(3) 1 Half turn strip - no flux bal. wdg.	944 µH	885 nH	
(4) Same with flux bal. opposite tab end	144 "	91 "	
(5) Same with flux bal. wdg. at tab end	38 "	24 "	
(6) 2 Par. half turns, outer leg (Figure 4)	42 µH	26 nH	
(7) 2 Par. half turns over primary (Figure 5)	8 "	5 nH	
			Measured Secondary
(8) 5 turn wire sec. spread across centerleg	2.9 µH	181 nH	185 nH
(9) 5 1/2 turn secondary - no flux bal. wdg.	17.5 "	1320 "	1580 "
(10) Same with flux bal. opposite end	4.2 "	317 "	307 "
(11) Same with flux bal. same end	2.8 "	211 "	207 "

Line (1) of Table I shows the open circuit primary inductance of 20 turns on the EC41 core. Line (2) demonstrates the lowest leakage inductance that can be obtained without interleaving the secondary between two primary half-sections. Dividing the 1.6 µH measured primary value by $(20/.5)^2$ gives 1 nH lowest possible leakage inductance for 1/2 turn - the ideal goal. (3) shows how bad a single half turn strip is without a flux balancing winding. Adding flux balancing opposite the tab end of the half turn (4) provides much improvement, but at the tab end (5) coupling between flux balance winding and the half turn is much better. Still, 24 nH is a long way from the 1 nH goal. It is just not possible for the flux balance winding at the one end of the centerleg to couple more effectively to the half turn along its entire length.

Line (6) shows the technique of Figure 4, with one turn of strip around each outer leg. The large amount of stray flux between these turns and the primary cause high leakage inductance. Best is (7), with the two half-cylindrical strips directly over the primary. Most of the 5 nH is in the cross-connected

tabs at one end, and this could be further reduced by putting tabs at both ends. This is the best approach when most of the transformer power is in the half-turn (or 1 1/2 turn) winding.

Lines (8) - (11) show the results of adding a half turn to several full secondary turns, using wire instead of strip. The secondary impedance levels are high enough to take measurements from the secondary side as well. (8) shows that the 5 full turn secondary does not couple as tightly to the primary as the shorted strip in (2). This is because the 5 turns were spread across the centerleg with large spaces between turns (but this is much better than bunching the 5 turns in the center of the primary). Several parallel wires should have been used to fill the centerleg. The 185 nH is almost twice what it should be compared to (2). Note that with the additional half turn placed at the same end of the centerleg as the flux balance winding (11) the coupling is good and the additional leakage inductance of the half turn is only 22 nH. This compares to the half turn secondary alone in (5), but in (11) it is small by comparison to the leakage inductance of the 5 full secondary turns.

References:

1. G. Perica, "Elimination of Leakage Effects Related to the Use of Windings with Fractions of Turns," Proceedings of Power Electronics Specialists Conference (PESC), 1984, pp. 268-278

SWITCHING POWER SUPPLY TOPOLOGY REVIEW

by

Lloyd H. Dixon, Jr.

INTRODUCTION:

This paper reviews the characteristics of the three basic circuit families commonly used in switching regulated power supplies: buck, boost and flyback (or buck-boost). These three circuit topologies may be operated in one of two modes: the discontinuous or continuous inductor current modes. The choice of operational mode has great effect on the overall characteristics. The control method used can also help to minimize the problems associated with any topology and operational mode. Three control methods that operate at fixed frequency are examined: direct duty cycle control, voltage feedforward, and current mode (two-loop) control. Several extensions of the basic circuits are also discussed, with the relative merits of each topology--operational mode--control method combination.

THREE BASIC TOPOLOGIES:

The three basic configurations shown in Figure 1 are: Buck, Boost and Flyback. The Cuk converter, which is not discussed, is an inversion of the flyback topology. The three different switching circuits employ the same three elements: inductor, transistor and diode, but arranged in a different manner (the output capacitors are filter elements, not part of the switching circuits). Theoretically, there are three other circuits possible using the same three elements with T configuration, but these are simply mirror images of the first three and couple power in the opposite direction.

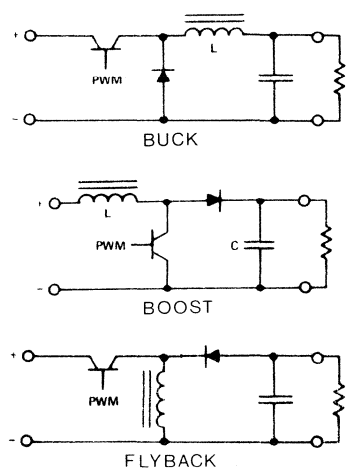


Figure 1.

One common principle that applies to all three topologies, regardless of operational mode or control method is: In steady state operation, the voltage across the inductor, averaged over each switching cycle, must equal zero. Otherwise, the average inductor current would change, violating the steady state premise.

Each of the three basic circuit families has a unique set of relationships between input and output voltages, currents, and duty cycle. For example, the basic buck regulator functions only with output voltage, V_o, less than V_{in} and with the same polarity. The basic boost circuit requires V_o greater than V_{in} with the same polarity. The flyback topology functions with V_o either greater or less than V_{in}, but the polarity must be opposite.

DISCONTINUOUS MODE OPERATION:

In the discontinuous inductor current mode, or "discontinuous mode", buck, boost and flyback circuits behave in a similar way. The inductor current is zero (hence discontinuous) during the last part of each switching cycle. During the first part of the cycle, the inductor current increases from zero, storing energy taken from the input. During the second part, all of this stored energy is discharged into the load, pumping energy from input to output.

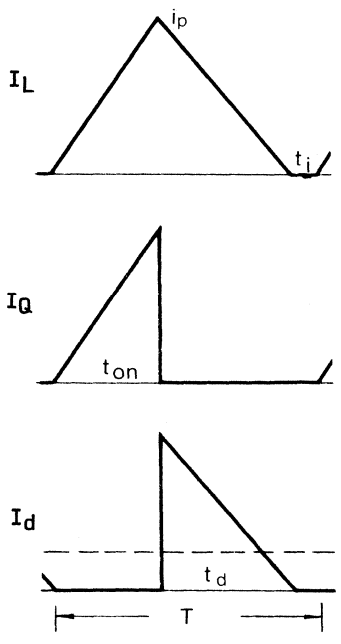
Current Waveforms. Discontinuous mode current waveforms are shown in Figure 2. The inductor, transistor and diode waveforms are the same regardless of circuit topology, but the input and output current waveforms differ for each circuit according to which of the three elements are in series with the input and the output.

Three States. There are three distinct operational states during each switching cycle:

1. During the transistor "on" time, t_{on}, inductor current I_L rises from zero to the peak value i_p. This peak current equates to energy stored in the inductor, $LI^2/2$, at the end of t_{on}. During this time the inductor current is drawn from the input, and this energy stored in the inductor each cycle is power taken from the input source.

2. When the transistor turns off, the inductor voltage reverses and its stored energy forces the same peak current to flow through the diode. During the diode conduction time, t_d, the inductor current drives the output and linearly decreases to zero. At the end of t_d, all the energy that was stored in the inductor has been delivered to the output.

3. When the current reaches zero, the inductor has no more energy. The current in all switching circuit elements is zero for the remainder of the switching period. During



	Buck	Boost	Flyback
I_{in}:	I_Q	I_L	I_Q
I_o:	I_L	I_d	I_d

Figure 2.

this idle time, t_i, the circuit waits for the next clock pulse to turn the transistor back on and begin the next cycle.

Discontinuous Mode Boundary. When load current increases, the control circuit causes transistor t_{on} (duty cycle) to increase. Peak inductor current then becomes greater and diode conduction time t_d must also increase. Consequently, an increase in load current causes a steady state reduction in the idle time, t_i. When load current increases to a certain level, t_i becomes zero, and the discontinuous mode boundary is reached. If the load current is further increased, the inductor current will no longer discharge to zero every cycle, and continuous mode operation results. The circuit will become unstable because the loop gain compensation required for stable discontinuous mode operation is not adequate to prevent oscillation in the continuous mode. It is imperative for the control circuit to sense and limit the inductor current to prevent crossing this mode boundary.

Excellent Closed Loop Response. In the discontinuous mode, it is easy to obtain excellent response in correcting disturbances that result from large step changes in line voltage and load current, because the inductor alway starts each switching cycle with zero stored energy. This makes it possible for the control circuit to obtain any energy level (and power output) required, from zero to full output, on a cycle-by-cycle basis. The inductor "vanishes" from the small signal closed loop characteristic, leaving only the output capacitor with its 90 degree phase lag. The resulting single-pole characteristic is inherently stable and easy to deal with in closing the loop (see the separate paper on "Closing the Feedback Loop"). The right-half-plane (RHP) zero which severely limits closed loop response in continuous mode boost and flyback circuits is not present in the discontinuous mode topologies.

High Peak Current. The one main disadvantage of the discontinuous mode is the high peak current through the transistor, diode and output filter capacitor. This requires semiconductors with higher current capability and puts an extreme burden on the output filter capacitor ESR (equivalent series resistance) and RMS current rating requirements. For example, in both boost and flyback circuits, the diode is in the output, and therefore the average diode current, I_d, must equal the DC output current, I_o. Under full load conditions, if diode time t_d is 50% of the switching period, the peak current is 4 times the full load I_o.

In the buck circuit the inductor current with its better form factor drives the output, so the peak current is somewhat less in proportion to the output current. However, the buck topology is seldom used in the discontinuous mode because the continuous mode provides much better performance.

Poor Open Loop Line and Load Regulation. The basic DC equation for the flyback topology operated in discontinuous mode is given below. The boost regulator has a similar but more complex formula (see "Closing the Feedback Loop"). For the flyback circuit:

(1) $$V_o = V_{in} D \sqrt{R_o / (2Lf)}$$

It can be seen from this equation that if the duty cycle is fixed (open control loop), V_o varies directly with V_{in} and the square root of the output load resistance, R_o. In other words, the open loop line and load regulation is quite poor, and duty cycle D must be changed considerably by the control circuit to maintain the desired output voltage under the full range of line and load conditions.

Control Method. In all three constant frequency control methods (direct duty cycle, voltage feedforward, and current mode), the output voltage is compared with a fixed reference voltage. The resulting error voltage is amplified and used as the closed loop control voltage, V_c.

Direct Duty Cycle Control: Transistor duty cycle $D = t_{on}/T$ is varied in proportion to control voltage V_c. Poor open loop line and load regulation requires fairly high loop gain for correction. The output filter capacitor is part of the closed loop system and introduces a phase lag which delays correction of V_{in} changes.

Voltage Feedforward Control: A sample of the input voltage is fed directly into the control circuit and causes the duty cycle to vary inversely with V_{in} as well as directly with V_c ($D = KV_c/V_{in}$). If V_{in} increases, D decreases automatically so that the input volt-seconds ($V_{in}D$) remains constant for a fixed V_c. Thus, V_c controls input volt-seconds directly. Open loop line regulation is good, so that less closed loop gain is required to meet DC regulation requirements. Equation 1 becomes:

(2) $$V_o = KV_c\sqrt{R_o/(2Lf)}$$

where K is the feedforward ratio = $V_{in}D/V_c$.

Current Mode Control: An inner, second control loop compares the peak inductor current, I_p, to the control voltage, V_c. In the outer loop, V_c now controls I_p directly. The inner loop provides good inherent line regulation, similar to voltage feedforward. Equation 1 becomes:

(3) $$V_o = KV_c\sqrt{R_oLf/2}$$

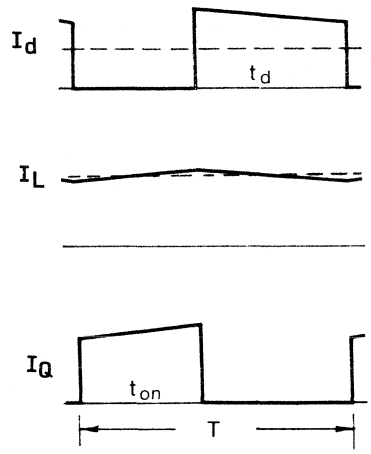
where K is the inner loop current control factor = $\max I_p/\max V_c$.

Either voltage feedforward or current mode control is recommended. They both have essentially the same good effect -- improved open loop line regulation, providing instantaneous correction to line changes and requiring less closed loop gain.

CONTINUOUS MODE OPERATION:

In the continuous inductor current mode (continuous mode), the inductor current is never zero during any part of the switching cycle (see Figure 3). Compared to the discontinuous mode for the same application parameters, the continuous mode requires much greater inductance. The inductor ripple current is small compared to the full load output current.

Current Waveforms. Continuous mode waveforms are shown in Figure 3. Just as with the discontinuous mode, the inductor, transistor and diode current waveforms are exactly the same for the buck, boost or flyback circuits, but the input and output waveforms differ according to which of the three elements are in series with input and output.



	Buck	Boost	Flyback
I_{in}:	I_Q	I_L	I_Q
I_o:	I_L	I_d	I_d

Figure 3.

The boost and flyback circuits have similar behavior. In both cases, the output current is the diode current, I_d, which is discontinuous. The peak output current is slightly more than half the value encountered in the discontinuous mode. This reduces the burden on the output capacitor.

The buck regulator behaves very differently. Its output current is the inductor current, which is not discontinuous, but has a relatively gentle slope and small ripple amplitude. This waveform is easy to filter, substantially reducing the output capacitor ESR and current rating requirements. For this reason, the continuous mode buck regulator is the most popular switching power supply configuration, particularly at higher power levels where the much higher peak current encountered with all other configurations put an intolerable burden on the output filter capacitor.

Two States. Because the inductor current is never zero, there is no idle time in the continuous mode and only two operational states during each switching cycle.

1. During transistor "on" time, t_{on}, inductor current I_L increases from an initial value (greater than zero) to a higher value, replacing the inductor energy given up during the "off" time. Current (and power) is drawn from the input.

2. When the transistor is off, the diode conducts for the rest of each cycle. I_L declines to the initial value, never reaching zero but giving up energy to the output.

In continuous mode operation, the upslope and downslope of inductor current are dependent only upon the input and output voltage levels and totally independent of the average inductor current or output load current. Without the flexibility provided by the third (idle) state of the discontinuous mode, V_{in}, V_o and duty cycle D are related differently for each topology. In the buck regulator, for example, the average voltage at the input side of the inductor is $V_{in}t_{on}/T$, or $V_{in}D$, while the voltage at the inductor output is V_o. In the steady state, the average voltage

across the inductor must be zero, so $V_O = V_{in}D$. This is the basic DC equation for the buck regulator. There are no terms relating to load current or resistance, which indicates excellent open loop load regulation. When I_O changes, steady-state I_L also changes, but the inductor ripple current and V_O do not change.

Continuous Mode Boundary -- Minimum Load Current. When the load current decreases, the duty cycle and inductor ripple current do not change (except momentarily), but the average inductor current declines proportionately. For the buck regulator $I_O = I_L$, for boost and flyback $I_O = (1-D)I_L$. At a certain critical load current level, the inductor current reaches zero at the minimum of the ripple waveform. This is the boundary for continuous mode operation. If the load current further decreases, the third state idle time appears, and the circuit operates discontinuously, with completely different operating characteristics. DC regulation degrades radically. In a continuous mode regulator, the load current must not be allowed to drop below the critical level where this boundary is crossed. This minimum load requirement is a disadvantage of continuous mode systems.

Poor Closed Loop Response. Small signal response of continuous mode regulators is much worse than discontinuous mode circuits because of the two pole second order characteristic of the resonant LC filter. Boost and flyback circuits also have a right-half-plane zero in their loop gain characteristic. While it is theoretically possible to compensate for the two filter poles, the capacitors used in the compensation network charge to unusual voltage levels during periods of large signal limited operation, when inductor current cannot keep up with changes in load current. This causes output voltage offset errors which take considerable time for correction (see separate paper: "Closing the Feedback Loop"). Current mode control overcomes this problem in continuous mode buck regulators by eliminating the inductor pole. Only the single first order filter capacitor pole remains, the same as in the discontinuous mode circuits.

The RHP zero associated with boost and flyback continuous mode circuits is much more difficult to deal with. In buck regulators, output current I_O equals inductor current I_L, but in boost and flyback circuits, $I_O = I_L(1-D)$. Consider the process in a flyback regulator. When load current increases, the output capacitor voltage immediately starts to drop. The resulting error voltage temporarily increases the duty cycle, D, causing the inductor current to rise to accommodate the increased load. However, it may take many cycles for the inductor current to complete its rise. During this time, increased D makes (1-D) smaller, so the output current is temporarily decreased, the opposite of what is desired. This additional lag because of the RHP zero inevitably forces the loop gain crossover frequency to be much lower than otherwise desired.

There is in addition a large signal problem with continuous mode circuits--the inability to rapidly slew the inductor current as desired with large step changes in load. This is because of the large inductor values used in continuous mode circuits. The

problem is most severe when attempting to increase the inductor current when operating near minimum V_{in}, especially if the circuit has been designed with input volt-second capability, $V_{in}D$, only slightly greater than required for steady state operation.

Good Open Loop Load Regulation, Poor Line Regulation. The basic DC equations for the continuous mode are:

	Buck:	Boost:	Flyback:
(4)	$V_o = V_{in}D$	$V_o = V_{in}/(1-D)$	$V_o = V_{in}D/(1-D)$

Unlike the discontinuous mode, the above equations reveal that the DC output voltage, V_o, is totally independent of output current or resistance, depending only upon V_{in} and D. The duty cycle does not change with steady-state changes in load current, but D must be changed to make correction for changes in V_{in}.

Direct Duty Cycle Control. Moderately high loop gain is required to correct the inherent poor open loop line regulation. It is difficult to design the closed loop, and many problems cannot be overcome. See earlier comments under "Poor Closed Loop Response."

Voltage Feedforward. Voltage feedforward applied in the same way as the discontinuous mode topologies provides good open loop line regulation in the continuous mode buck regulator. Equation 4 (buck) becomes:

$$(5) \qquad V_o = KV_c, \qquad K = V_{in}D/V_c$$

Open loop line and load regulation are both good. Closed loop gain is now required only for good dynamic response to changes in load. Boost and flyback topologies in the continuous mode are only partially compensated by this simple feedforward technique. Methods that are more complex will achieve compensation, but they are beyond the scope of this paper.[1]

Current Mode Control. Applied to continuous mode buck regulators, current mode control provides greatly improved performance. First, the inner current control loop provides inherent good line regulation, even with the outer loop open. Second, the inner loop eliminates the filter inductor pole so that the outer loop no longer has a two-pole second order resonant characteristic, but only the single filter capacitor pole. The gain characteristic becomes very easy to compensate. Third, compensation capacitors at the error amplifier input (which cause output voltage errors after large signal limited operation) are not required because the inductor pole is eliminated. Current mode control has the single disadvantage that it introduces load current dependency which does need closed loop correction. Buck regulator Equation 4 becomes:

$$(6) \qquad V_o = KV_cR_o, \qquad K = \max I_L/\max V_c$$

Current mode control also facilitates the paralleling of several individual power supply modules. The current control loop insures that each module will always deliver its assigned proportion of the total load current.

In the continuous boost and flyback topologies, the performance improvements from current mode control are less dramatic. Only partial voltage feedforward compensation is accomplished. When V_{in} changes, the inner current control loop maintains I_L constant, but I_o will change because the (1-D) factor relating I_L to I_o in boost and flyback circuits changes with V_{in}.

Current mode control does eliminate the inductor pole and thereby simplifies the closed loop design, but it does not eliminate the RHP zero, which is the worst limitation of the continuous mode boost and flyback circuits.

TRANSFORMER COUPLED ADAPTATIONS OF THE BASIC TOPOLOGIES:

Transformer coupled versions of the basic circuits provide several important advantages, particularly in applications where primary power is the 120 V or 230 V AC line. First, the transformer provides the isolation required for off-line power supplies. Second, the transformer permits a turns ratio adjustment which avoids the very small duty cycle and high peak currents that would otherwise occur when input and output voltages are very different, as in most off-line applications. The ability to set the turns ratio also removes the V_{in} vs. V_o and polarity restrictions that apply to the basic topologies. Also, multiple outputs at various voltages are easily obtained with multiple secondary windings.

Transformer coupling introduces some new problems, however. These include: additional cost, size and weight, losses in the core and windings, potential core saturation (especially in push-pull circuits), core reset in single-ended circuits, and voltage spikes and losses due to transformer leakage reactance.

Forward Converter (Buck). The single ended forward converter in Figure 4. is identical to the basic buck regulator with the addition of a transformer and series diode. The transformer provides line isolation and usually a large step-down turns ratio when operated off the rectified and crudely filtered AC line. For example, with 200-400 V DC input and 5 V output, a turns ratio of 15:1 is typical, to increase the duty cycle to near 50% and reduce the peak primary current.

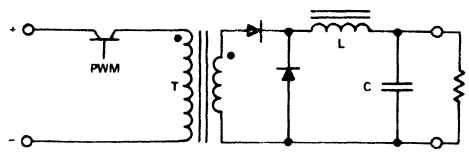


Figure 4. Forward Converter

The steady-state voltage across any transformer or inductor must average zero, or the current must change (which is not steady-state) and the core will saturate. In a push-pull system, this naturally occurs because of the symmetry of the alternating positive and negative waveform applied to the windings. In a single ended forward converter, this does not happen naturally. Specific provision must be made to reset the core by allowing the voltage across the windings to backswing during the transistor "off" time so that the reverse volt-seconds equal and cancel the volt-seconds applied during the "on" time.

The series diode is required to decouple the secondary and permit this voltage backswing. To protect the transistor, the backswing must be limited by some kind of clamp. This is often accomplished by a tertiary transformer winding, bifilar with the primary, which is diode clamped to V_{in} (the clamp is essential, but not shown in Figure 4). With the backswing thus clamped to V_{in}, the backswing voltage is the same as the forward voltage applied during the "on" time. This means t_{on} (and D) must be limited to 50%, otherwise the forward volt-seconds will exceed the reverse volt-second capability and the transformer will saturate. In summary, (1) clamp the backswing, and (2) clamp the maximum duty cycle so the forward volt-seconds can never exceed the reverse volt-second capability. With the backswing clamped to a reverse voltage equal to the forward, the voltage applied to the transistor will be 2 times V_{in}.

Transformer utilization in the single-ended forward converter is not as good as in a push pull converter, because power is not transferred during the time allowed for core reset. However, the forward converter is very popular at power levels up to 1 KW because the single ended base drive circuitry costs less.

Additional secondaries are often used when multiple output voltages are required. The continuous mode is always used because of the ease of filtering the small inductor ripple current. Current mode control is definitely advantageous.

Push-Pull Center-tap (Buck)

Figure 5 shows a push-pull centertap version of the buck regulator with two outputs whose voltages will proportion according to their respective secondary turns. The push-pull drive automatically provides core reset on alternate half cycles, but these alternate half cycles must be quite symmetrical or the volt-seconds will not cancel, resulting in core saturation. Symmetry can be spoiled by unequal transistor storage times or $V_{ce(sat)}$. Many papers have been written on symmetry correction circuits, but the best method is to use a current mode control IC such as the UC1846, which senses unbalance in the primary current waveform and automatically corrects by changing the pulse widths of alternate half cycles.

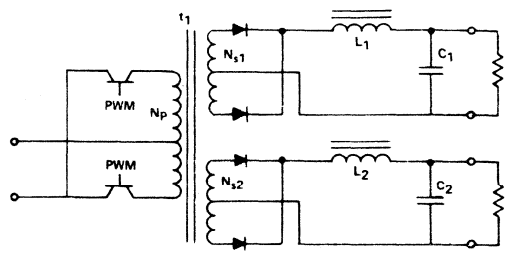


Figure 5. Push-Pull Centertap

Transistor voltage ratings must be 2 times V_{in} because of the doubling effect of the centertap primary. Peak reverse rectifier voltage may be 5 or 6 times V_o, assuming 2:1 V_{in} range. Dual base drive circuits are required.

Buck regulators are inherently "voltage-fed", that is they are driven from a voltage source and there are only low impedance

elements in the input circuit. This creates a substantial risk of damage or destruction of the switching transformers in the event of a temporary downstream fault condition, such as transformer saturation due to drive asymmetry, poor rectifier recovery characteristics, or transistor conduction overlap due to storage time with inadequate deadband provided by the control IC. These events, often transitory, have been responsible for many switching power supply failures, and they are hard to prove. These problems are eliminated by proper design and component selection.

In any buck regulator with multiple outputs, when unbalanced step changes in load occur, dynamic cross-regulation between outputs is extremely poor because of the dynamic isolation caused by the filter inductors in series with each output. This problem may be corrected by eliminating the individual inductors, coupling them by placing all the inductor windings on a common core. Perfect coupling should not be sought, however, because slight voltage differentials due to such things as unmatched rectifier forward drops will cause high circulating ripple currents. Design the coupled inductor to have 10-20% leakage inductance. This controls the circulating currents with little impairment of dynamic cross-regulation.[2]

With any topology, to get good dynamic response with large step change from light load to full load, and during full load startup, the short circuit current limit must be substantially greater than the full load current.

Half Bridge (Buck). The half bridge is also a push-pull version of the buck regulator. As shown in Figure 6, two series bulk filter capacitors provide a tapped input source. The two transistors connect the single transformer primary across the two capacitors alternately. The primary voltages and currents are symmetrical AC. DC current is not drawn from the center-tap of the input supply.

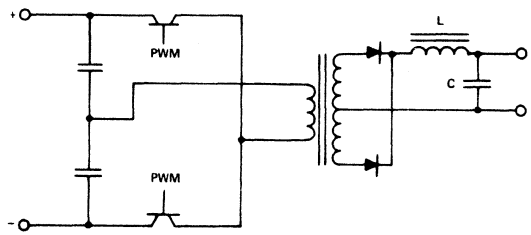


Figure 6. Half Bridge

The big advantage of the half bridge against the push-pull centertap configuration discussed previously is that the transistor voltage ratings are cut in half (although the current is doubled). This has become less important with higher voltage rating transistors more available. Base drive transformers must be used because the two base-emitters do not have common reference unless complementary NPN/PNP transistor are used, which they seldom are. The same problem with transformer drive asymmetry potentially exists.

This configuration has been extremely popular in the past. In 1983, most designers would question its cost-effectiveness at power levels under 1 KW.

Full Bridge (Buck). The full bridge (not shown) is a higher power extension of the half bridge. the circuit is identical to Figure 6 except the two series capacitors are replaced by two more transistors identical to the first two which complete the bridge. For a given power level, the transformer primary voltage is double that of the half bridge and the current is halved. The transistor voltage ratings are the same, but there are twice as many, and the transistor currents are halved.

Single-Ended Flyback. At first glance, the circuit of Figure 7 looks much like the forward converter of Figure 4. However, the transformer in Figure 4 is not a transformer, but an inductor with primary and secondary windings. Its purpose is to store energy. (The purpose of a true transformer is to directly couple energy, not to store it.) This is the shunt inductor of the flyback topology, as in Figure 1.

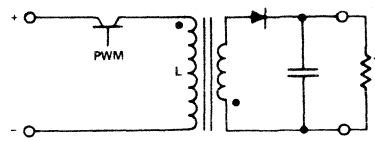


Figure 7. Single-Ended Flyback

The inductor primary and secondary have polarity opposite the forward converter transformer. When the transistor is "on", primary current (and inductor energy) is increasing, but during this time the output rectifer is reverse biased. When the transistor turns off, the inductor voltage reverses and maintains the same instantaneous ampere-turns through the secondary and the rectifier to the output, in order to maintain the energy stored in the core (or gap). Just as with the previous buck regulators, the multiple windings provide line isolation and the opportunity to adjust the turns ratio to optimize the duty cycle and minimize peak primary current.

The flyback topology is quite amenable to multiple outputs by applying additional secondaries withthe appropriate turns ratios. The dynamic cross-regulation between these multiple outputs is theoretically quite good, because there is no filter inductor in series with each output to spoil the dynamic coupling, as in the buck regulator circuits. However, leakage inductance between the secondaries can severely hurt the cross-regulation, and considerable care must be applied to the design of the inductor in this respect.

The single ended flyback circuit is quite popular at low power levels because of its simplicity and low cost. Its big disadvantage in the discontinuous operating mode is the high peak current in the transistor and the output which makes the filter capacitor problem quite painful. The continuous mode does not quite cut the peak current in half, but brings in other problems such as the RHP zero and difficult compensation methods with poor transient response. In 1983, many sophisticated designers use this flyback technique up to 200-300 Watts.

Push-Pull Boost. This last example--compare the push-pull boost regulator in Figure 8 with Figure 1. The transistors alternately apply the input inductor current to the transformer primary and the outputs. Where is the shunt transistor in the Figure 1 boost regulator that "recharges" the inductor? The two transistors in the primary of the transformer provide this switching function by deliberately making them conduct simultaneously, thus shorting out the primary, when it is desired to recharge the inductor. In this method, which eliminates the need for a third, shunt transistor, the two transistors are either both on, or on individually. They are never both off, as in the push-pull buck regulators. A little innovation in the control-base drive technique is necessary.

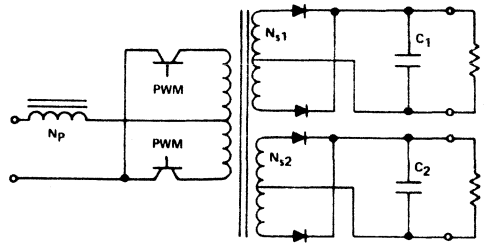


Figure 8. Push-Pull Boost

Like the flyback, the boost regulator has no filter inductor in series with each output, so the dynamic cross-regulation is good.

All boost topologies are inherently "current-fed", because of the inductor in series with the input. Because of this, boost regulators can shrug off temporary downstream fault conditions such as core saturation, poor rectifier recovery, or transistor conduction overlap. All these things do is help recharge the inductor current. Boost converters also generate much less EMI at the input because the input current waveform has small AC content.

RECOMMENDATIONS: For post regulation, point of load regulation and for developing additional voltages from an existing line isolated DC supply (CM = Current mode, FF = Feedforward):

For step-down:	Buck, Continuous, CM
For step-up:	Boost, Discontinuous, FF or CM
For reverse polarity:	Flyback, Discontinuous, FF or CM

For applications that require transformer coupled circuits for isolation and/or multiple outputs:

Under 200 W:	Flyback, Discontinuous, FF or CM
200 W--1 kW:	Forward Converter (Buck), Continuous, CM
Over 1 kW:	Half Bridge, Full Bridge, Continuous, CM

REFERENCES:

1. L. H. Dixon, Jr., "Pulse Width Modulator Control Methods with Complementary Optimization," Powerconversion International, January 1982, pp 14-21.

2. H. Matsuo and K. Harada, "New Energy Storage DC-DC Converter with Multiple Outputs," Solid State Power Conversion, Nov./Dec. 1978, pp 54-56.

THE EFFECTS OF LEAKAGE INDUCTANCE

ON SWITCHING POWER SUPPLY PERFORMANCE

by

Lloyd H. Dixon, Jr.

INTRODUCTION.

Leakage inductance is often the largest single factor in degrading the performance of a switching power supply. The effects of leakage inductance in buck and boost regulators differ markedly from flyback (buck-boost) circuits.

This paper describes the effects of leakage inductance on circuit losses, load regulation and cross-regulation with multiple outputs. Methods of minimizing leakage inductance in practical transformers and coupled inductors are discussed.

Forward Converter. The first example chosen is a forward converter with multiple outputs as shown in Figure 1. Transformer mutual inductance and leakage inductances are not shown. This two-transistor version facilitates non-dissipative clamping of the energy stored in these transformer inductances and also reduces transistor voltage rating requirements. The circuit of Figure 1 is the same as in the 250 Watt Forward Converter Design Review covered separately, with a second output, V_2, providing 15 Volts at 3 Amperes in addition to the original 5 Volt, 50 Amp main output, V_1.

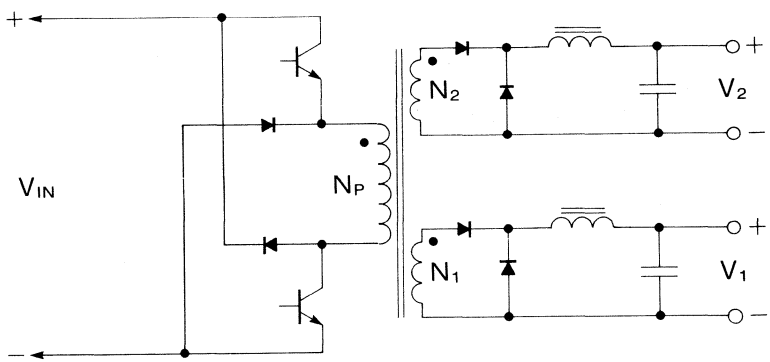
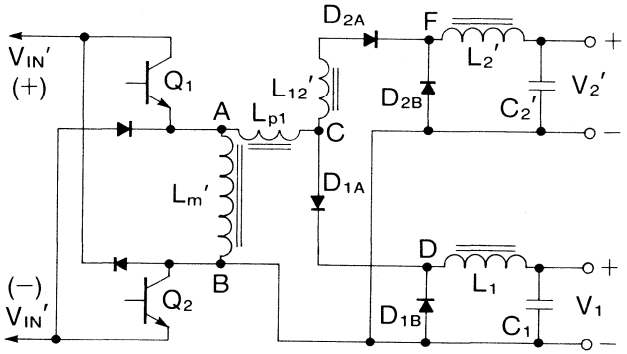


Figure 1. Forward Converter without Parasitic Inductances

In order to simplify the analysis, rectifier and transistor voltage drops are neglected. The effects of the parasitic inductances are most easily analysed in the equivalent circuit of Figure 2, in which the "ideal" transformer is eliminated. This is

accomplished by normalizing the elements of the input and the #2 output according to their turns ratios with respect to the #1 main output:



$$V_{IN}' = V_{IN}(N_1/N_p), \qquad V_2' = V_2(N_1/N_2)$$

$$L_2' = L_2(N_1/N_2)^2, \qquad C_2' = C_2(N_2/N_1)^2, \quad \text{etc.}$$

Figure 2. Forward Converter Equivalent Circuit

L_m' is the normalized mutual inductance of the transformer. L_{p1} is the leakage inductance between the primary and the main secondary, and L_{12}' is the leakage inductance between main and #2 secondaries, all referred to the main secondary, N_1.

Operation with no Leakage Inductance. Circuit operation will first be examined with the assumptions that the leakage inductances L_{p1} and L_{12}' are zero, and the #2 output current, I_2', is also zero. This is the basic buck regulator configuration with added mutual inductance, L_m'.

Referring to the waveforms of Figure 3, filter inductor current, I_{L1}, is the familiar triangular waveform superimposed upon the DC output current, I_1. I_{L1} is carried entirely by rectifier D_{A1} during the "on" time of the switching transistors, t_{on}, and free-wheels through D_{A2} during the transistor "off" time. During t_{on}, voltage V_{DB} at the input of the L-C filter equals V_{IN}', but during the off time V_{DB} is zero. The output voltage of an inductor input filter (with continuous inductor current) always equals the time averaged input voltage, therefore:

$$V_1 = V_{IN}'t_{on}/T \qquad (1)$$

During t_{on}, the input voltage is impressed across the transformer causing a linearly increasing current, I_{Lm}', through the mutual inductance. The maximum value of I_{Lm}' at the end of t_{on} is:

$$\max I_{Lm}' = V_{IN}'t_{on}/L_m' \qquad (2)$$

During t_{on}, normalized transistor current I_{Q1}' is the sum of the filter inductor current, I_{L1}, and the mutual inductance current, I_{Lm}'. During the off time, I_{Q1}' is zero. I_{Lm}' cannot decrease instantaneously. This causes the voltage on L_m' to reverse, forcing I_{Lm}' to flow through the clamp diodes. Thus the energy which was stored in L_m' will be recovered by pumping it back into the input source.

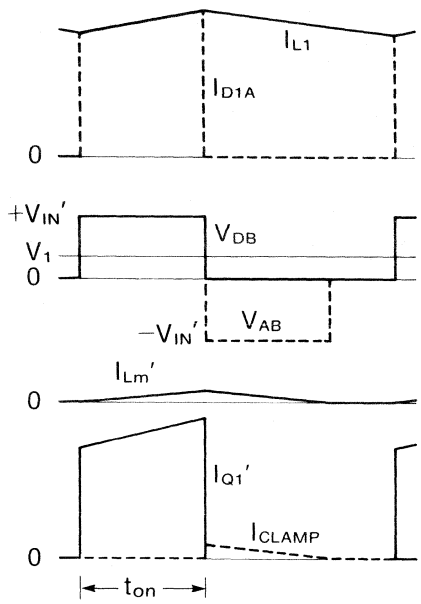


Figure 3.

Since the reverse voltage across L_m' equals V_{IN}', I_{Lm}' will decrease at exactly the same rate that it increased during the "on" time, thereby taking exactly the same time, equal to t_{on}, to reach zero again. This illustrates the fact that in order to reset the core each cycle, the reverse volt-seconds during the "off" time must at least equal the volt-seconds during the "on" time. When the reverse clamp voltage is equal to the forward voltage, as in this case, the duty cycle must be limited to 50% maximum, otherwise I_{Lm}' will continue to rise in subsequent cycles which will cause the core to saturate.

Normally, I_{Lm}' will be less than 10% of the full load current through the switching transistors causing a negligible increase in transistor losses. Likewise, I_{Lm}' has negligible effect upon the open loop line and load regulation. The energy stored in L_m' can result in significant losses if dumped into dissipative clamps. However, this energy can be recovered by clamping to input or output, or otherwise put to good use such as providing auxiliary power for the control and drive circuits.

Using the transformer design of the 250 Watt Forward Converter Design Review as an example, the 92 turn primary and 6 turn secondary result in a turns ratio of 15.33. The minimum V_{IN} of 200 Volts becomes 13 Volts V_{IN}' referred to the secondary. Primary mutual inductance, L_m, is 25mH or a normalized L_m' of 106uH referred to the secondary. From Equation 2, using a maximum t_{on} of 12.5 usec (40 kHz operation), the maximum I_{Lm}' is 1.5 Amps, negligible compared to the 50 Amp peak full load current in the secondary. The energy stored in L_m' equals 5 Watts at 40 kHz. Most of this energy is not lost, but pumped back to the input.

Effects of Leakage Inductance with Single Output. Figure 4 shows the result of introducing a finite value of leakage inductance, L_{p1}, in the #1 main output. Assume D_{2A} is open, completely disabling the #2 output.

L_{p1} has the effect of delaying the transfer of current between D_{1A} and D_{1B} at the beginning and end of the transistor "on" time. Referring to Figures 2 and 4, at the beginning of t_{on}, L_{p1} prevents instantaneous transfer of the filter inductor current to D_{1A}. D_{1B} must continue to conduct a diminishing portion of the filter inductor current during time t_1 while the current through L_{p1} and D_{1A} rises to finally equal I_{L1}. The time required for this current transition, t_1, is simply:

$$t_1 = I_1 L_{p1}/V_{IN}' \qquad (3)$$

Although V_{AB} jumps to V_{IN}' at the very beginning of t_{on}, V_{DB} remains at zero throughout t_1 because D_{1B} remains conducting. With t_{on} fixed (open control loop), output voltage V_1 is reduced by the volt-seconds represented in the shaded area averaged over cycle time, T. The open loop output voltage error is:

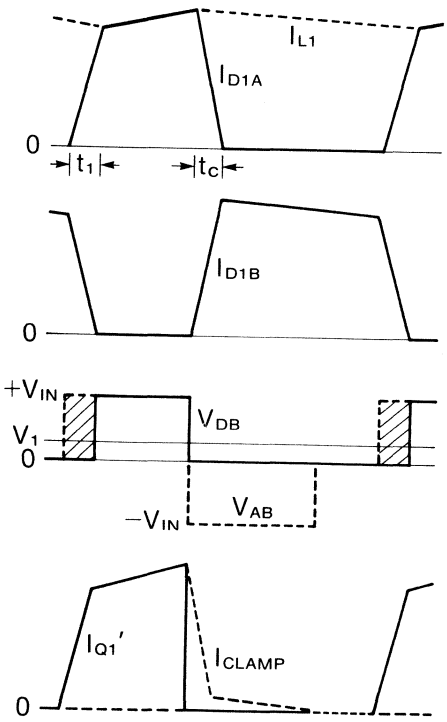


Figure 4.

$$\Delta V_1 = V_{IN}' t_1/T = V_{IN}' I_1 L_{p1}/V_{IN}' T = I_1 L_{p1}/T \qquad (4)$$

Equation 4 shows that the output voltage error varies linearly with load current. Interestingly, the value L_{p1}/T behaves just like an equivalent series resistance: "R_{p1}" = L_{p1}/T.

Energy is taken from the input source during t_1 and stored in L_{p1}:

$$W_{Lp1} = t_1 V_{IN}' I_1/2 = \frac{1}{2} L_{p1} I_1^2 \qquad (5)$$

During time t_c, L_{p1} delays transfer of current back to the free-wheeling rectifier, D_{1B}. D_{1A} and D_{1B} both conduct during t_c, and V_{DB} is zero. This has no effect on the output voltage since V_{DB} is zero in any case at the end of t_{on}.

The voltage across L_{p1} reverses during time t_c in order to maintain its current flow. V_{AB} becomes negative and the current from L_{p1} flows through the clamp diodes (in addition to the mutual inductance current discussed previously). Thus, the energy stored in the leakage inductance is also recovered back to the input.

In summary, the leakage inductance between primary and secondary hurts the open loop load regulation, but this is not usually important because it is easily brought into spec by closing the

loop. The stored energy in the leakage inductance should either be recovered or put to good use, in exactly the same ways as the energy stored in the mutual inductance.

Continuing the 250 Watt Forward Converter example, the 92 turn primary consists of 4 layers of AWG19 wire, and the 6 turn secondary has 10 AWG18 wires in parallel to carry the high current. Assume the primary and secondary are <u>not</u> interleaved, that is, the entire primary is wound, then .01 cm insulation, then the entire secondary. Using the EC52 core, the primary to secondary leakage inductance, L_{p1}, referred to the secondary, is 0.52 uH. Applied to Equation 4, the open loop voltage error of the 5 Volt output will be 1.04 Volts at 50 Amp full load. For correction, a 20% increase in t_{on} will be required under closed loop control. The energy stored in the leakage inductance at full load amounts to 26 Watts at 40 kHz, which will hopefully be recovered by clamping to the input.

If the primary is interleaved with the secondary, i.e., wind two layers of the primary, insulate, entire secondary, insulate, then the remaining 2 primary layers, L_{p1} is reduced dramatically to 0.19 uH. Open loop output voltage error will be only .38 Volts and the energy stored equals 9.5 Watts at 40 kHz.

<u>Effect on Cross-Regulation of Multiple Outputs</u>. The waveforms of Figure 5 show the final step taken of drawing load current I_2' from the #2 output and with a finite value of leakage inductance, L_{12}', between secondaries.

L_{12}' has the effect of causing an <u>additional</u> delay in the transfer of current between #2 output rectifiers D_{2A} and D_{2B}. At the beginning of the "on" time, while current is increasing in L_{p1}, D_{1A} and D_{1B} are both conducting, holding voltage V_{CB} to zero. This means that throughout time t_1 there is no voltage across L_{12}' so that its current cannot start to increase. At the end of t_1, when the current through L_{p1} finally equals I_{L1}, the current through D_{1B} becomes zero and V_{CB} is allowed to rise. Current through L_{12}' and D_{2A} then starts to increase toward I_{L2}', throughout the interval t_2.

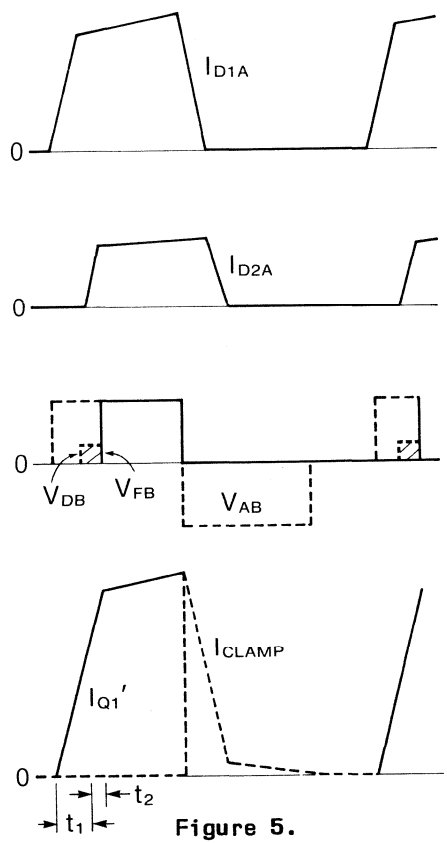


Figure 5.

During t_2, D_{2A} and D_{2B} both conduct, sharing I_{L2}'. V_{FB} is zero because D_{2B} is conducting. The third waveform of Figure 5 shows that during t_2, V_{FB} is zero but V_{DB} is a positive value, the same as V_{CB}. The shaded areas represent the difference in volt-seconds applied to the inputs of the two filters. When averaged over the period T, this equates to a differential or cross-regulation voltage error between outputs 1 and 2. There is no way to correct for this error, other than by post-regulation.

To quantify this error we must know V_{DB} and t_2. At the beginning of t_2, V_{CB} is allowed to rise above zero and current through L_{12}' starts to increase. This same increase in current must also occur through L_{p1}. Thus the two inductors are directly in series during t_2, so that the voltage across each is in direct proportion to its inductance value:

$$V_{DB} = V_{CB} = V_{L12}' = V_{IN}'L_{12}'/(L_{p1}+L_{12}') \quad (6)$$

$$t_2 = (L_{p1}+L_{12}')I_2'/V_{IN}' \quad (7)$$

$$\Delta V_{12}' = V_{DB}t_2/T = I_2'L_{12}'/T \quad (8)$$

Note the similarity to Equation 4. The equivalent series resistance: "R_{12}'" = L_{12}'/T.

In the 250 Watt Forward Converter example using an EC52 transformer core, a portion of the window area allocated to the secondary will be used to add a 15 Volt, 3 Amp winding (45 Watts). Since 6 turns are used for the main 5 Volt winding, the 15 Volt output will require approximately 3 times as many, or 18 turns. It is important that the lower power 15 volt secondary should be wound <u>on top of</u> the higher power 5 Volt winding. The normalized leakage inductance between the secondaries will always be in series with the larger diameter winding because it has greater normalized inductance. Cross regulation voltage error is minimized, because the lower power output will have smaller normalized current changes through the leakage inductance.

The leakage inductance, L_{12}' in series with the outer #2 secondary in the EC52 core is approximately 0.25 microHenries (normalized to the #1 winding). The cross regulation voltage error due to load changes in the 15 volt #2 output may be calculated using Equation 8 either normalized to the 5 volt #1 output or not normalized. The results are:

Turns Ratio, $n = N_2/N_1 = 18/6 = 3$
Period T = 25 µsec

<u>Not Normalized</u>		<u>Normalized</u>
V_2 = 15 V	1/n	V_2' = 5 V
I_2 = 0-3 A	n	I_2' = 0-9 A
L_{12} = 2.25 µH	$1/n^2$	L_{12}' = 0.25 µH
ΔV_{12} = 0.27 V	1/n	$\Delta V_{12}'$ = .09 V

It is worth mentioning a few additional points. In the example

chosen, the leakage inductance between the secondaries is physically located in series with the low power #2 secondary. The effect of changing output #2 load current on cross-regulation has been demonstrated above. However, the cross-regulation due to changing #1 main output load is theoretically perfect. Both outputs will track each other perfectly when load #1 changes, and if #1 is closed loop regulated, both are regulated. This is because there is no intervening impedance to impair cross-regulation in series with the #1 output from the common feed point C in Figure 2. This is why it is important to locate this leakage inductance in series with the low power output which has less effect on cross-regulation.

Cross-regulation can be improved dramatically by winding the secondaries together (multifilar). That is, the wires of all secondaries are co-mingled in the same winding volume, rather than separate discrete secondaries wound on top of each other. This can make the leakage inductance between secondaries so small it becomes negligible. It is sometimes not practical to wind the secondaries multifilar, such as when copper foil is used for one or more secondaries.

It would be desireable to include the primary in the multifilar bundle to reduce the primary to secondary leakage inductance, but this is not practical in off-line applications because of the large turns ratio and the need for high voltage isolation between primary and secondaries.

Wiring inductance between the transformer secondaries and the filter inductor inputs (points D and F in Figure 2) has exactly the same effect as leakage inductance between secondaries; that is, wiring inductance has an adverse effect on cross-regulation. It is vital to minimize wiring lengths wherever the current is discontinuous. This is especially important with low voltage outputs and at higher power levels.

Be aware of the fact that after minimizing leakage and wiring inductances, the DC cross-regulation may be excellent, but the dynamic, or AC cross regulation will be pitifully bad if individual filter inductors are used in each output. This is true for any multiple output buck regulator, because a disturbance on any output is almost perfectly decoupled from all other outputs because of the high AC impedance of the filter inductors.

The solution to this problem is to put all output filter inductor windings on a common single core. This provides excellent AC coupling between the multiple outputs. The turns ratios between these windings must be the same as the voltage ratios between the respective outputs. The only problem with this technique is that slight offsets in voltage caused by rectifier forward drop variations will cause large circulating currents and output ripple at the switching frequency. The problem is solved by deliberately introducing a few percent of leakage inductance between the multiple windings of the filter inductor, which absorbs the voltage variations yet does not interfere significantly with the AC cross-coupling.

THE EFFECTS OF LEAKAGE INDUCTANCE ON MULTI-OUTPUT FLYBACK CIRCUITS

Lloyd H. Dixon, Jr.

A similar topic dealing with buck-derived regulators was presented at previous Unitrode seminars (see Section P2). Leakage inductance is also the major cause of poor cross-regulation in flyback circuits, but the circuit analysis is quite different. This topic shows how to predict and minimize the effects of leakage inductance and wiring inductance in continuous and discontinuous mode flyback regulators.

Introduction: A typical flyback regulator circuit with two outputs is shown in Figure 1. The flyback "transformer" is actually an inductor with multiple windings. While the transistor switch is ON, the inductor draws increasing current from the input and stores this energy. During the ON time, the output rectifiers are reverse biased (note the polarity dots). When the transistor turns OFF, the inductor ampere-turns cannot instantaneously change. The voltages across all inductor windings reverse or "fly back" forcing the ampere-turns that were flowing in the primary to transfer to the secondary windings. The previously stored energy is then delivered to the outputs.

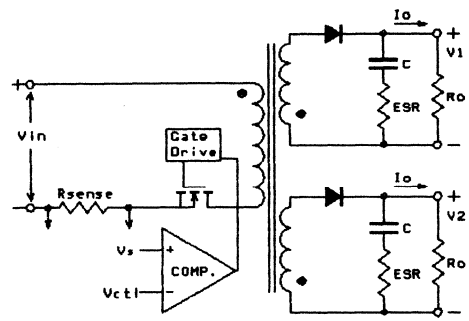
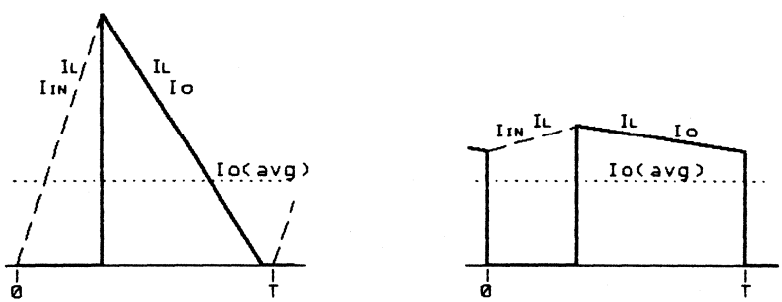


Figure 1 - FLYBACK CONVERTER

A flyback regulator may be operated in the continuous or discontinuous inductor current modes. Idealized current waveforms for the discontinuous mode (at full load) are shown in Figure 2a, which assumes a 1:1 turns ratio. By definition, the inductor current starts at zero at the beginning of each switching period. All of the energy stored during the ON time is delivered to the outputs and the current is back to zero before the end of each period. In the continuous mode shown in Figure 2b, the inductor current is never zero during normal operation, and the inductor holds much more energy than is taken from the input and delivered to the output each switching cycle.



(a) Discontinuous (b) Continuous

Figure 2 - Inductor Current Modes

These two inductor current operating modes have radically different operating characteristics, with divergent opinions by experienced designers as to which mode is better. Note that for the same average output current (same power output), the discontinuous mode reaches nearly twice the peak current required in the continuous mode. However, as indicated by the relative inductor current slopes, the continuous mode typically employs 10 times the inductance value and requires $10/1.8^2 = 3$ times the inductor energy storage capability as the discontinuous mode.

Non-Ideal Aspects: All flyback circuits depend upon inductive energy storage. This is usually accomplished by introducing a small non-magnetic gap in series with the inductor core. Unfortunately, the inductor windings cannot all be equally well coupled to the energy storage gap because of the physical separation between the windings. Additional amounts of magnetic energy are also stored between and within the windings. These amounts of energy are represented in the circuit as leakage inductances.

When the transistor turns off, leakage inductance between transformer primary and secondaries will fight the transfer of current to the secondaries, causing a large voltage spike to occur across the transistor. This inductive spike must be clamped to a voltage level less than the transistor rating or the transistor will be destroyed. (Figure 1 does not show this necessary clamp.) There are many possible clamping methods -- with some, the energy put into the clamp is lost, hurting circuit efficiency, with other methods the clamp energy is conserved. The two-transistor 150 Watt Flyback Regulator Design Review (Section A3) saves this energy by returning it to the input.

Leakage inductance between secondaries, together with wiring inductances from each secondary to its respective filter capacitor, are the main cause of poor cross-regulation between the outputs.

Circuit diagrams such as Figure 1 seldom show these many parasitic inductive elements which play such an important role in flyback circuit performance. Circuit analysis becomes complex and confusing when all these elements are included, compounded by the differing turns ratios between the windings.

The Normalized Equivalent Circuit: Considerable simplification is possible as shown in the normalized equivalent circuit of Figure 3. In the normalized circuit, the actual circuit values associated with each winding have been translated according to the actual turns ratios into equivalent circuit values with 1:1 turns ratios. Since input-output isolation is not relevant to this analysis, the ideal 1:1 transformer may then be discarded and the windings directly interconnected. When the analysis is completed, the resulting values may be "de-normalized" to their actual values according to the turns ratios.

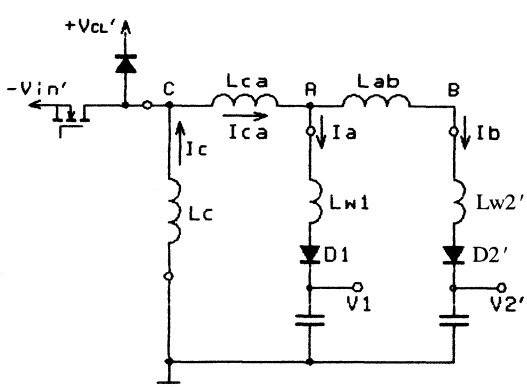


Figure 3 - Normalized Circuit

For example, assume an off-line regulator with a 30:1 turns ratio between primary and 5V secondary, and a 3:1 turns ratio between 15V secondary and the 5V secondary. Normalization may be with respect to any winding. In this case, all windings are normalized to the 5V winding by dividing each voltage and multiplying current by the actual turns ratio. Inductance and resistance are divided and capacitance multiplied by the turns ratio squared. Referred to the 5V secondary, a V_{in} of 300V divided by the turns ratio of 30 translates to V_{in}' of 10V. Primary inductance of 450µH divided by 30^2 becomes 0.5µH. The V2 of 15V at 4A secondary becomes V2' of 5V at 12A, etc.

The normalized circuit of Figure 3, mutual inductance L_C represents energy stored in the gap, L_{ca} represents leakage inductance between primary and secondary A, and L_{ab} is the leakage inductance between secondaries A and B. Mutual inductance L_C is connected directly to V_{in}' through the transistor or to V_{CL}' through the clamp diode, whereas outputs V1 and V2' are coupled to L_C through leakage inductances and secondary wiring inductances L_{w1} and L_{w2}. Primary wiring inductance is negligible because it is divided by 30^2. This Figure 3 configuration applies when the primary winding is closest to the gap -- either inside the secondaries with the centerleg gapped or outside the secondaries with the outer leg gapped. If the primary were on the other side of the secondaries opposite the gap, the equivalent circuit would have L_C connected to point B instead of point C.

To further simplify the analysis, output ripple voltages are assumed to be zero. The error caused by this assumption is small in a practical power supply and its effect nearly averages out over a complete switching period.

Energy Lost to the Clamp: The continuous mode waveforms of Figure 4 show two non-ideal occurrences, both caused by leakage and wiring inductances which fight the transfer of current from primary to secondary when the transistor switches on and off. The leakage inductances plus wiring inductances are normally a small fraction of the primary inductance L_C. Assuming V1 and V2' are substantially equal, the leakage and wiring inductances may be combined:

$$L_{ps} = L_{ca} + \frac{L_{w1}(L_{ab}+L_{w2}')}{L_{w1}+L_{ab}+L_{w2}'}$$

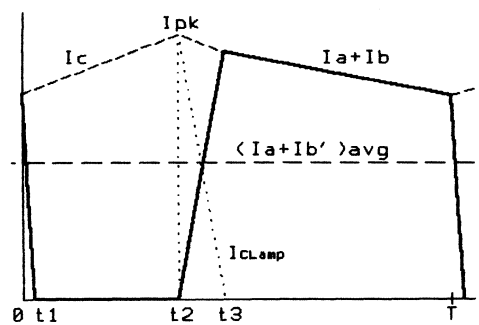


Figure 4 - Current Transfer

Immediately before the transistor turns on at t_0, inductor current I_C equals I_{ca} and flows through L_{ps} to the outputs. At t_0, the transistor pulls point C down to $-V_{in}'$. However, I_{ca} cannot instantaneously decrease, which prevents I_C from immediately transferring to the input. The time required for I_{ca} to reach zero and I_C transfer to be completed is (neglecting diode drops):

$$t_1 = (V_{in}'+V_1)/L_{ps} \quad (1)$$

Some of the energy in L_{ps} when the transistor turns on transfers to L_C, the rest goes to the output - none is lost.

This turn-on transfer problem cannot occur in the discontinuous inductor current mode because I_{ca} is always zero before the transistor switches on.

A much more serious transfer delay occurs when the transistor switches off at time t_2. At t_2, inductor current Ic is at its maximum peak value, but current I_{ca} through L_{ps} is zero. The voltage across L_C reverses in an attempt to force I_C through L_{ps}. I_{ca} cannot change instantaneously, so L_C forces its current into the clamp. I_{ca} rises according to the voltage $V_{CL}'-V1$ across L_{ps}, and I_{CL}' decreases in a complementary manner as shown in Figure 4. The transfer time is:

$$t_3-t_2 = I_{c(pk)}\frac{L_{ps}}{V_{CL}'(1+L_{ps}/L_C)-V_1} \qquad (2)$$

With V1 = V2' = Vout, the energy transferred into the clamp is:

$$W_{clamp} = \frac{L_{ps}I_{pk}^2}{2} \cdot \frac{1}{1+L_{ps}/L_C-V1/V_{CL}'} \qquad (3)$$

This equation also applies to the discontinuous inductor current mode. It also may be used (with a small error) when the primary winding is opposite the gap, or when the primary is split and interleaved on both sides of the secondaries. (Interleaving will reduce L_{ca} by a factor of 3 and accordingly reduce the energy lost to the clamp.)

The energy diverted from the output to the clamp hurts open loop load regulation, but this is not very significant because the closed loop feedback easily corrects for this. But in order to maintain reasonable efficiency in flyback supplies of more than a few Watts output this energy must be recovered in some way rather than allow it to be dissipated. The two-transistor circuit shown in Section A3 accomplishes this quite easily with a pair of cross-connected diodes which return the energy to the Vin source. Single transistor flyback circuits usually employ a single diode with an added winding bifilar with the primary. Even when the clamp energy is conserved, it should be minimized because it increases the current in the transistor and the energy storage requirement of the flyback transformer.

As equation (3) reveals, the energy delivered to the clamp equals the energy stored in the primary-secondary leakage inductance, L_{ps}, <u>increased</u> by the fraction on the right whose denominator is usually considerably less than 1. The L_{ps}/L_C term is almost negligible, but $V1/V_{CL}'$ is 0.5 when the clamp voltage is twice V1 (as in the example used). In this case, the energy sent to the clamp is <u>twice</u> the energy stored in L_{ps}. In order to minimize the energy diverted to the clamp, it is important to (1) minimize L_{ps} which consists of leakage inductances and wiring inductances, (2) make the clamp voltage V_{CL}' as large as possible compared to V1 (but this will increase the transistor V_{CE} requirements).

Table I shows that in the same application — 100 W, 100 kHz — the discontinuous mode circuit puts only 8.48 Watts into the clamp vs. 15.99 Watts

for the continuous mode. Even though Ipk in the discontinuous mode is almost twice as large, primary-secondary inductance L_{ps} is 6 times smaller which gives the advantage to the discontinuous mode. The L_{ps} would be even smaller fovoring the discontinuous mode even more but the wiring inductance which is the same in both circuits is a much more significant portion of the discontinuous mode L_{ps}.

Cross-Regulation in the Continuous Mode:

Figure 5 shows the secondary current waveforms of the two-output flyback circuit of Fig. 3 operated in the continuous inductor current mode and with equal normalized output voltages (V1 = V2'). L_C+L_{Ca} together force current I_C into both outputs. The division of this current between the two outputs is determined by the inductances L_{W1} and $L_{ab}+L_{W2}'$ in series with the outputs.

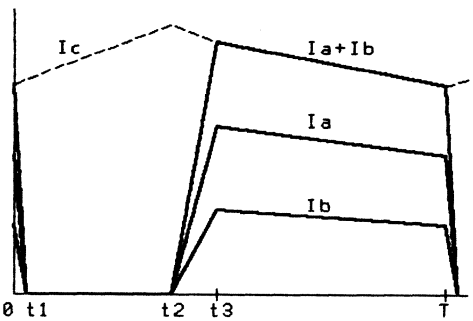


Figure 5 - Two Outputs, V1 = V2'

Let output #1 inductance L1 = L_{W1}, and output #2 inductance L2 = $L_{ab}+L_{W2}'$.
At the beginning of the off time, point C is at Vclamp. The voltages across L1 and L2 are equal. At the beginning of the OFF time (t_3), peak I_C divides into I_a and I_b:

$$I_a = \frac{I_C \cdot L2}{L1+L2} \; ; \qquad I_b = \frac{I_C \cdot L1}{L1+L2} \tag{4}$$

Let $L_t = L_C+L_{Ca}$. After current transfer to the secondaries is completed at t_3, L_t freewheels across V1 (=V2'), forcing current I_C into the parallel combination of L1 and L2. The downslope of Ic and the average I_C (=I_a+I_b) is determined by Vout across L_t. L1 and L2 have almost no effect on the total output current because L_t is very much larger than L1 and L2 in parallel. The total output current I_C (I_a+I_b) is maintained by the control loop at the level required to keep the output voltages in regulation.

With V1 = V2', the voltages across L1 and L2 are equal during the entire OFF time, so that not only are the peak I_a and I_b values proportioned to peak I_C according to the inductor ratios of equation 4, but their current slopes and average output currents have the same proportional relationships.

So with zero output voltage differential, the average currents I_a and I_b are apportioned strictly by L1 and L2 as per equation 3 and their ratio is inversely proportional to the inductances:

$$I_a/I_b = L2/L1$$

However, the actual load currents cannot be expected to observe the ratio established above. To change the I_a/I_b ratio consistent with actual load current requirements requires a small differential voltage, ΔV_{12}, between output voltages V1 and V2. This differential is so small compared to V1 and V2 that it has negligible effect on the total current I_a and I_b, but it will cause the current slopes in L1 and L2 to diverge, changing the apportionment of average current between I_a and I_b.

Figure 6 shows what happens when I_b is reduced by 25% below the value set by the inductor ratio. The dash line shows the current waveforms when Vl = V2', as in Figure 5. Suppose I_b=6A, I_a=12A so that I_c=18A. If the load on output #2 changes causing I_b to drop 25% to 6A but I_a stays at 12A, then I_c must drop by the same 2A to 16A. The control loop will make this happen. However, if Vl remains equal to V2' I_a and I_b will drop proportionately, by 1.333A and .667A respectively, as shown by the dotted lines. In order to reduce I_b by 2A and keep I_a at the original level, a small differential voltage ΔV_{12} will appear between Vl and V2. V2 will become more positive than Vl, increasing the I_b downslope and in this case causing I_a to slope upwards. The solid lines in Figure 5 show the resulting waveforms. Note that the slopes change but not the initial peak values.

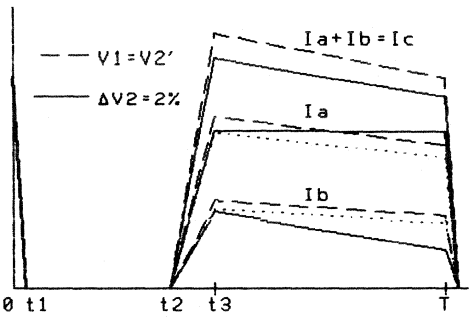


Figure 6 - Two Outouts, ΔV2 = 2%

The voltage differential ΔV_{12} is the output voltage cross-regulation error accompanying the change in load current on one output. The error will appear in whichever output is <u>not</u> sensed and regulated by the control circuit, regardless of which output experiences the load change. The magnitude of the cross-regulation error is:

$$\Delta V_{12} = \frac{2\Delta I_b \cdot L2}{T(1-D)^2} = -\frac{2\Delta I_a \cdot L1}{T(1-D)^2} \quad ; \qquad (1-D) = Vin/(Vo+Vin) \qquad (5)$$

Where D is the duty cycle and T the switching period = $1/f_s$. In the continuous mode example given in Table I, Ll is .02 µH while L2 is .07+.012 = .082 µH. With ΔV_{12} = 0, I_a/I_b = .082/.02 = 4/1. Having I_a 4 times greater than I_b with ΔV_{12} = 0 is probably acceptable if output #1 has most of the load power requirement of the supply, because a relatively small ΔV_{12} can make the necessary adjustment. (Normalized load currents are proportional to load power because the normalized voltages are the same.)

With D=.36 and T=10µsec, equation 5 predicts ΔV_{12} of .01V for a 1A change in I_a (10 mΩ). This is a 0.2% change in voltage for an 8.33% change in current. For a 1A change in I_b the voltage differential is -.04V (40 mΩ). This is a .8% change in voltage for a 16.7% change in current. If the #1 output is actually 15V with a 3:1 turns ratio, the latter translates to an actual .12V differential for a 1/3 A change, or 0.36Ω.

Note that equation 5 shows a linear relationship between current and voltage changes. But be careful. If ΔV_{12} becomes too large, the I1 or I2 downslope may reach zero current before the end of the switching period. The output reaching zero becomes discontinuous and the cross-regulation becomes much worse. Equation 5 no longer applies. If the output that becomes discontinuous is sensed for closed loop control, the loop gain characteristics probably change (this has not been evaluated).

Equation 5 also shows that cross-regulation improves when duty cycle D is smaller, which occurs with high Vin.

Cross-regulation in the Discontinuous Mode:
The waveforms of Figure 7 show the secondary currents of the Figure 3 flyback circuit operated in the discontinuous mode with V1 = V2' ($\Delta V_{12} = 0$). The peak values, the downslope and the average current values are all proportioned the same as determined by L1 and L2, just as with the continuous mode. Equation 4 applies to the discontinuous mode, as well. However, in the discontinuous mode, all the inductor values are much smaller (except for wiring inductance) so that the slopes are much steeper, and the peak current is nearly twice the discontinuous mode. Transfer time t_3-t_2 is much shorter and less energy goes to the clamp.

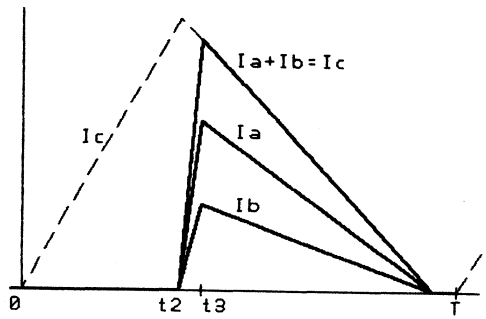


Figure 7 - Two Outputs, V1 = V2'

In the discontinuous mode example given in Table I, L1 and L2 are both .02µH, dominated by winding inductances. This means that with V1=V2, I_a and I_b are equal (not as shown in Figure 7). If ΔV_{12} is changed to decrease I_a and increase I_b, the current waveforms in an actual flyback circuit will look like Figure 8. The current in one secondary looks like a spike, while the other secondary has a rounded waveform. The curvature is because of small voltage changes across the output capacitors and their ESRs. In spite of the strange shape, the normalized currents add up to the expected triangular waveform.

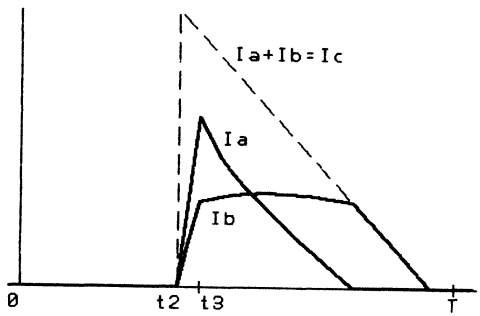


Figure 8

Figure 9 shows the situation of Figure 7 with I_b reduced in current and I_a constant. The explanation of its behavior is similar to the continuous mode example of Figure 6. If I_b is decreased by 2A and I_a stays the same, then the control circuit must reduce I_c by 2A. But this will cause the average I_b and I_a to decrease proportionately by .667A and 1.33A respectively as shown by the dotted lines. So an output voltage differential ΔV_{12} is necessary in order to decrease the downslope of I_a to maintain its original average value, and increase the downslope of I_b to reduce its average value by the desired 2A.

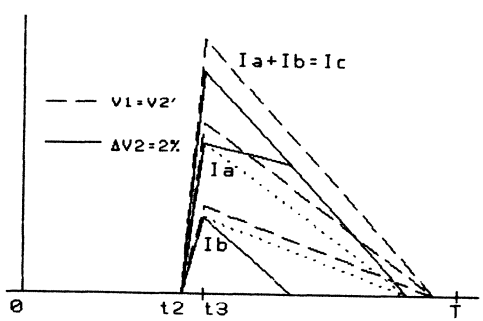


Figure 9 - Two Outputs, $\Delta V2'$ = 2%

Compared to the continuous mode, there is one big difference: In the discontinuous mode, one triangle becomes a trapezoid (I_a), while the other triangle gets a smaller base. The relationship between voltage changes and current changes is much more complex and non-linear:

$$\Delta I_a = \frac{I_{a0}}{(Vl \cdot Lp/(\Delta V_{12} L_t) + 1)} \quad ; \quad \Delta I_b = \frac{I_{b0}}{(Vl \cdot Lp/(\Delta V_{12} L_t) + 1)} \qquad (6)$$

Where Lp is the parallel combination of Ll and L2. ΔI is solved in terms of ΔV rather than the other way around because the equation is much simpler. Because of the non-linearity of the ΔV-ΔI relationship, the changes must all be calculated from a specific starting condition, which is with Vl = V2 (ΔV=0), as depicted in Figure 7. I_{a0} and I_{b0} are the average values under this condition, which must be predefined.

For the example given in Table I, I_{a0}/I_{b0} = L2/Ll = .02/.02. Therefore I_{a0} equals I_{b0}. Taking an arbitrary starting point of 9A total normalized output current, I_{a0} and I_{b0} will both equal 4.5A. Using equation 6, ΔV_{12} calculates to be .019V (.019mΩ). Note from the form of equation 6 that ΔI_a changes proportional to the starting value of I_{a0} with ΔV_{12} fixed. Thus a ΔV_{12} of .019V will support a 2A ΔV_{12} if I_{a0} and I_{b0} are raised to 9A (.0095mΩ).

TABLE I -- DISCONTINUOUS VS. CONTINUOUS MODE EXAMPLE

Input: 100 W , f_s: 100 kHz Refer to Figure 3

	Continuous Mode		Discontinuous Mode	
	Actual	Normalized	Actual	Normalized
Core Type, (Area Product	EC35 (AP=.94)		LP22/13 (AP=.33)	
Primary: Turns	180	6	60	2
V_{in}	-300	-10	-300	-10
$I_{in(pk)}$	1.1	33	2.0	60
V_{CL} (clamp)	300	10	300	10
Output 1: Turns	6	6	2	2
Vl	5	5	5	5
Il	12	12	12	12
Output 2: Turns	18	6	6	6
V2	15	5	15	5
I2	2	6	2	6
Windings are not interleaved				
L_c		5 µH		0.5 µH
L_{ca}		.14 µH		.016µH
L_{w1}	.02	.02	.02	.02
L_{ab}		.07		.008
L_{w2}	.11	.012	.11	.012
L_{ps}		.156		.026
L_{12}		.1		.04
Watts into clamp:	15.99	15.99	8.48	8.48 W

How to Calculate the Amount of Leakage Inductance: Leakage inductance represents the energy storage between two windings. It may be roughly calculated from the winding geometry, using the inductance formula:

$$L = N^2 \mu_o \mu_r \cdot \text{Area/Length} \times 10^{-2}$$

In the S.I. system of units, $\mu_o = 4\pi \cdot 10^{-7}$. For the non-magnetic materials between and within the windings, $\mu_r = 1$. For concentric coils, "Area" is the cross-section in cm^2 of the hollow cylindrical shape between the windings (the distance from the middle of one winding to the middle of the other, multiplied by the average length of one turn). "Length" is the length of the cylindrical shape -- the length of the winding in cm^2, or the breadth of the winding window. N is the number of turns in the whichever winding the leakage inductance will be referenced to. With the windings normalized, it doesn't make any difference.

How to Minimize Leakage Inductance:

1. Windings must be long and thin (few layers) for intimate coupling. Pot cores have very poor window form factor - windings are short and thick. Ferrite ETD and LP cores are good. Mo-Permalloy powder toriods provide the best winding form factor but they are probably too lossy for use in discontinuous mode applications because of the large flux swings involved.

2. Secondaries must be tightly coupled to get good cross-regulation. Wind multifilar, otherwise as close together as possible. Don't sandwich the primary between two secondaries. This reduces eddy current losses but hurts cross-regulation.

3. Primary to secondary leakage inductance does not hurt cross-regulation, but it does divert much of the inductor energy into the clamp. In off-line applications, insulation requirements force significant area between primary and secondary windings which cam make the leakage inductance quite large. If necessary, interleave the primary and secondaries by putting on half the primary turns, then all the secondaries, then the other half of the primary turns outside the secondaries. The primary halves must be series connected. (Never parallel windings that are at different levels in the winding structure or large circulating current will result.) Interleaving will reduce primary-secondary leakage inductance by a factor of three, but it reduces the leakage inductance between secondaries very little and therefore has little effect on cross-regulation.

How to Minimize Wiring Inductance: Wiring inductance is especially critical in low voltage, high current outputs.

1. Minimize the area enclosed by the loop from the transformer secondary through the rectifier to the filter capacitor and back to the secondary. Keep the distances as short as possible and keep the outward and return conductors very close to each other. A ground plane is no good for the return path unless the outward conductor is held very close to it.

2. Don't use round wire, use flat strip or braid with their breadths facing each other as closely as possible. Two copper strips 1 cm wide and 10 cm long spaced 0.3 cm apart have a total inductance of 20 nH. Spread apart, the inductance will rise to 100 nH.

What Sequence for the Secondaries: Referring to Figure 3, with zero differential between the normalized output voltages, the output currents will divide according to the ratio of inductances L_{w1} vs. $L_{ab}+L_{w2}'$. A high voltage output will usually have much lower normalized wiring inductance (because it is reduced by N^2). If the high voltage output is in position 1 with the closest coupling to the primary, it will take most of the normalized current (and power output). A large differential offset will be required to force power to output #2 to achieve a better balance.

Because the low voltage output has higher normalized wiring inductance, it usually makes sense to put it in the #1 position closest to the primary, where its wiring inductance helps to balance out leakage inductance L_{ab}. This will provide better distribution of power without requiring as much output voltage offset. Better balance can be achieved by deliberately increasing wiring inductance selectively, but this will hurt cross-regulation.

9/86

Magnetic Amplifier Control for Simple, Low-Cost, Secondary Regulation

Regulating multiple outputs of a switching power supply has always presented an additional challenge to the designer. With a single pulse-width modulated control system, how can the control loop be configured to keep all outputs in regulation when each may have varying loads? Although it is sometimes possible to average an error signal from each output — degrading the regulation on some outputs to improve on others — a more common approach, as shown in Figure 1, is to close the overall power supply loop to the output with the highest load current and opt for some form of auxiliary — or secondary — regulation for all the other outputs.

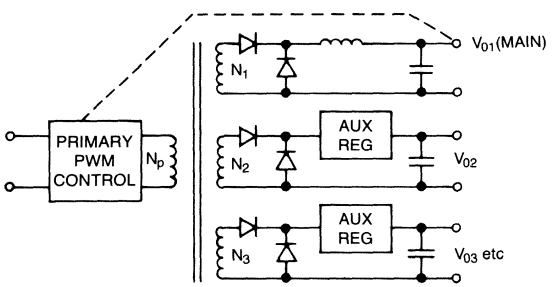


Figure 1. A typical multiple output power supply architecture with overall control from one output.

Secondary Regulators

The problem with multiple outputs originates from the fact that the open-loop output impedance of each winding, rectifier, and filter set is not zero. Thus, if one assumes that the overall feedback loop holds the output of V_{01} constant, then the energy delivered to N_1 must increase with increasing load on that output. This is accomplished by increasing the duty cycle on N_P which, of course, is seen by all the secondaries causing the unregulated outputs to rise.

Similarly, a changing load on one of the unregulated outputs will cause a direct change in that output as a function of its output impedance. Since the overall feedback loop is not sensing this output, no correction can take place. While these problems are minimized by closing the feedback loop on the highest power output, they aren't eliminated in any multiple output supply which sees varying loads. Using secondary regulators on each output other than the one controlled by the feedback loop is the usual solution. One additional benefit of these regulators, particularly as higher frequencies reduce the transformer turns, is to compensate for the fact that practical turns ratios may not match the ratio of output voltages.

Clearly, adding any form of regulator in series with an output adds additional complexity and power loss. The challenge is to minimize both. Before getting into mag amps, it is worth discussing some other commonly used solutions to this problem.

Linear Regulators

Linear regulators usually trade efficiency for simplicity. There is always an added power loss equal to the input-output voltage differential across the regulator times the load current passing through it. Since these are DC regulators, a rectifier-filter must preceed the regulator as shown in Figure 2. There are at least three reasons why the use of linear regulators may be an acceptable choice.

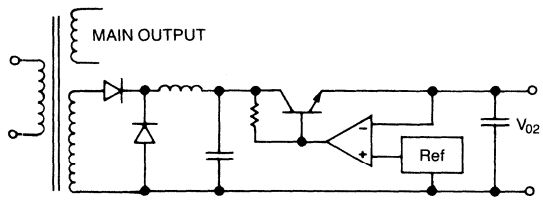


Figure 2. Secondary regulation by means of a linear, DC regulator.

1. Since our premise is that these regulators would be used on the lower power outputs, their power losses may be a small percentage of the overall power supply losses.
2. The fact that a secondary regulator needs only to compensate for the non-zero output impedances of the various outputs means that its input need not see a widely varying input voltage level.
3. There have been "high-efficiency" linear regulators introduced, such as the UC3836 shown in Figure 3, which allows the minimum input voltage to go down to less than 0.5 volts over the output voltage. With a low minimum ($V_{IN} - V_O$), the average value can also be low, offering significant power savings.

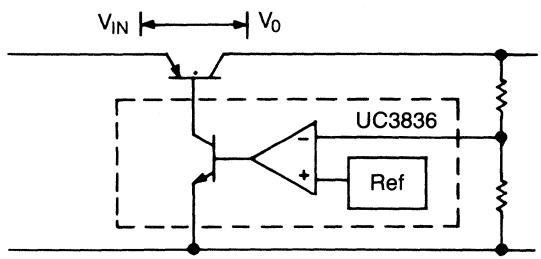


Figure 3. The UC3836 provides a more efficient linear regulator by minimizing the minimum input-output differential.

The advantages of a linear regulator are simplicity, good regulation unaffected by other parts of the power supply, and lowest output ripple and noise.

Independent Switchers

A second type of commonly used secondary regulator is some kind of switching DC to DC converter — usually a buck regulator as shown in Figure 4. In the past, this approach was often used when load current levels made the power loss of a linear regulator unacceptable. The disadvantage of the complexity over a linear regulator has been minimized with the availability of several integrated circuit products. Figure 4, for example, shows the combination of a PIC-600 power stage and a UC3524 PWM controller, usable for load currents to 10 amps. An equally popular solution is Unitrode's L296 4-amp buck regulator. The obvious advantage of a switcher is potentially higher efficiency; however, there are also several disadvantages:

1. In their simplest form, these are generally DC to DC converters meaning that as an independent secondary regulator, an additional rectifier and LC filter would be needed at the input.
2. To alleviate the above problem, a pulse regulation technique could be used, but this introduces problems with frequency synchronization to the primary switching frequency.
3. This, in turn, can lead to another problem. Since most IC regulators use trailing-edge modulation, a primary side current mode controller can become confused with secondary switchers as the primary current waveform may not be monotonic.
4. And finally, the power losses of a switcher are not zero and making them insignificant to the total power supply efficiency may not be a trivial task.

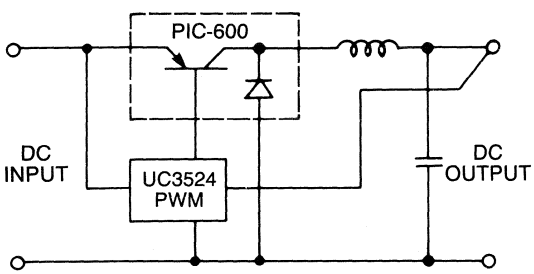


Figure 4. A secondary buck-type switching regulator is most easily implemented with a PIC-600 power module and an IC controller.

There are at least two applications where some type of switcher would clearly be the best solution. One is where other considerations require something besides a step-down converter. For example, a higher voltage could be generated by using a boost configuration switching regulator.

A second usage for a switcher is for very low output voltages — 5 volts or less. Here the use of a BISYN® low-voltage, synchronous switch allows operation right off the secondary winding, eliminating both the rectifier diodes and the input LC filter. In this respect, a BISYN operates similar to a mag amp and can be a very efficient low-voltage secondary regulator.

Magnetic Amplifiers

Although called a magnetic amplifier, this application really uses an inductive element as a controlled switch. A mag amp is a coil of wire wound on a core with a relatively square B-H characteristic. This gives the coil two operating modes: when unsaturated, the core causes the coil to act as a high inductance capable of supporting a large voltage with little or no current flow. When the core saturates, the impedance of the coil drops to near zero, allowing current to flow with negligible voltage drop. Thus a mag amp comes the closest yet to a true "ideal switch" with significant benefits to switching regulators.

Before discussing the details of mag amp design, there are a few overview statements to be made. First, this type of regulator is a pulse-width modulated down-switcher implemented with a magnetic switch rather than a transistor. It's a member of the buck regulator family and requires an output LC filter to convert its PWM output to DC. Instead of DC for an input, however, a mag amp works right off the rectangular waveform from the secondary winding of the power transformer. Its action is to delay the leading edge of this power pulse until the remainder of the pulse width is just that required to maintain the correct output voltage level. Like all buck regulators, it can only substract from the incoming waveform, or, in other words, it can only lower the output voltage from what it would be with the regulator bypassed.

As a leading-edge modulator, a mag amp is particularly beneficial in current mode regulated power supplies as it insures that no matter how the individual output loading varies, the maximum peak current, as seen in the primary, always occurs as the pulse is terminated.

Mag Amp Operation

Figure 5 shows a simplified schematic of a mag amp regulator and the corresponding waveforms. For this example, we will assume that N_S is a secondary winding driven from a square wave such that it provides a ± 10 volt waveform at v_1. At time $t = 0$, v_1 switches negative. Since the mag amp, L1, had been saturated, it had been delivering +10V to v_3 prior to $t = 0$ (ignoring diode drops). If we assume $v_C = -6V$, as defined by the control circuitry, when v_1 goes to −10V, the mag amp now has 4 volts across it and reset current from v_C flows through D1 and the mag amp for the 10 μsec that v_1 is negative. This net 4 volts for 10 μsec drives the mag amp core out of saturation and resets it by an amount equal to 40V-μsec.

When $t = 10$ μsec and v_1 switches back to +10V, the mag amp now acts as an inductor and prevents current from flowing, holding v_2 at 0V. This condition remains until the voltage across the core — now 10 volts — drives the core back into saturation. The important fact is that this takes the same 40 volt-μsec that was put into the core during reset.

When the core saturates, its impedance drops to zero and v_1 is applied to v_2 delivering an output pulse but with the leading edge delayed by 4 μsec.

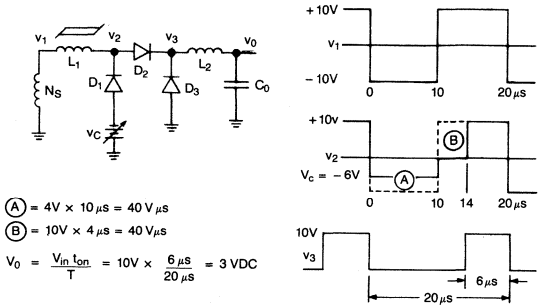


Figure 5. A simplified mag-amp regulator and characteristic waveforms.

Figure 6 shows the operation of the mag amp core as it switches from saturation (point 1) to reset (point 2) and back to saturation. The equations are given in cgs units as:

N = mag amp coil turns
Ae = core cross-section area, cm²
ℓe = core magnetic path length, cm
B = flux density, gauss
H = magnetizing force, oersteads

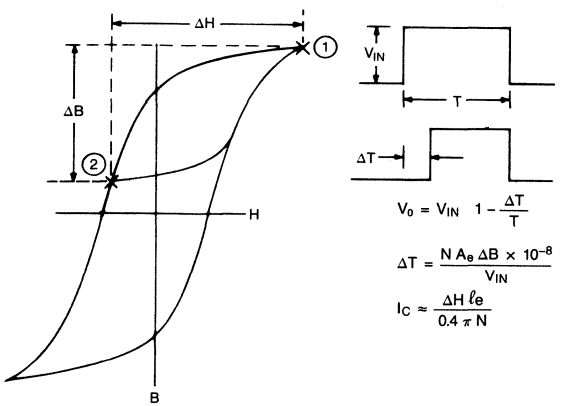


Figure 6. Operating on the B-H curve of the magnetic core.

The significance of a mag amp is that reset is determined by the core and number of turns and not by the load current. Thus, a few milliamps can control many amps and the total power losses as a regulator are equal to the sum of the control energy, the core losses, and the winding I²R loss — each term very close to zero relative to the output power.

Figure 7 shows how a mag amp interrelates in a two-output forward converter illustrating the contribution of each output to primary current. Also shown is the use of the UC1838 as the mag amp control element.

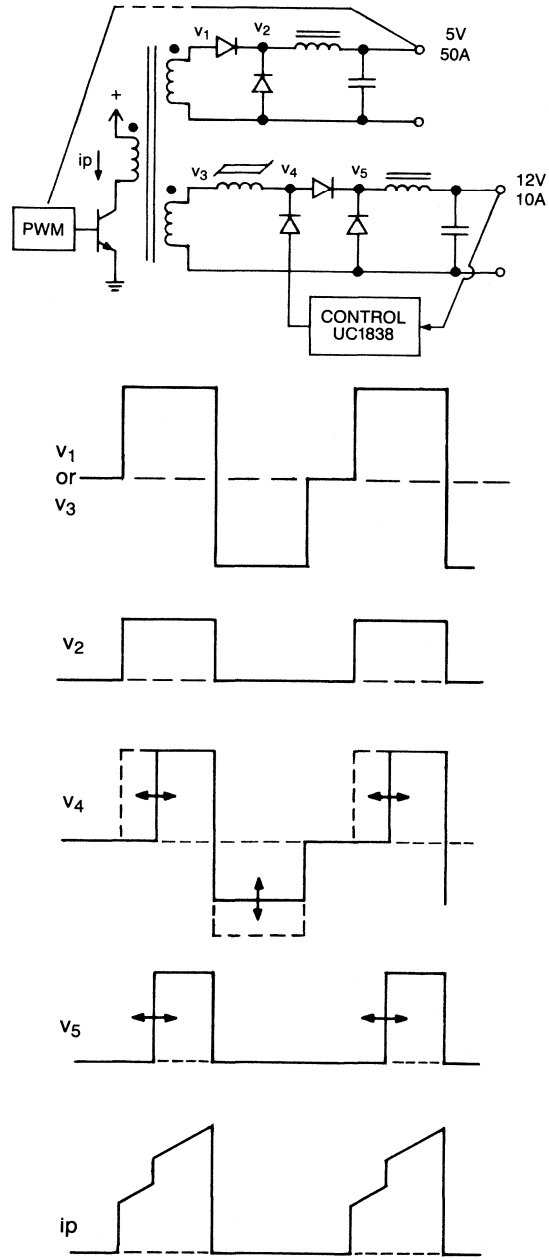


Figure 7. Control waveforms for a typical two-output, secondary regulated, forward converter.

The UC1838 Mag Amp Controller

This IC has been designed specifically as a controller for mag amp switching regulators. Its block diagram of Figure 8 shows three functions:

1. An independent, precision, 2.5V reference
2. Two identical operational amplifiers
3. A PNP output driver

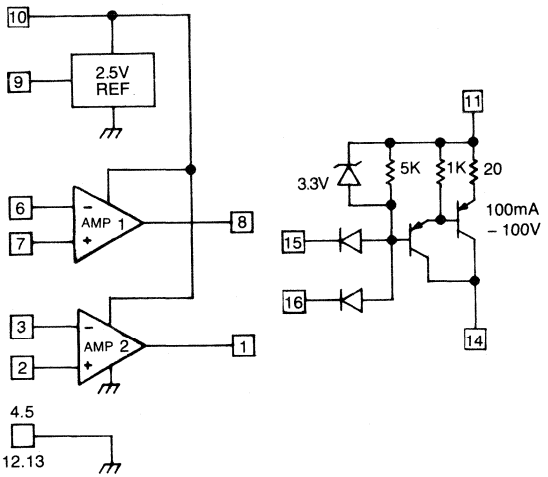


Figure 8. The block diagram of the UC1838 mag-amp control integrated circuit.

The reference is a band gap design, internally trimmed to 1%, and capable of operating with a supply voltage of 4.5 to 40 volts. The op amps are identical with a structure as shown simplified in Figure 9. These have PNP inputs for a common mode input range down to slightly below ground, are internally unity-gain compensated for a bandwidth of 800 KHz, and have class A outputs with a 1.5mA current sink pull-down. The open-loop voltage gain is 120db to a single pole at 1 Hz with an additional phase lag of 15° at 1 MHz. Two op amps are included to provide several options. For example, if one is used to close the voltage feedback loop, the other can be dedicated to some protection function such as current limiting or over-voltage shutdown. Alternatively, if greater loop gain is required, the two amplifiers could be cascaded.

The PNP output driver can deliver up to 100 mA of reset current with a collector voltage swing of as much as 100V negative (within the limits of package power dissipation). Remembering that the mag amp will block more volt-seconds with greater reset, pulling the input of the driver low will attempt to reduce the output voltage of the regulator. Thus, there are two inputs, diode "OR"ed to turn-on the driver, turning-off the supply output. When operating as a current source, the response of this driver circuit is flat to one megahertz, at which point it has introduced 90° of phase shift.

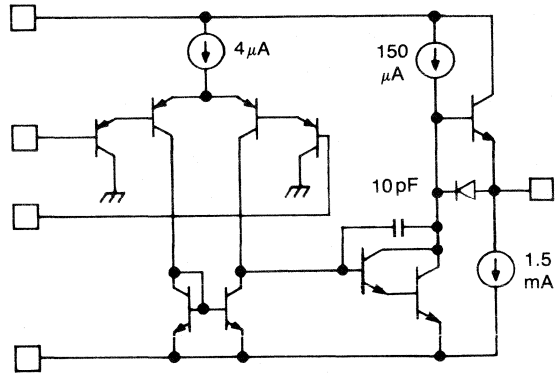


Figure 9. Simplified schematic of each of the operational amplifiers contained within the UC1838.

Current limiting of the output driver is achieved by means of the 3.5V zener clamp (which is temperature compensated to match two V_{BE}'s) in conjunction with the 20Ω emitter resistor. Pin 11 of the driver can be connected to any convenient voltage source from 5DVC to the level used for Pin 10.

Mag Amp Design Principles

One of the first tasks in a mag amp design is the selection of a core material. Technology enhancements in the field of magnetic materials have given the designer many choices while at the same time, have reduced the costs of what might have been ruled out as too expensive in the past. A comparison of several possible materials is given in Figure 10. Some considerations affecting the choices could be:

1. A lower Bmax requires more turns — less important at higher frequencies.
2. Higher squareness ratios make better switches
3. Higher I_M requires more power from the control circuit
4. Ferrites are still the least expensive
5. Less is required of the mag amp if it only has to regulate and not shut down the output completely.

MATERIALS

Example: Similar Toroids, 1" O.D., 0.75" I.D., 0.25" High, 25KHz, 20V.

Trade Name	Composition	Bmax (kG)	Core Loss @ Bmax	Squareness Ratio	Turns Req'd	I_M (A)
Sq. Permalloy 80	79% Ni, 17% Fe	7	1.2W	0.9	19	0.04
Supermalloy	78% Ni, 17% Fe, 5% Mo	7	1.0W	0.55	19	0.03
Orthonol	50% Ni 50% Fe	14	7.2W	0.97	10	0.39
Sq. Metglass	Fe, B	16	7.6W	0.5	9	0.06
Power Ferrites	Mn, Zn	4.7	1.8W	0.4	11	0.1
Sq. Ferrite (Fair-Rite #83)	Mn	3.9	2.8W	0.9	13	0.4

Figure 10. A comparison of several types of core materials available for mag-amp usage.

In addition to selecting the core material, there are additional requirements to define, such as:

1. Regulator output voltage
2. Maximum output current
3. Input voltage waveform including limits for both voltage amplitude and pulse width
4. The maximum volt-seconds — called the "withstand Area," Λ — which the mag amp will be expected to support.

With these basic facts, a designer can proceed as follows:

1. Select wire size based on output current. 400 Amp/cm² is a common design rule.
2. Determine core size based upon the area product:

$$Aw\,Ae = \frac{Ax \bullet \Lambda \bullet 10^8}{\triangle B \bullet K} \quad \text{where}$$

Aw = Window area, cm²
Ae = Effective core area, cm²
Ax = Wire area, (one conductor) cm²
Λ = Required withstand area, V-sec
$\triangle B$ = Flux excursion, gauss
K = Fill factor ≈ 0.1 to 0.3

3. Calculate number of turns from

$$N = \frac{\Lambda \bullet 10^8}{\triangle B\,Ae}$$

4. Estimate control current from

$$Ic \approx \frac{H\ell e}{0.4\,\pi\,N} \quad \text{where}$$

ℓe = core path length, cm

H is taken from manufacturer's curves. Note that it increases with frequency.

5. Check the temperature rise by calculating the sum of the core loss and winding loss and using

$$\triangle T \approx \left(\frac{P \text{ watts}}{A \text{ (surface) cm}^2}\right)^{0.8} \times 444°C$$

6. Once the mag amp is defined, it can be used in the power supply to verify Ic and to determine the modulator gain so that the control requirements may be determined.

Compensating the Mag Amp Control Loop

The mag amp output regulator is a buck-derived topology, and behaves exactly the same way with a simple exception. Its transfer function contains a delay function which results in additional phase delay which is proportional to frequency. This phenomenon will be considered in more detail later.

Figure 11 shows the entire regulator circuit, with the modulator, filter, and amplifier blocks identified. The amplifier, with its lead-lag network, is composed of the op-amp plus R1, R2, R3, C1, C2, and C3. The modulator, for the purpose of this discussion, includes the mag amp core, the two rectifier diodes, plus the reset driver circuit which is composed of D1, Q1, and R7.

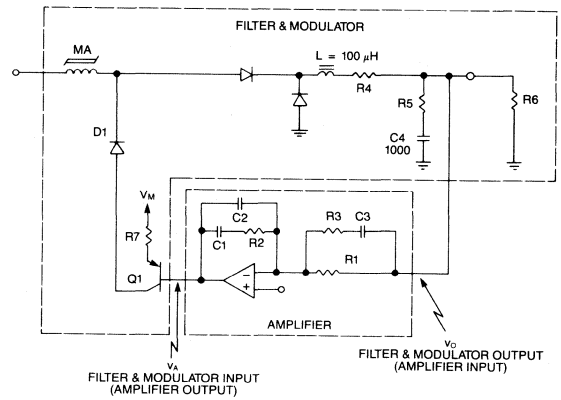


Figure 11. Schematic diagram of the regulator control loop.

The basic filter components are the output inductor (L) and filter capacitor (C4). R4 and R5 are the parasitic resistances of these components. The load resistor (R6) is also included, since it determines the damping of the filter.

The purpose of proper design of the control loop is to provide good regulation of the output voltage, not only from a dc standpoint, but in the transient case as well. This requires that the loop have adequate gain over as wide a bandwidth as practical, within reasonable economic constraints. These are the same objectives we find in all regulator designs, and the approach is also the same.

A straightforward method is to begin with the magnitude and phase response of the filter and modulator, usually by examining its Bode plot. Then we can choose a desired crossover frequency (the frequency at which the magnitude of the transfer function will cross unity gain), and design the amplifier network to provide adequate phase margin for stable operation.

Figure 12 shows a straight-line approximation of the filter response, ignoring parasitics. Note that the corner frequency is $1 / (2\,\pi\,\sqrt{LC})$, or 316 Hz, and that the magnitude of the response "rolls off" at a slope of –40 dB per decade above the corner frequency. Note also that the phase lag asymptotically approaches 180 degrees above the corner frequency.

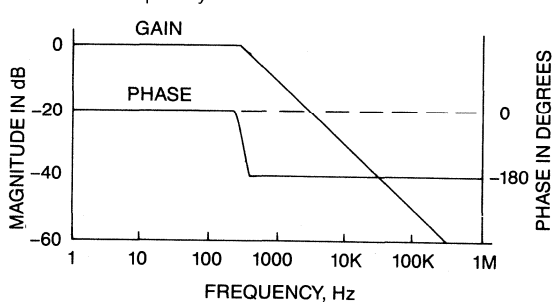


Figure 12. Output filter response.

Figure 13 shows the straight-line approximation of the combined response of the filter and modulator. With a modulator gain of 10, flat to frequencies well above the region of interest here, the magnitude plot has simply been shifted upward by 20 dB.

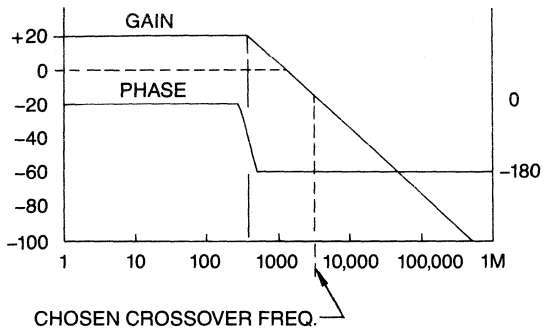


Figure 13. Filter-modulator response.

If we close the loop with an inverting error amplifier, introducing another 180 degrees of phase shift, and cross the unity gain axis above the corner frequency, we will have built an oscillator — unity gain and 360 degrees of phase shift.

An alternative, of course, is to close the loop in such a way as to cross the unity-gain axis at some frequency well below the corner frequency of the filter, before its phase lag has come into play. This is called "dominant pole" compensation. It will result in a stable system, but the transient response (the settling time after an abrupt change in the input or load) will be quite slow.

The amplifier network included in Figure 11 allows us to do a much better job, by adding a few inexpensive passive parts. It has the response shown in Figure 14. The phase shift is shown without the lag of 180 degrees inherent in the inversion. This is a legitimate simplification, provided that we use an overall lag of 180 degrees (not 360 degrees) as our criterion for loop oscillation.

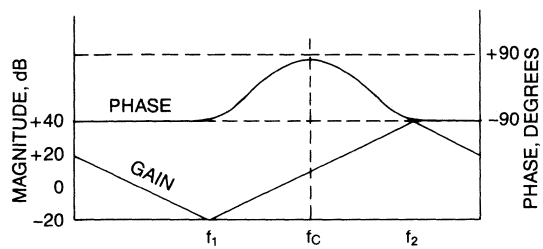


Figure 14. Amplifier response.

The important point is that this circuit provides a phase "bump" — it can have nearly 90 degrees of phase boost at a chosen frequency, if we provide enough separation between the corner frequencies, f1 and f2. This benefit is not free, however. As we ask for more boost (by increasing the separation between f1 and f2) we demand more gain-bandwidth of the amplifier.

Additional Phase Shift of the Modulator

Using the usual time-averaging technique, we can justify the linear model of the filter and modulator. The modulator is represented by its dc gain, v_O/v_A, and a phase shift term which accounts for its time delay. This phase delay has two causes:

1. The output is produced after the reset is accomplished. We apply the reset during the "backswing" of the secondary voltage, and then the leading edge of the power pulse is delayed in accordance with the amount of reset which was applied.
2. The application of reset to the core is a function of the impedance of the reset circuit. In simple terms, the core has inductance during reset which, when combined with the impedance of the reset circuit, exhibits an L-R time constant. This contributes to a delay in the control function.

The sum of these two effects can be expressed as:

$$\varnothing_M = (2D + \alpha)\ \frac{\omega}{\omega_S}\ , \text{where}$$

$\varnothing_M$ = Modulator phase shift
D = Duty ratio of the "off" time
α = resetting impedance factor: = 0 for a current source, = 1 when resetting from a low-impedance source, and somewhere in between for an imperfect current source.
ω_S = $2\pi f_S$, where f_S = the switching frequency.

When the unity-gain crossover frequency is placed at or above a significant fraction (10%) of the switching frequency, the resultant phase shift should not be neglected. Figure 15 illustrates this point. With α = 0, we insert no phase delay, and with α = 1 we insert maximum phase delay which results from resetting from a voltage source (low impedance). The phase delay is minimized in the UC1838 by using a collector output to reset the mag amp.

The phase shift shown in Figure 15 is a result of both the impedance factor and duty ratio effects. In the case of resetting from a current source, the delay due to duty ratio is the more significant.

It is difficult to include this delay function in the transfer function of the filter and modulator. A simple way to handle the problem is to calculate the Bode plot of the filter/modulator transfer function without the delay function, and then modify the phase plot according to the modulator's phase shift.

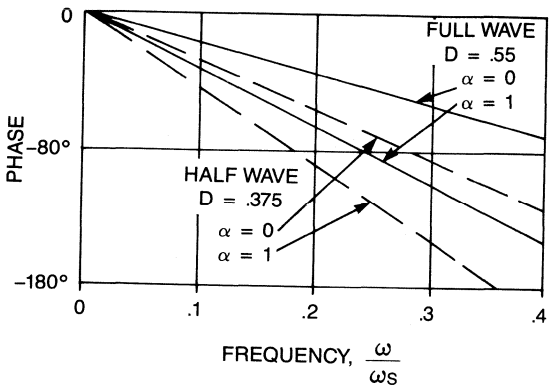


Figure 15. Mag-amp phase shift.

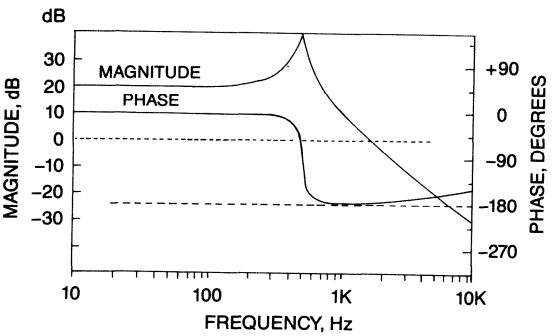


Figure 16. Filter-modulator response neglecting modulator phase shift.

Design Example

As an example, consider a 10 V, 10 A output to be regulated with a mag amp. Assume that the output inductor has been chosen to be 100 μH, and that the output capacitor is 1000 μF. Each has .01 ohms of parasitic resistance, and the load resistor is 1 ohm.

We begin by plotting the response of the filter/modulator. In order to do this, we must determine the dc gain of the modulator. This can be done experimentally by applying a variable voltage, V_A to the base of Q1, adjusting it to set t he output, V_O, to 10 V and then making a small change around the nominal value to determine the incremental gain. Assume that a 0.1 V change in V_A results in a 1 V change in the output; this gives a gain of 10. For a first look, the phase delay of the modulator is set at zero by choosing α = 0 and D = 0. The result is the plot of Figure 16. Note that the crossover frequency is approx. 1.6 KHz, at which the phase margin is only about 15 degrees.

Figure 17 illustrates the effect of phase shift, by setting α = .2 and D = .6. Note that the crossover frequency is unchanged, but that the phase margin is now approximately zero. The loop can be expected to oscillate.

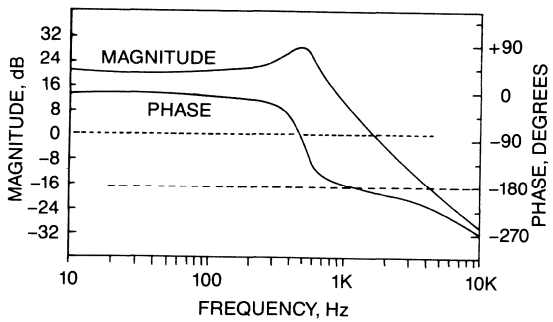


Figure 17. Filter-modulator response, with modulator's phase shift.

Dean Venable, in his paper, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," has derived a simple procedure for designing the amplifier network. In summary, the procedure is as follows:

1. *Make a Bode Plot of the Modulator.* This can be done with the use of a frequency response analyzer, or it can be calculated and plotted, either with the use of a simple straight-line approximation or with the use of one of the available computer analysis programs. Don't forget to include the effect of the filter capacitor's ESR (equivalent series resistance), using its minimum value, since this presents the worst case for loop stability. Also, include the modulator's phase shift.
2. *Choose a Crossover Frequency.* The objective, of course, is to make this as high as possible for best (fastest) transient response. The limiting condition on this choice is as follows: The amplifier can provide, as a theoretical maximum, 90 degrees of phase boost, or — stated another way — 180 degrees of boost from its inherent 90 degrees of phase lag. We will work with this latter convention, and assign it the symbol B_C, the boost at the crossover frequency. The required B_C, then is:

   $B_C = M - P - 90$, where

   M = Desired Phase Margin, and
   P = Filter & Modulator Phase Shift.

   Examining this relationship, we can see that the Desired Phase Margin is $M = B_C + P + 90$,

and hence if the filter-modulator phase shift is 180 degrees, the theoretical limit of phase margin is 90 degrees. Since an acceptable minimum phase margin for reasonable transient response is around 60 degrees, we deduce that we must choose a corner frequency below that at which the filter and modulator phase lag is:

$P = M - B_C - 90$, or $P = 60 - 180 - 90 = -210$

To accomplish this we would have to separate the amplifier's two corner frequencies by infinity. A more practical case is to choose -190 degrees as a limit — maybe even less, since separating these frequencies (for more phase boost) may require an impractical amount of gain-bandwidth in the amplifier.

With this guideline in mind, we establish the criterion that:

$P > -190$ degrees.

Combining this with the earlier criterion of not trying to cross over at a frequency greater than one-tenth the switching frequency, we have:

$$f_C = .1\ f_s,$$

— or —

f_C = the frequency where the filter-modulator's phase shift has fallen to −190 degrees.

Choose the result which yields the lower crossover frequency.

It is a coincidence in this design example that the filter-modulator phase shift is −190 degrees at approximately 2 KHz, one-tenth the switching frequency. In this case, the choice of the crossover frequency is unanimous!

Dean Venable's "K Factor" is the ratio between the two corner frequencies, f1 and f2:

$K = f2 / f1$

and, the two frequencies are centered geometrically about the crossover frequency. Therefore, $f1 = fc/\sqrt{K}$, and $f2 = fc\sqrt{K}$.

In this design example, we have chosen 2 KHz as our crossover frequency, where the modulator's phase lag is −190 degrees, and wish to have 60 degrees of phase margin. The result is:

$B_C = 60 - (-190) - 90 = 160$ degrees

3. *Determine the Required Amplifier Gain.* This one is simple! The amplifier must make up the loss of the filter and modulator at the chosen crossover frequency. In this example, the filter and modulator has approximately −3 dB at the crossover frequency of 2 KHz, and hence the amplifier must have a gain of 1.41 (+3 dB) at 2 KHz.

With this information now at hand, we're ready to crank out the values of the amplifier components, as explained in Mr. Venable's paper:

$K = (\text{Tan}\ [(Bc/4) + 45])^2$

$C2 = 1 / (2\ \pi\ f\ G\ R1)$

$C1 = C2\ (K - 1)$

$R2 = \sqrt{K} / (2\ \pi\ f\ C1)$

$R3 = R1 / (K - 1)$

$C3 = 1 / (2\ \pi\ f\ \sqrt{K}\ R3)$

where f = crossover freq. in Hz, and G = amplifier gain at crossover (expressed as a ratio, not dB)

Figure 18 shows the response of this amplifier over the frequency range of interest.

Incidentally, the value for K is 130.65, and the corner frequencies are 175 Hz and 22,860 Hz.

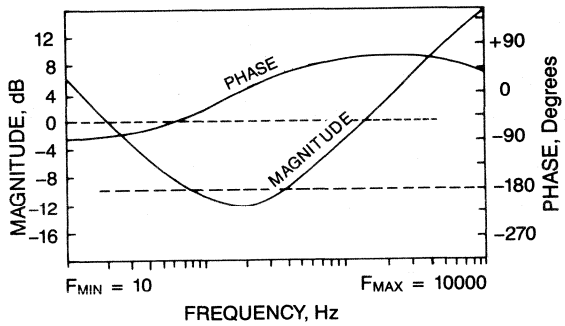


Figure 18. Compensated error amplifier response.

Combining the amplifier's response with the filter and modulator response results in the overall loop response, and this is shown in Figure 19. Note that the crossover frequency is 2 KHz, and that the phase shift is −120 degrees (60 degrees of phase margin).

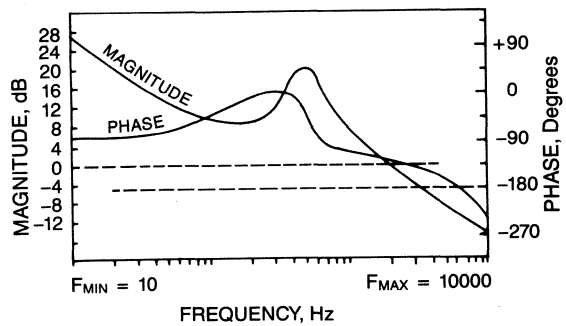


Figure 19. Overall regulator loop response.

Check the Gain-Bandwidth Requirement for the Amplifier

To avoid disappointment, it is wise to check to see that the design does not require more gain-bandwidth than the amplifier can provide. This is fairly easy to do. We can simply calculate the gain-bandwidth product at f2, since above this frequency the amplifier can be expected to be rolling off at the same −20 dB/decade slope. The gain at f2 is:

$G_{f2} = \sqrt{K}\ G$, and hence the required gain-bandwidth is:

$GBW = \sqrt{K}\ G\ f2 = KGf$ since $f_2 = \sqrt{K}\ f$

In this example the result is 368 KHz, well below the gain-bandwidth of the amplifier in the UC1838. If it had not been so, we would have had two choices: We could settle for a lower crossover frequency or less phase margin (not recommended), or add another amplifier in cascade with the one in the UC1838. The added amplifier would simply be designed as a non-inverting amplifier with modest gain and placed after the output of the existing amplifier. We might also examine the possibility of increasing the gain of the modulator by increasing the number of turns on the mag amp.

Full-Wave Mag Amp Outputs

Although the examples thus far have explored the forward converter (a half-wave topology), mag amp output regulators also work well with half-bridge and full bridge converters (full-wave topologies). Two saturable reactors are required, as shown in Figure 20. Since the output current is shared by the two reactors, the cores can be smaller than the single core of a half-wave topology of the same power level.

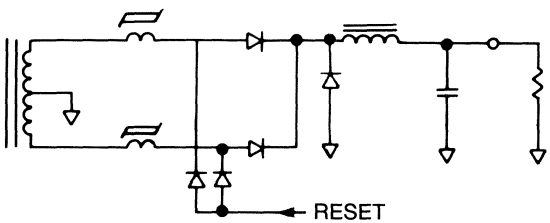


Figure 20. Full-wave output regulator.

Converters with Multiple Mag Amp Outputs

There is no limit to the number of outputs which can be employed on a single converter, or even from a single secondary winding of the transformer. Recall, however, that the mag amp regulator is like a conventional buck regulator and can only provide voltages which are lower than that which would occur if the mag amp were not present.

Loop stability does not become complicated by the addition of more output regulators. The task is simply to stabilize each of the regulator control loops in the normal fashion.

Interaction of the Mag Amp Loop with the Main Converter Control Loop

There are no surprises here. The output regulator behaves like a second converter (buck regulator) cascaded with the main converter. If both are stable when considered individually, they will not upset each other.

When considering the two circuits as a cascade, it is reasonable that if the output regulator responds quickly to a load transient, this perturbation will be presented to the main converter. The main loop will then deal with this if it senses the effect at the sensing point.

Interaction with the Converter's Input Filter

Assuming the absence of current-mode control of the main converter, the only significant interaction of the mag amp outputs will be with the input filter. But this is not a problem if the filter is properly damped in accordance with the negative resistance presented by the input of the converter. A simple way to ensure stability is to determine the maximum-load negative input resistance of the converter at low frequency (the ratio of the change in input power to a small change in input voltages, squared), then damp the input filter so that the magnitude of its output impedance is always below this value.

Continuous vs. Discontinuous Conduction of the Output Inductor

It is possible to operate the mag amp regulator with its output choke in the discontinuous mode, provided that the mag amp's winding is designed to reduce the pulse width accordingly. When this is done, the mag amp can reduce the pulse width to maintain output regulation even when the load current falls below the "critical" current of the output inductor. Transient response is affected just as it is in a simple buck regulator; it becomes poorer as the corner frequency falls.

References

1. Mullett, Charles, "Design and Analysis of High Frequency Saturable-Core Magnetic Regulators," Powercon II, April 1984.
2. Venable, H. Dean, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," Proceeding of Powercon 10, March 1983.
3. Unitrode IC Corp. acknowledges and appreciates the support and guidance given by the Power Systems Group of the NCR Corporation, Lake Mary, Fla. in the development of the UC1838.